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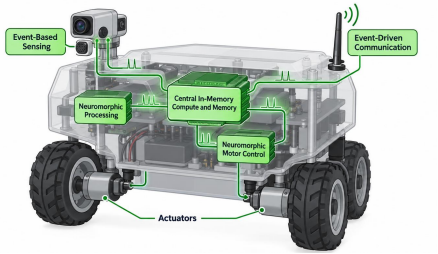
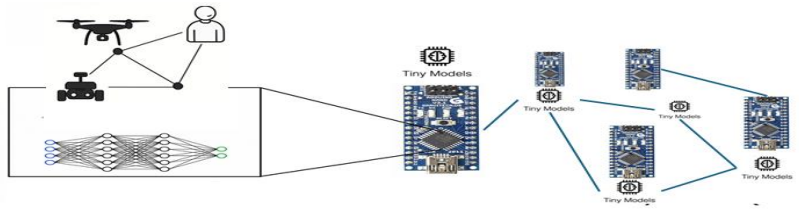



## Sovereign AI at the Edge Heterogeneous, Decentralised and Collaborative Compute

**Spotlight to European Innovation SemiCon 2026**

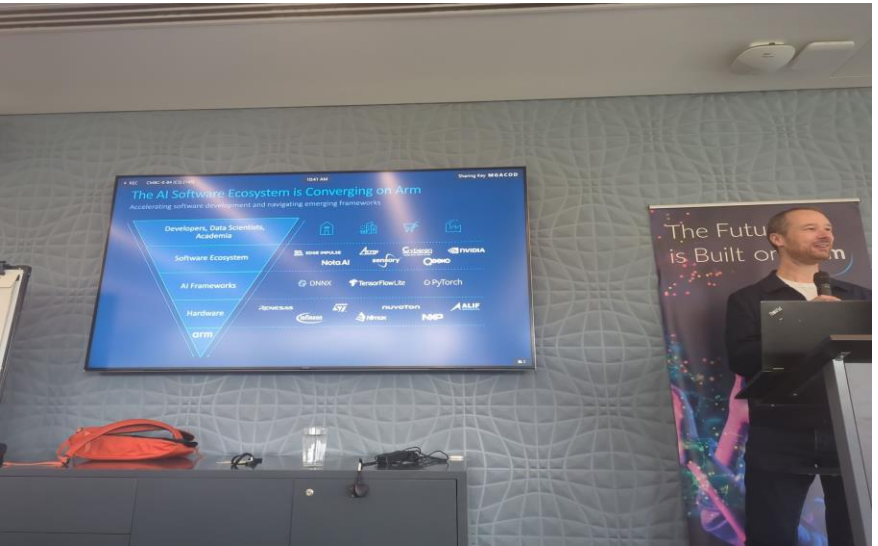
# Why do we need collaborative AI and heterogenous chips



Engineering and Physical Sciences Research Council

TinyML UK

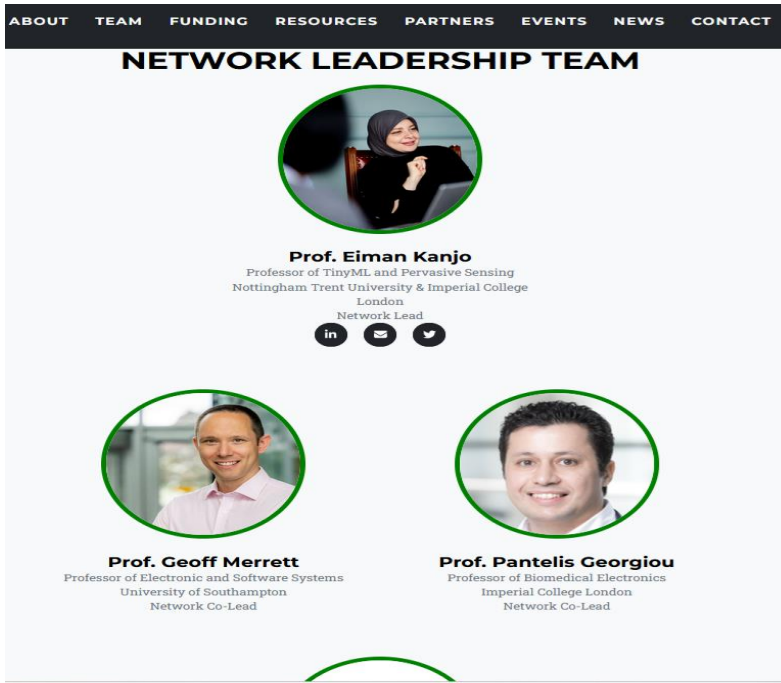



**EPSRC TinyML UK Network**

https://www.tinyML.uk



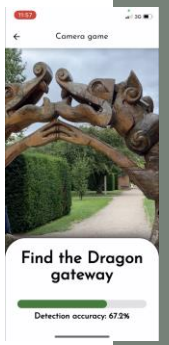
Engineering and Physical Sciences Research Council

Green+ Network

https://www.greenplus.uk

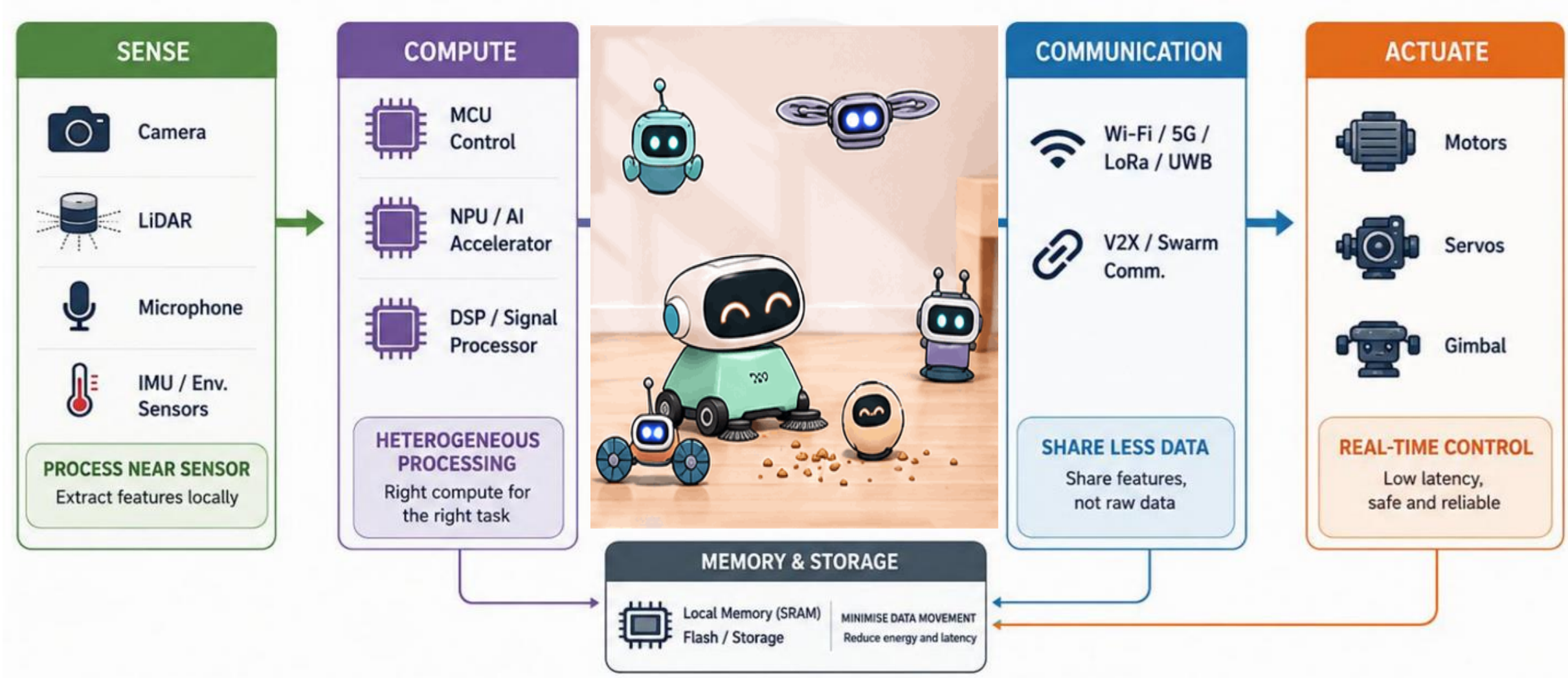
# Bringing Edge AI and pervasive technology to Engineer Healthier Environments






# Heterogeneous Compute for Physical and Contextual AI




**AI must operate where data are generated and where decisions have physical consequences.**

# Models for Physical AI

**SMALL**

**fits**

**SPECIALISED**

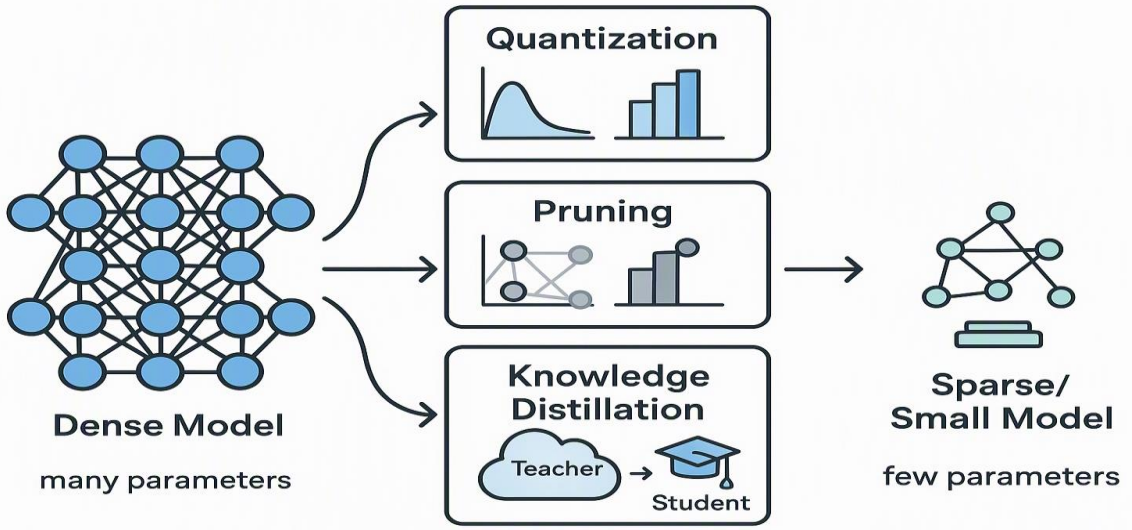
**understands**

**COLLABORATIVE**

**combines**

**OPEN-WEIGHT**

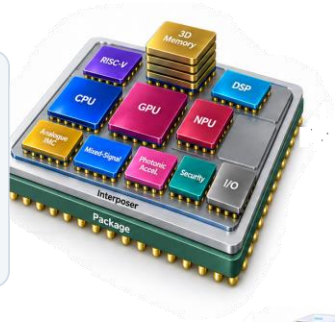
**can evolve**



# The Three Levels of Heterogeneous Intelligence

**1** **WITHIN THE CHIP**

Different cores and accelerators




**2** **WITHIN THE DEVICE**

Digital, analogue and neuromorphic units




**3** **ACROSS DEVICES**

Independent nodes combine capabilities



# Chip Heterogeneity

e.g. Apple debuted M6 in the new Mac mini and M5 Ultra in the new Mac Studio.

https://www.apple.com/uk/newsroom/2026/08/apple-introduces-m6-and-m5-ultra-for-a-big-leap-in-performance-and-ai-compute/

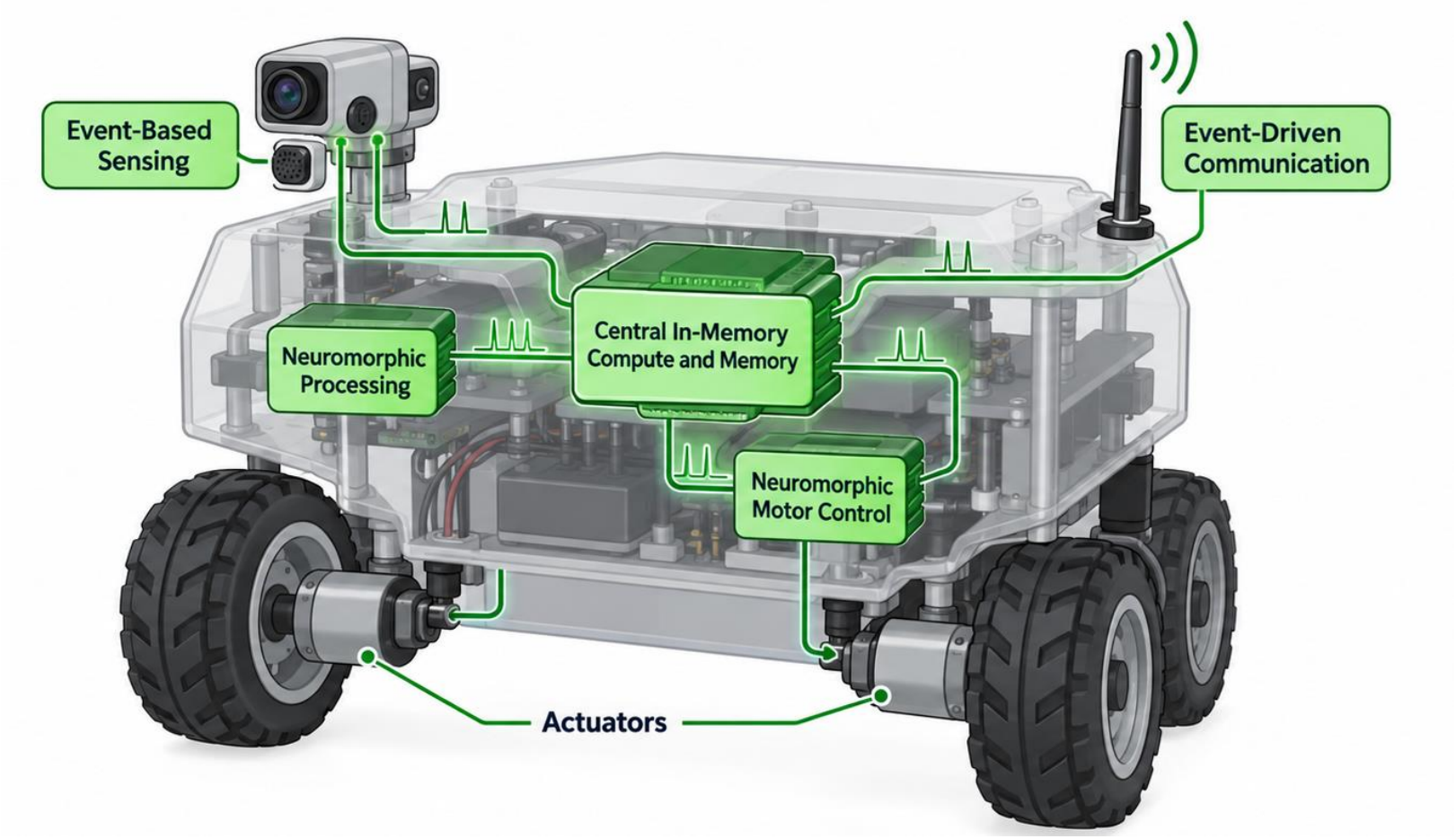
M6, Apple's first state-of-the-art 2-nm chip, advances every compute block, delivering gains across every dimension of performance.

The chip features a larger **12-core CPU** complex with the world's fastest CPU core, a larger **12-core GPU** with **Neural Accelerators**, **a Dual 16-core Neural Engine**.

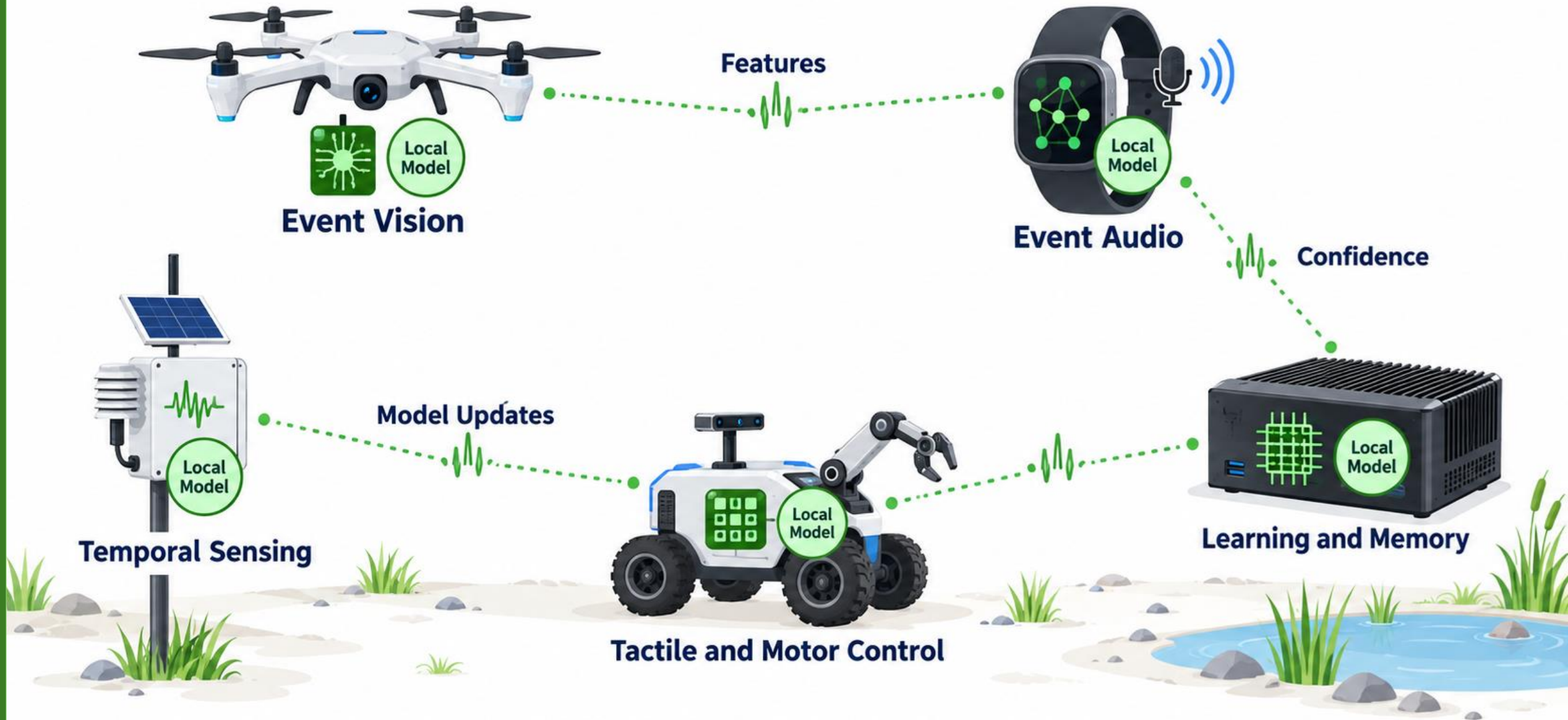
M5 Ultra, uses UltraFusion technology to form a quad-die architecture for the first time in an M-series system on a chip (SoC). The chip includes an **up-to-36-core CPU** and **up-to-80-core**.



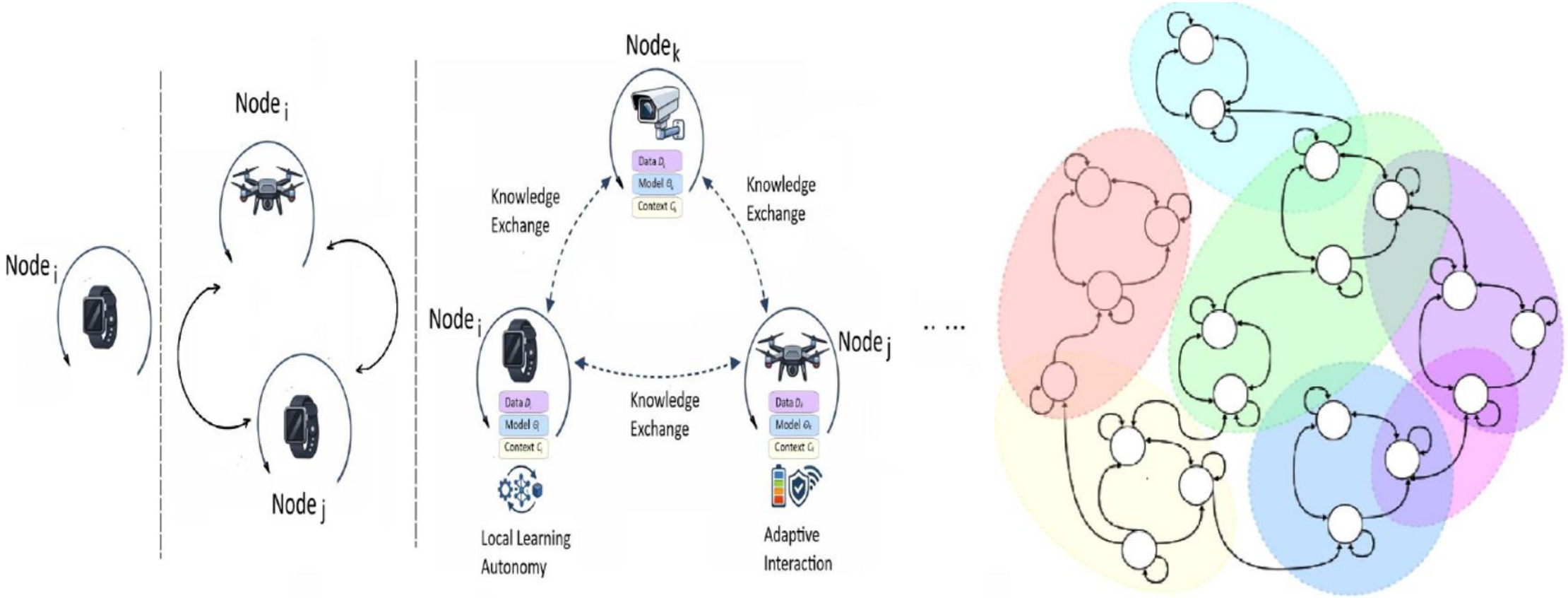
# Heterogeneity within a robot



# Heterogeneity Across Devices



# Node Learning: A Framework for Adaptive, Decentralised and Collaborative Network Edge AI




https://wiki.edgeaifoundation.org/working-group/node-learning/

Node Learning: A Framework for Adaptive, Decentralised and Collaborative Network Edge AI, E Kanjo, M Aslanov, arXiv preprint arXiv:2602.16814, 2026

# What neuromorphic computing contributes

**EVENT-DRIVEN**

Compute follows activity

**TEMPORAL**

Time carries information

**LOCAL STATE**

Memory close to processing

**ASYNCHRONOUS**

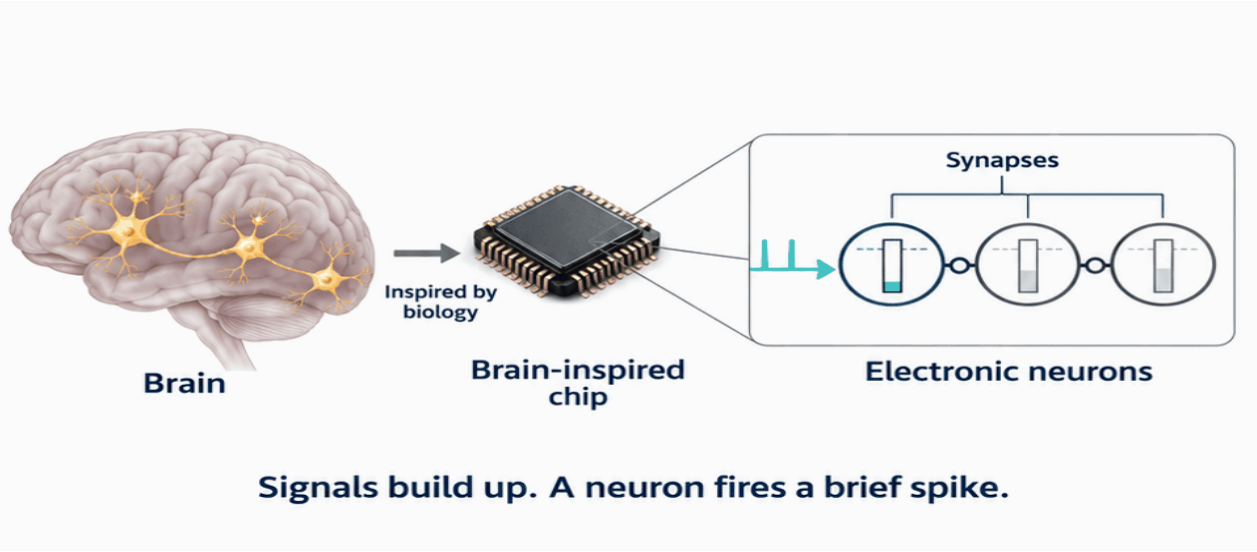
No single global clock required

**PARALLEL**

Many states update together

**SPARSE**

Communicate selected events

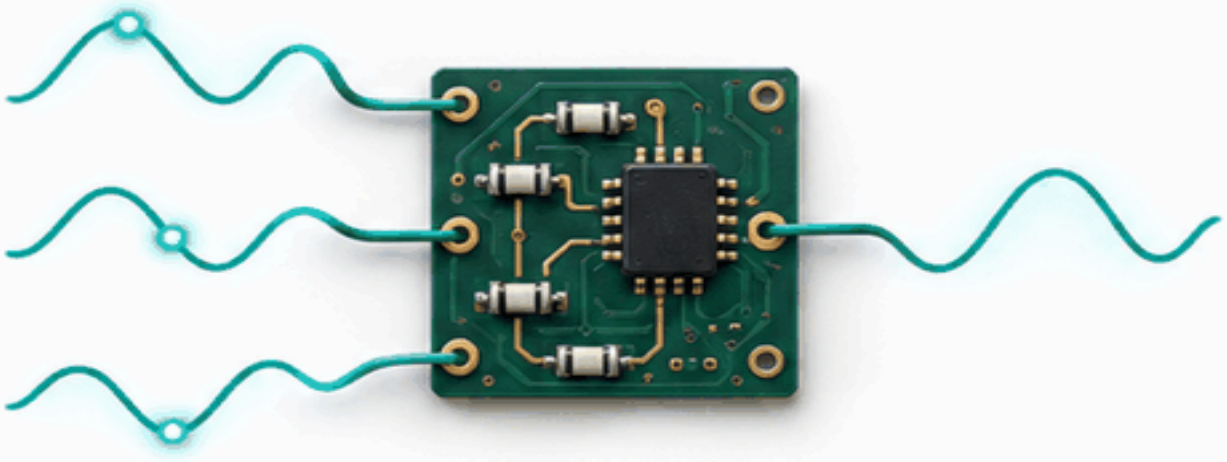



**Neuromorphic hardware may be digital, analogue or mixed-signal.**

# Future Compute

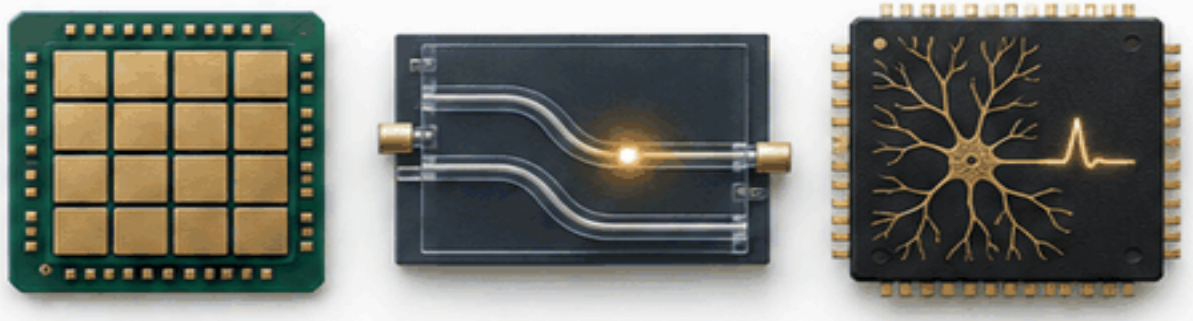
*The von Neumann bottleneck limits what a microcontroller can deliver*

## Analogue computing



Physical signals carry out calculations

## Novel computing



In-memory | Photonic | Neuromorphic

Different hardware for different tasks

These approaches can overlap and can work alongside digital processors.

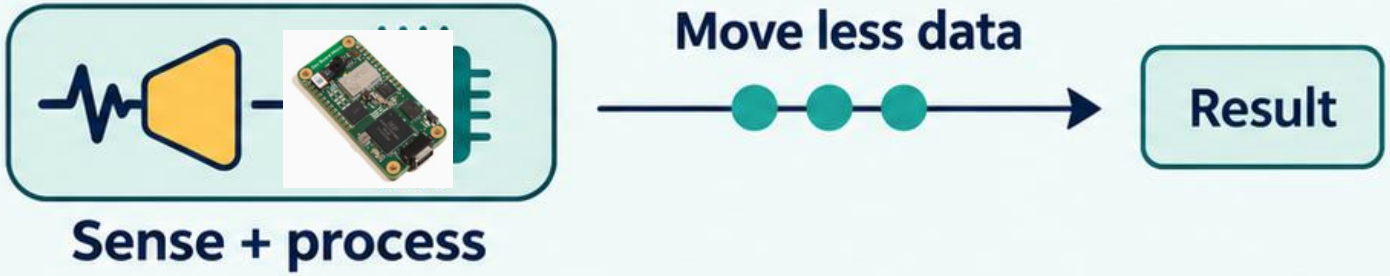
Engineering and Physical Sciences Research Council

# ProSensing: Low-power, high-speed, adaptable PROcessing-in-SENSING

## Conventional approach



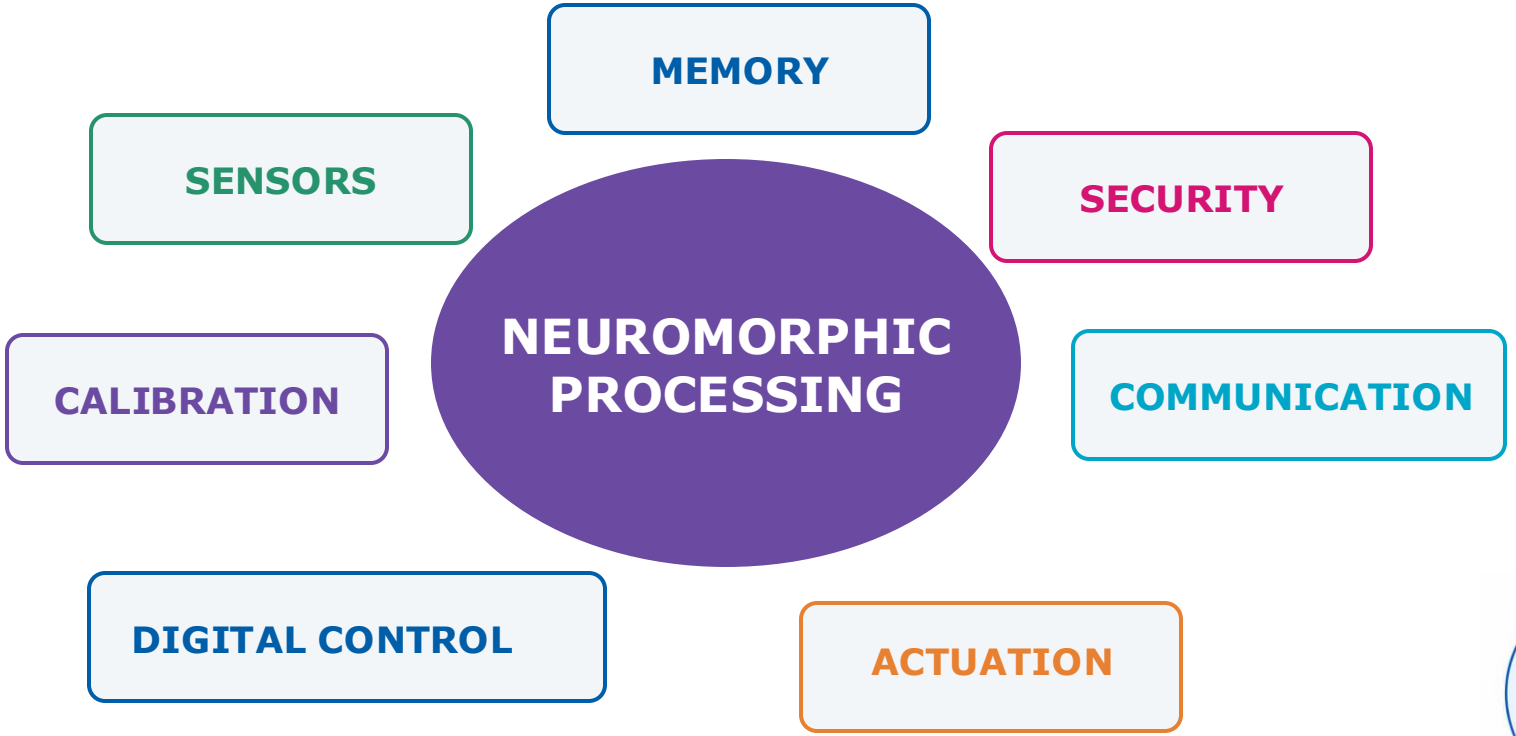

## ProSensing approach

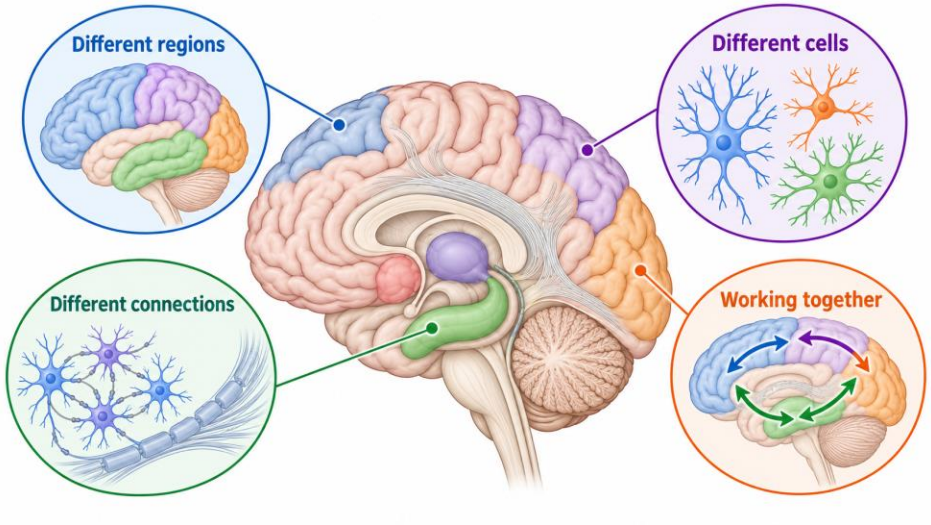



Less data movement | Potentially lower energy | Faster local responses

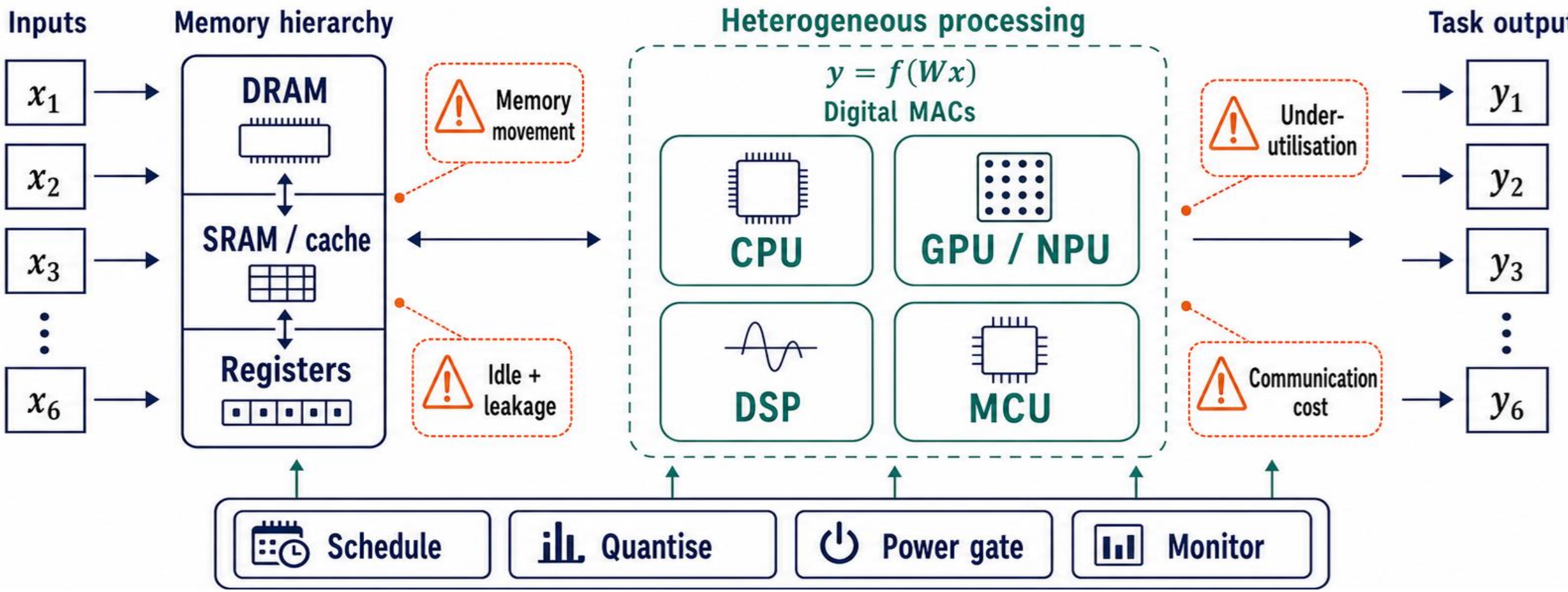
Analogue processing and memory-based pattern matching can help.

# A neuromorphic processor is one part of the system
# Can the whole system become neuromorphic?



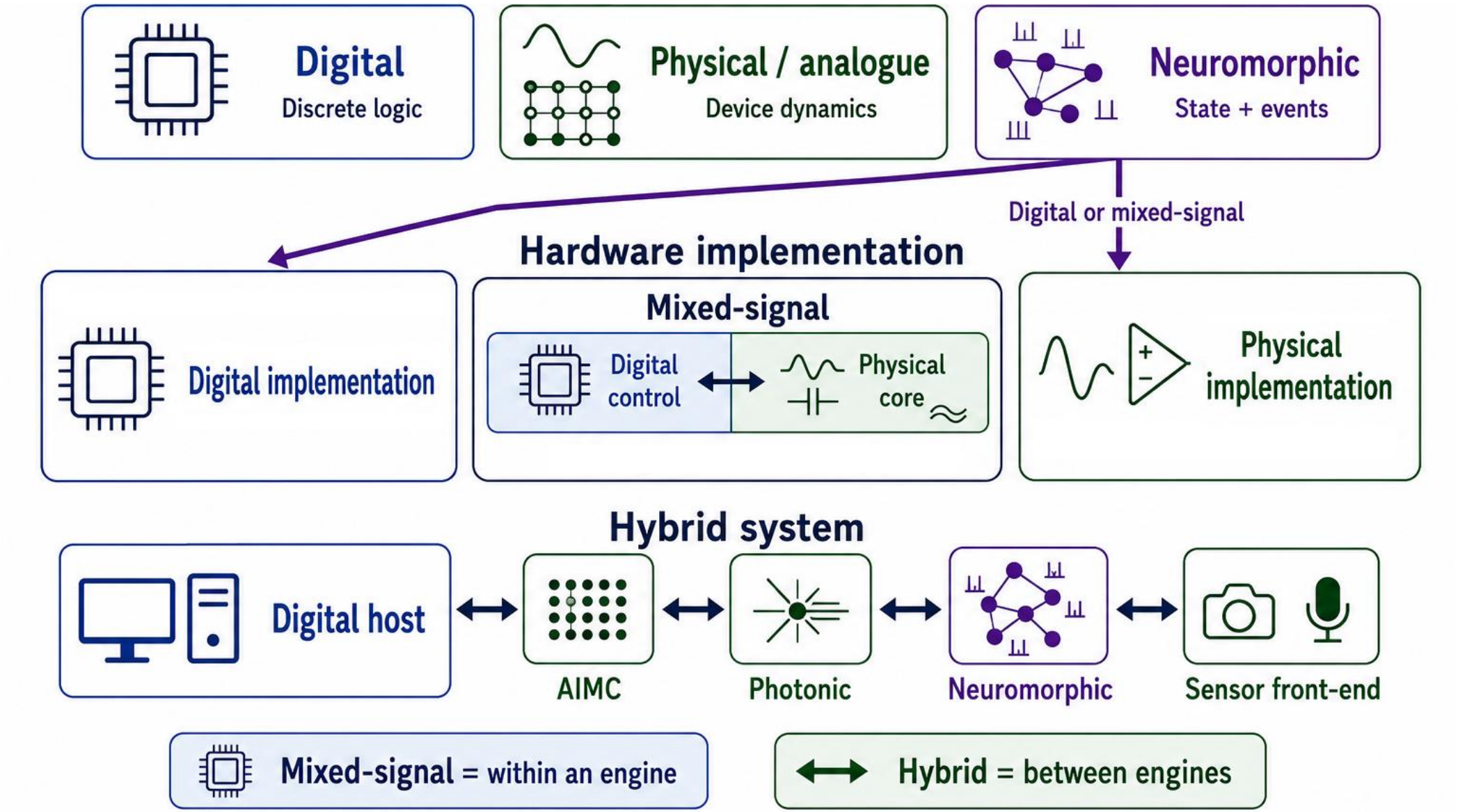



*Beyond Peak TOPS/W: A System-Level Perspective on Hybrid Digital, Analogue and Neuromorphic Computing.*




*Kanjo, E., & De Silva, V. (2026). Beyond Peak TOPS/W: A System-Level Perspective on Hybrid Digital, Analogue and Neuromorphic Computing.*

# Physical computing as specialised acceleration



# Energy is a system property

**E system =**

- SENSING
- + COMPUTE
- + MEMORY
- + CONVERSION
- + COMMUNICATION
- + CONTROL

**Compare complete systems at matched accuracy, latency, workload and operating conditions.**

**Beyond peak TOPS/W**

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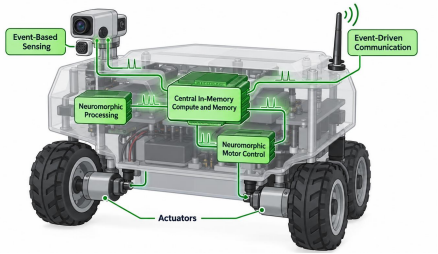


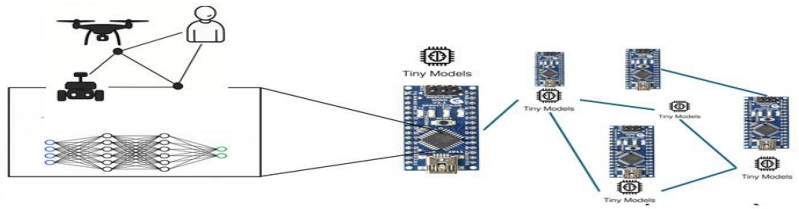


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