

SPEAKER

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Biography

Dr. Kim is a Principal Engineer in the DRAM Metrology Technology team within the Infra Technology Center at SK hynix. He leads inline analysis technology related to X-ray and optical metrology, as well as the analysis of physical properties in semiconductor processes and integration. He received his Ph.D. from KAIST in 2017 and his M.S. from Korea University in 2003. His research focuses on the physical and chemical behavior of next-generation and manufacturing memory devices based on nanoscale structures, multilayer films, and novel materials. He has proposed nanoscale metrology techniques, and the results obtained using inline metrology have shown good agreement, demonstrating the feasibility of these experiments for understanding end-of-line electrical properties. He has also shown that accurate characterization of physical properties is critical for material design and simulation of low-k and high-k thin films, which are susceptible to electrical degradation during product processing and handling and can directly affect final product yield.

Publications and Achievements (2013~Present)

1. **Jae Hyun Kim**, et al.; Electronic Materials Letters, **(2017)**, 13.2: 120-128.
2. Joo Young Jung, Nadeem Qaiser, Gang Feng, Byung-il Hwang, Taegeon Kim, **Jae Hyun Kim**, Seung Min Han, Physical Chemistry Chemical Physics, 19, 1311-1319, **(2017)**
3. **Jae Hyun Kim**, et al.; ECS Journal of Solid State Science and Technology, 5, 438-440, **(2016)**

4. **Jae Hyun Kim**, et al. Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, **(2016)**, 34.4: 041208.
5. YOO, Woo Sik; **KIM, Jae Hyun**; HAN, Seung Min, Journal of Micro/Nanolithography, MEMS, and MOEMS, 13, 011205, **(2014)**
6. Sun-Wook Kim, Dae-Seop Byun, Mijin Jung, Saurabh Chopra, Yihwan Kim, **Jae-Hyun Kim**, Seung-Min Han, Dae-Hong Ko, Hoo-Jeong Lee, APPLIED PHYSICS EXPRESS, v.6, no.6 **(2013)**

Abstract

최근 소재 개발과 EUV 리소그래피 기술의 비약적인 발전에 따라 고집적 메모리 양산용 소자 기술은 현저한 발전을 이루어 왔다.

그럼에도 불구하고 박막 내 물리적·화학적 결함, 소재의 본질적 물성, 그리고 박막 간 계면 특성은 아직 충분히 규명되지 않았다.

본 과정에서는 박막의 물리적 특성과 더불어 계면 특성에 대한 심층적 고찰의 필요성을 제시한다. 더 나아가 다양한 소자 통합 및 메모리 제조 공정 전반에서 전기적·물리적 결함을 민감하게 분석할 수 있는 신규 특성 평가 기법을 소개하고자 한다.

Recent advances in materials development and EUV lithography have driven substantial progress in device technology for high-volume memory manufacturing.

However, the physical and chemical defects in thin films, the intrinsic properties of materials, and the properties of interfaces between thin films are still not fully elucidated.

This study highlights the necessity of examining both the physical properties of thin films and interfacial characteristics.

In addition, we will discuss novel characterization metrologies that enable sensitive analysis of electrical and physical defects in diverse device integration and memory manufacturing contexts.