

Position Paper

A close-up, high-angle photograph of a silicon wafer with multiple dies. The wafer is illuminated with a spectrum of colors, including red, orange, yellow, green, and blue, creating a vibrant, multi-colored pattern across the surface of the chips.

European Chips Act 2.0

Executive Summary

The European Chips Act marked a milestone for Europe's semiconductor industry. Since its adoption in 2023, the Act has strengthened the EU's semiconductor capabilities, catalysing over **€69 billion** of investments powering new research and manufacturing capacities across the continent. **SEMI Europe members** broadly support the Chips Act's objectives and structure. However, several structural challenges could limit its long-term success and the broader spillover benefits for Europe if not promptly addressed.

A "**Chips Act 2.0**" is needed to deliver process-efficient, fast scale-up and industrialisation solutions across the entire European semiconductor value chain, from R&D and design through materials, equipment, and front- and back-end manufacturing. By aligning the objectives of the Chips Act 2.0 with other legislative frameworks, embedding it within a broader EU Tech Strategy, and deploying new policy instruments, these measures could transform it into a truly strategic tool.

To guarantee that the Chips Act 2.0 will effectively respond to the concerns and needs of the semiconductor ecosystem in Europe, SEMI Europe highlights the following key points:

SEMI Europe – Policy Recommendations for a Chips Act 2.0

- 1. Closing the Industrialisation Gap:** Close Pillar I's industrialisation gap by including a budget line for the participation of the industry into research pilot line projects, establishing dedicated industrialisation pilot line programmes and providing a preferential and simplified access to Pillar II state support measures for investments linked to Chips Act pilot lines. Adopting tailored measures for smaller players, via pilot line vouchers and budget lines for SMEs, start-ups and scale-ups is equally important to best achieve the development of parallel enabling technologies, products and supply chains.
- 2. A "First-Of-A-Kind" for the Value Chain:** Expand the "First-Of-A-Kind" (FOAK) definition to effectively capture all segments of the semiconductor supply chain, from chip design to equipment, materials and components, and their related research and product development activities. Create new categories for these segments in addition to the "Integrated Production Facility" and "Open EU Foundry".
- 3. A Process-Efficient Chips Act 2.0:** Deliver simplified administrative and reporting procedures under Pillar I, considering the business realities of the semiconductor ecosystem, including the limited resources of SMEs, start-ups and scale-ups. Establish a fast-track process and a single point of contact (One-stop-shop) within the Commission to receive and dispatch Pillar II applications while harmonising procedures and information requirements, with a legally binding and defined timeline for applications' processing.
- 4. Cross-Policy Alignment:** Coherently and efficiently integrate the Chips Act 2.0 in the wider network of EU policies to secure the competitiveness of Europe's semiconductor ecosystem, incentivising cross-sector synergies and promoting chips' integration across various end-user applications by delivering a European Technology Strategy that aligns different legislations' objectives and mechanisms.
- 5. An Enhanced Policy Toolbox:** Explore and incentivise the adoption of new policy instruments to increase the global attractiveness of the EU for semiconductor investments, including a dedicated Chips Act governing body, tax incentives, specific measures relative to the size of businesses, water and energy supply guarantees, and support to European Semiconductor Consortiums.
- 6. A Consultative Policy-Making Grounded into Business Realities:** Under Pillar III, integrate a multi-level and systematic consultation process between the European Commission, Member States, via the European Semiconductor Board (ESB), and the semiconductor industry while safeguarding data confidentiality.

1. Closing the Industrialisation Gap

Accelerate Chips Act industrialisation via specific budget allocations for industry participation, tailored measures for SMEs and start-ups, preferential access to Pillar II state aid for industrial projects developed in the frame of Chips Act pilot lines and the creation of dedicated industrialisation pilot lines.

The success of pilot lines will depend largely on companies' ability to adopt their technological outputs. This adoption requires the parallel co-development and qualification of complementary semiconductor technologies and products, including chip design tools, process materials, specialty chemicals, and equipment.

So far, the Chips Act pilot lines are “research” pilot lines that provide funding exclusively to public research organisations, namely RTOs and academia. Under the current framework, **companies willing to participate in pilot line projects must cover all participation costs**¹. These costs have often **disincentivised companies to participate in these research projects** and are unbearable for SMEs, start-ups and scale-ups, reducing the ultimate success rate of the projects².

To close this industrialisation gap, **increasing industry participation in research pilot lines is pivotal**. This can be achieved by including a **dedicated budget line to support the involvement of industrial actors in these projects**.

Tailored support to smaller players, in the form of **pilot line vouchers and budget lines for SMEs, start-ups and scale-ups in research pilot lines**, is also essential to achieve the development of parallel enabling technologies and products on which advanced pilot line technologies will rely (Ex. Pilot line vouchers, R&D vouchers, specific budget line in pilot lines for SMEs, startups and scaleups).

In addition, the current “research” pilot lines can be complemented with industrialisation pilot lines where necessary. These pilot lines should group industrialisation projects from companies of varying sizes (Large firms, SMEs and startups) for the prototyping, development and industrialisation of the most strategic Chips Act R&D projects, while pooling and ultimately reducing related costs.

To better connect Pillar I and Pillar II, a **preferential access to “First-of-a-Kind” state aid can be provided** to industrial investment projects across the semiconductor ecosystem that are linked to research pilot lines³.

In this context, SEMI Europe recognises the strategic potential of Important Projects of Common European Interest (IPCEI) in strengthening the ecosystem, **provided that the framework is simplified** to reduce administrative timelines and accelerate market uptake. IPCEIs should extend beyond traditional R&D and focus on strengthening EU critical capacities across the semiconductor value chain. By streamlining procedures, establishing predictable timelines kept to the minimum and securing the foundational supply chain, IPCEIs could more effectively bridge the gap between innovation and industrial deployment, ensuring timely impact for the European semiconductor industry. Nonetheless, SEMI Europe recognises that the IPCEI should remain a complementary tool in addition to the existing measures articulated under Pillar I and II of the Chips Act.

¹ Ex. Access to developed systems, product prototyping and development, co-development and qualification of process materials and specialty chemicals integration, and commercial viability.

² The general success rate of R&D in the semiconductor sector is 40%-60%. This rate will likely be lowered in the case of the Chips Act pilot lines, due to the low scale-up opportunities caused by the limited involvement of industry players.

³ So far, Chips Act provisions provide preferential access to research pilot lines only for companies benefiting from state aid under the Chips Act.

2. A “First-Of-A-Kind” for the Value Chain




Expanding the scope of Pillar II to consolidate European capacities in chip design, materials, components and equipment, and enabling support for research and product development activities in these segments

At this point in time, Pillar II has played a role in strengthening the attractiveness of Europe’s semiconductor ecosystem, but additional measures remain necessary. Pillar II has exclusively enabled investments towards front-end and back-end manufacturers⁴ and **has not resulted in support for other segments of the semiconductor supply chain** (i.e. design⁵, materials⁶, components and equipment⁷, and related research and product development activities). These critical sectors supply capital products and solutions for chip production and **require a dedicated long-term commitment towards their consolidation**. This is necessary to secure product’s time-to-market transition, develop and maintain a critical mass of highly specialised engineers and technical knowledge not replicable through short-term training programs.

Accordingly, it is pivotal to refine the scope of the “First-Of-A-Kind” (FOAK) definition to **include the whole semiconductor supply chain**, including chip design and design tools, materials, components and semiconductor-related equipment as well as research and product development activities in these segments.

Changes to the FOAK definition must be reflected in other sections of Pillar II by creating new tailor-made categories entitled to the same benefits as the Open EU Foundry (OEF) and Integrated Production Facility (IPF) categories. Eligibility to the FOAK, IPF and OEF should be guaranteed for EU and non-EU headquartered companies based on tangible criteria, including operational footprint in Europe and effective contribution to European semiconductor supply chain capabilities.

These categories could be framed in the following ways:

-  **Design Centre of Excellence:** *Revision of Article 17 establishing a “Design Centre of Excellence” label based on the same criteria of IPF and OEF;*
-  **Strategic Supply Chain Facilities:** *Suppliers of critical materials (Ex. Specialty gases, ultra-high purity chemicals, advanced process materials including CMP slurries, photoresists, atomic layer deposition (ALD) precursors, and EUV-compatible chemistries, and critical raw materials inputs), advanced components (Ex. Photomasks, high-precision lenses and optical systems, raw wafers) and semiconductor-related equipment (Ex. Metrology and inspection systems, manufacturing test equipment, packaging equipment, and process control).*
-  **Product Development Facilities:** *Encourage ultra-rapid scale-up required to meet first-mover advantages for facilities dedicated to the development, engineering, and industrial maturation of semiconductor equipment, component or materials, which carry out activities relating to initial design and qualification, prototype development, process integration, operational testing and validation.*

⁴ SEMI Europe, Chips Act Report: 30 SEMI Recommendations for a Chips Act 2.0. [URL](#)

⁵ Chip capabilities are primarily determined during the design phase which generates substantial intellectual property and advances Europe’s capacities in strategic sectors, including AI, IoT, quantum computing, advanced automotive systems, or industrial automation.

⁶ Materials such as photoresist chemicals and specialty gases require exceptionally high purity levels and complex molecular formulations that are unique to the semiconductor industry. These materials are specifically engineered for particular stages and types of chip manufacturing, which significantly limits the availability of alternative suppliers in the event of a supply shortage.

⁷ Although semiconductor equipment is falling under the framework of the Chips Act, there has been a considerable lack of investment and public support for this segment. This is linked to the fact that the very definition strictly covers equipment that is “utilised in semiconductor manufacturing,” thereby reducing the scope of technologies that could be supported under Pillar II.

3. A Process-Efficient Chips Act 2.0

Pillar I - Bringing pragmatic and simplified mechanisms accounting for business realities

Under its simplification agenda, the European Commission intends to lighten the regulatory load for businesses and reduce administrative burden at the legislations' implementation phases⁸. Efforts to bring greater simplification and less burdensome administrative process must be stepped up with due **consideration of business realities**, and must sustain previous efforts of public authorities and semiconductor players to jointly develop swift procedures.

Setting **more appropriate administrative and reporting requirements adapted to the size and resources of companies** will be essential for the success of the pilot lines. This will require preserving the current framework of the Hosting Agreement and Joint Procurement Agreement, which were jointly developed by the European Commission and the RTOs to fit the specificities of the industry.

Pillar II – Binding timelines, harmonised and fast-tracked approval processes to improve EU's attractiveness for semiconductor investments

Besides the legal foundations, the processes required for the verification and attribution of the First-of-a-Kind (FOAK), Integrated Production Facility (IPF) and Open EU Foundry (OEF) **certification have often put significant time and resource constraints on companies**. Whereas application dossiers have overlapping information requirements, these processes are performed in parallel by different DGs of the European Commission. The **validation of the FOAK status and state aid provision takes 9-12 months**, while similar validation and related administrative processes often take approximately **6 months in the U.S. and China, and less than a month in South Korea and Taiwan**. The European Commission's delays in the FOAK and IPF/OEF validation are stacked on top of the national permitting processes and negotiations, which could also take up to several months⁹.

The right balance can be found between the European acquis and a simplification of Pillar II procedures. This can be achieved by establishing a **single point of contact (One-stop-shop)** within the European Commission. It will receive and horizontally dispatch applications for Pillar II certifications between DG CNECT and DG COMP, while **harmonising the administrative processes of the respective services**. A legally binding, **strictly defined timeline for the processing of the FOAK and OEF/IPF applications** must be adopted to provide greater predictability to businesses' long-term investment plans. Lastly, to continue attracting foreign investments, this One-stop-shop must be equally accessible to both EU and non-EU headquartered companies.

4. Cross-Policy Alignment

The European Chips Act is embedded in a broader policy ecosystem where complementary legislation can help shape a comprehensive European strategy based on market demand. An EU Technology Strategy is strongly needed to coherently connect the various initiatives and guarantee that they aim towards the same objectives.

Vertical Alignment – Policy foundations for semiconductor growth

⁸ European Commission, "A simpler and Faster Europe: Communication on Implementation and Simplification". [URL](#)

⁹ SEMI Europe, Chips Act Report: 30 SEMI Recommendations for a Chips Act 2.0. [URL](#)

Vertically, the Chips Act must be supported by a robust policy framework that guarantees a coherent **2028-2034 Multiannual Financial Framework (MFF) and European Competitiveness Fund (ECF) aligned with its ambitions** to create a seamless “**lab-to-fab-to-market**” pathway. Furthermore, a funding programme tailored to SMEs within the ECF should be created to provide equity-based financing, easier access to first-of-a-kind facilities, and simplified application procedures. Parallel simplification efforts pursued to harmonise Joint Undertakings (JU) under Horizon Europe must not dilute the existing Chips JU in a wider, inappropriate and overly streamlined structure that doesn’t **consider the specificities of the semiconductor industry**.

A **stable global trade environment and steady supply of critical minerals** are vital conditions for the good functioning of the entire semiconductor supply chain, especially for the supply of semiconductor materials and equipment. This must be achieved by further **aligning EU industrial and trade policies**, fostering a **predictable regulatory environment** and delivering a coherent, risk-based and harmonised EU economic security practice that safeguards strategic technologies and attracts high-value semiconductor investments.

Lastly, delivering a **fully functional Capital Market Union (CMU)** is equally important to strengthen Europe’s attractiveness and ease semiconductor investment, especially for start-ups and scale-ups, via harmonised, cross-border access to financing that complements traditional bank lending.

Horizontal Alignment – Generating chip demand via cross-industrial policy coordination

Horizontally, should the supply and demand of advanced semiconductor technologies not align, the European Chips Act funding will bring limited benefits to the EU. So far, the lack of market demand and the semiconductor talent gap are the primary concerns of semiconductor companies investing in Europe¹⁰.

The alignment and coordination necessary across various European industrial policies must be **set in the long-term timeframe and provide predictability to businesses**. It must **tackle potential overlaps between industrial policies**, which could cause inefficient money allocation, inadequate financing and additional administrative burdens. Policy coordination must take place at both the macro-policy level, connecting provisions of the Chips Act 2.0 with the corresponding policies on AI (Ex. Cloud and AI Development Act, AI Gigafactories), quantum, automotives, renewables and workforce development, and at the implementation phase of these policies. It must enhance collaboration between the various businesses populating these sectors, contributing to the creation of business cases, fostering innovation and supporting the industrial deployment of next-generation technologies.

Any demand-side measures (Ex. “Buy European”, “Made in EU”) must consider the specific global structure and dependencies in the semiconductor ecosystem, and the central role of international technological partnerships in ensuring European competitiveness. Such measures mustn’t contradict the Chips Act objectives to attract and stimulate investments in Europe. They must be structured around companies’ contribution to supply chain security and resilience and based on companies’ operational footprint in Europe.

Europe is facing a considerable workforce challenge as it will lack approximately 65,000 skilled workers by 2030¹¹. The Chips Act must align with parallel skill development initiatives, including international partnership, to increase and tailor training and reskilling capacities to most relevant microelectronics fields across all educational levels, guarantee an active involvement of the industry in educational programmes and attract talents from partner countries.

¹⁰ SEMI Europe, Chips Act Report: 30 SEMI Recommendations for a Chips Act 2.0. [URL](#)

¹¹ European Skills Academy, Skills Strategy 2025. [URL](#)

5. An Enhanced Policy Toolbox

Exploring and incentivising the use of complementary policy tools to attract and stimulate semiconductor investments in Europe

The **European Chips Act is directly competing with third countries' initiatives** also aiming to develop their semiconductor industry and further attract investments. With Chips Acts around the world often bringing a greater set of policy instruments, the EU must **explore new policy solutions** that could be implemented by the Member States across the Union.

Establishing an **overarching governance structure for the implementation of the Chips Act 2.0** is highly needed to strengthen industry representation within decision-making bodies and to consolidate existing platforms and initiatives (Ex. Industrial Alliance, ESB, and Chips JU) under a single, coordinated framework.

Targeted fiscal incentives (Ex. Tax credits) implemented within a harmonised EU framework and tailored to company size can reduce capital costs, attract investment, and foster innovation across Europe's semiconductor ecosystem.

Moreover, public-private and private **Semiconductor Consortia operating in Europe** must be further supported. They must draw on international best practices in public-private semiconductor co-investment, such as the European Semiconductor Manufacturing Company (ESMC) and RAPIDUS, to align public and private investments, pool expertise and de-risk innovation in critical semiconductor technologies.

These instruments can be performed while integrating the semiconductor **industry's specific water and energy needs into national strategies**. Such instruments must account for the distinct infrastructural needs of the upstream segments of the semiconductor supply chain, integrating fab manufacturing considerations in national planning frameworks. This approach will ultimately strengthen Europe's investment attractiveness, ensuring stable manufacturing and supporting industrial resilience.

6. A Consultative Policy-Making Grounded into Business Realities

Integrate a multi-level and systematic consultation process between the European Commission, Member States, via the European Semiconductor Board (ESB), and the semiconductor industry while safeguarding data confidentiality

It is essential to guarantee an effective and pragmatic decision making under Pillar III that is grounded into semiconductor business reality. Efforts pursued under Pillar III must primarily **strengthen collaboration** between the European Commission, Member States via the European Semiconductor Board (ESB) and the Industrial Alliance for Processors and Semiconductors. This consultation must be ensured between the entire semiconductor industry and the European Semiconductor Board (ESB) with which there has been negligible contact.

The European Commission has made **steady progress in establishing its strategic mapping and monitoring system**, including the development of early warning indicators. These efforts must guarantee that the **confidentiality of shared data** is safeguarded while guaranteeing the full coordination with, and consultation of the industry.

Contact persons

Stefano Ramundo Orlando
Manager Advocacy and Public Policy
sorlando@semi.org

Adrien Padovani
Senior Policy Coordinator (Industry, Research, International Projects)
apadovani@semi.org

SEMI Europe

Rue du Commerce 124, 1000 Brussels
EU Transparency Register : 597361847853-70
<http://www.semi.org/eu>