How 3D integration can enable heterogeneous integration of materials and technologies?

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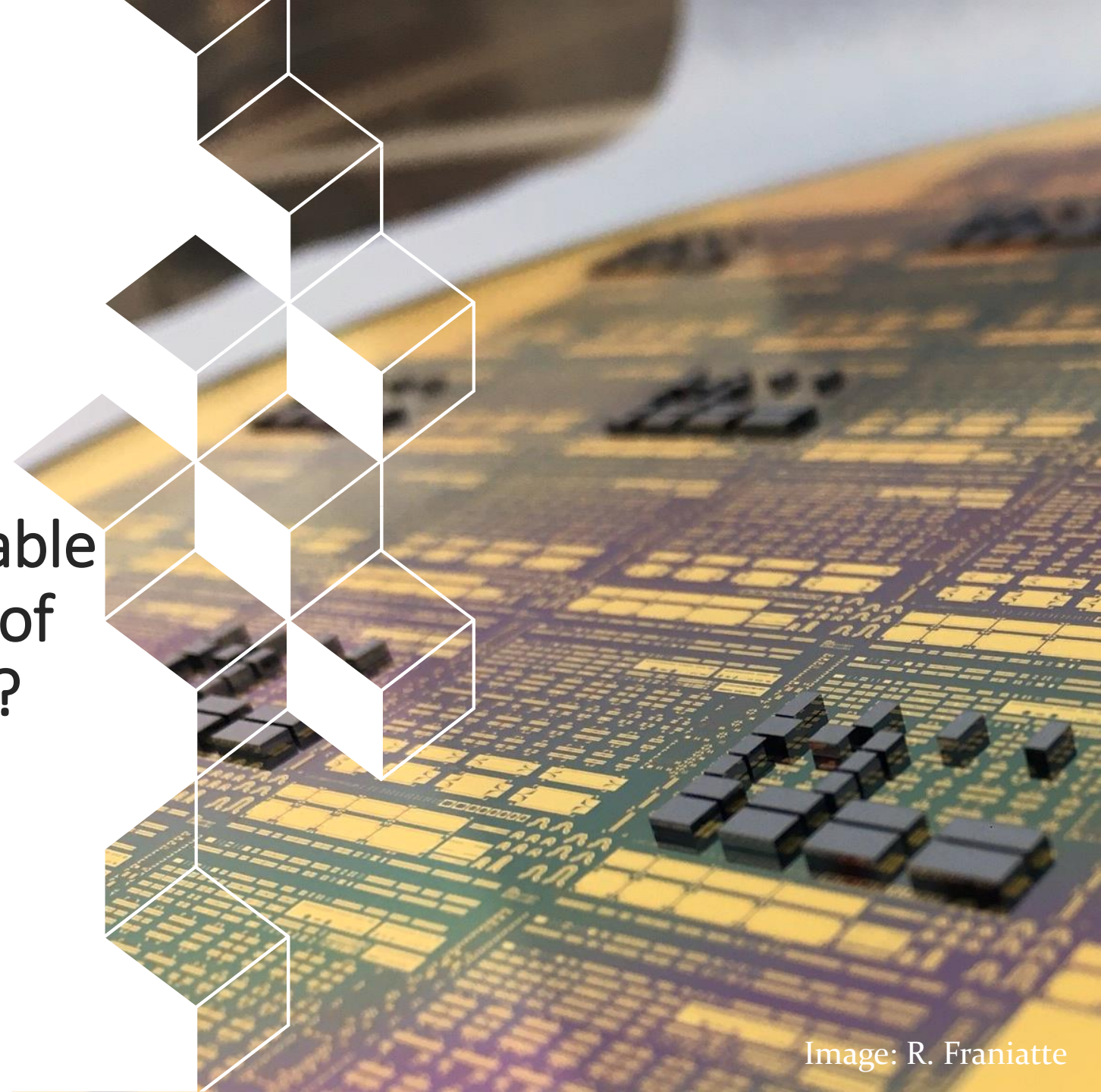

Image: R. Franiatte

Outline

- Context
- 3D Building Blocks for Heterogeneous Integration of Devices
- High Performance Material tiling for large diameter

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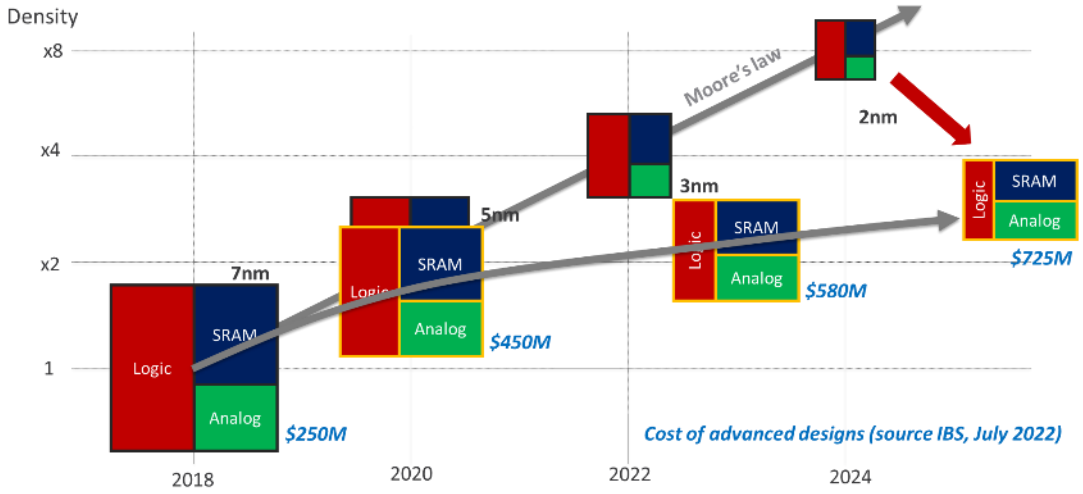
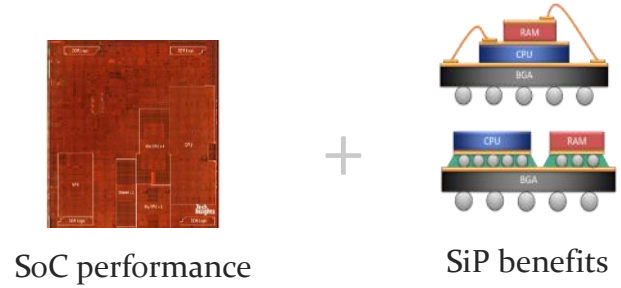
New paradigms are needed

- **Interconnects Bottleneck**
  - Dramatic R.C increase → strong impact on latencies
  - Gate delay << interconnects delay
- **Scaling becomes costly**
  - High development cost (mask, IP porting, verif…)
  - High manufacturing cost (low yield with large die)
- **Heterogeneous architectures needed**
  - More processing (AI, perception accelerators…)
  - More data to handle (memory capacity, fusion…)
  - Reuse of legacy (ISA, I/O interface…)
  - More modularity, scalability & sustainability



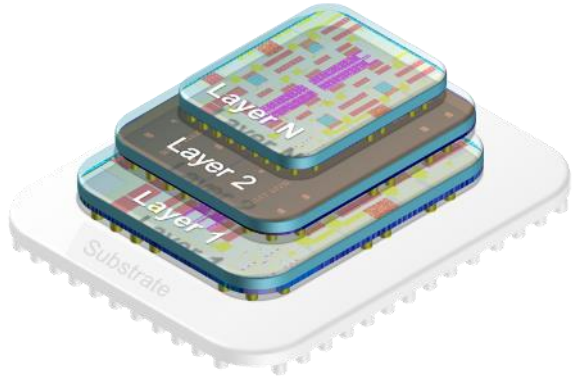
3D benefits for advanced systems

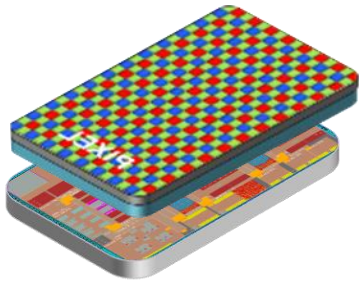
- **High-performance interconnections**
  - Low R, L, C → latencies, bandwidth, energy efficiency
  - Massively parallel processing with vertical links
- **Answers to modern design needs**
  - Reduced form factors, I/O number non limited by pad size
  - Partitioning, IP reuse, scalability & density
- **Heterogeneous integration**
  - Mixed CMOS nodes & materials (Si, III-V, II-VI, passives, MEMS)



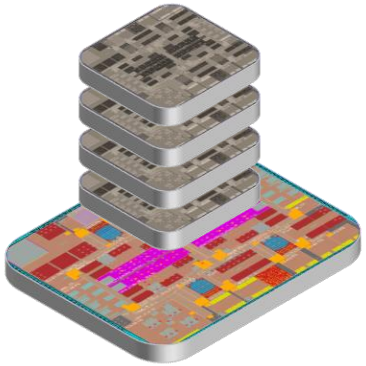
SoC performance

SiP benefits

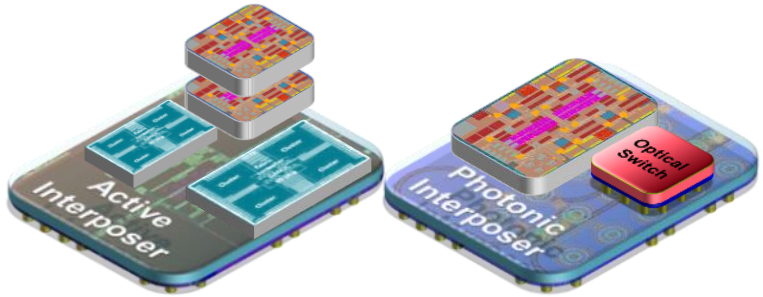




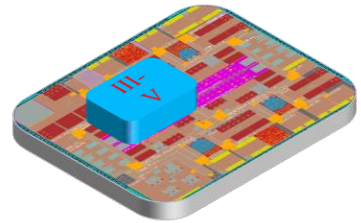
Sensor on logic



Memory on Logic



Chiplet-based integrations



III-V on Logic

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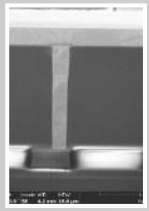
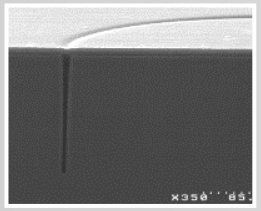
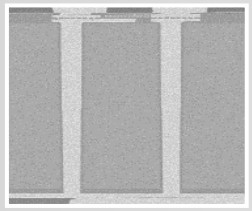
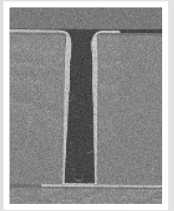
A complete tool box for 3D integration & packaging

TSV
Through Silicon vias

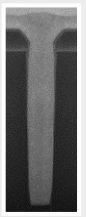

TSV HD Ø1x10µm


TSV / Trench first AR30

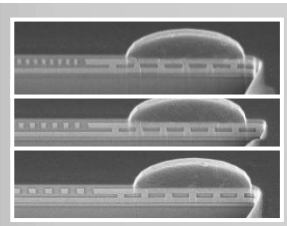

TSV mid AR10

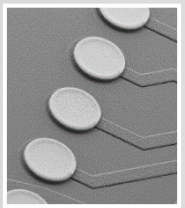

TSV last AR 0,5 → 5

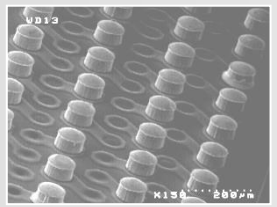

1x6 µm

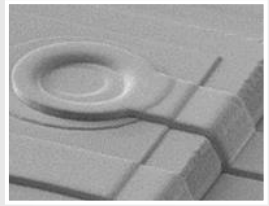

0.5x3 µm

Routing

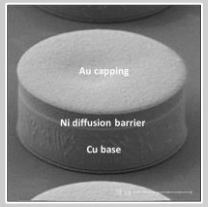

Front-side Cu damascene



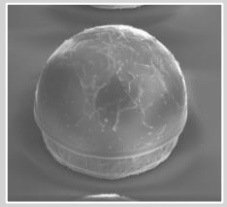

Back-side RDL co-integration (Pitch 20µm) with UBM & BUMP

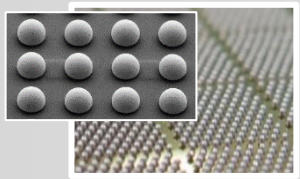

Cu conformal routing

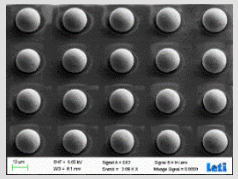
Connecting

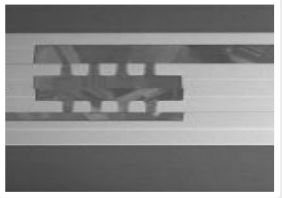


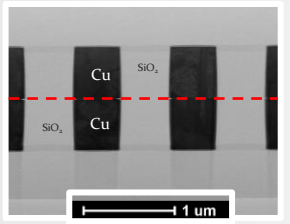
Copper pillars (Ø10µm)


Copper bumps (Ø10µm)


Bumping (Ø70µm) Balling (Ø300µm)

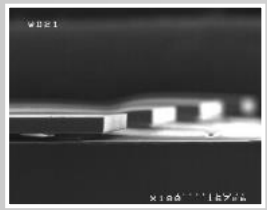

Bumping indium < 180°C & µTubes room T°C

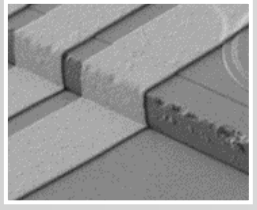

Direct /Hybrid bonding

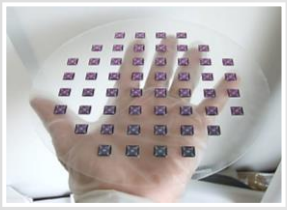


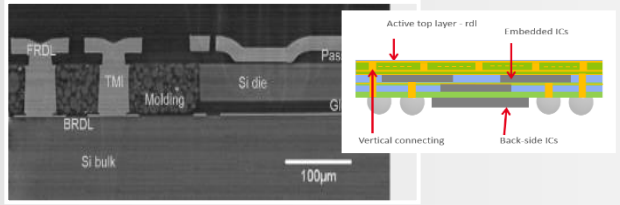
1µm Pitch

Rebuit Warp & thining




Si ultra thinning (20-30µm)



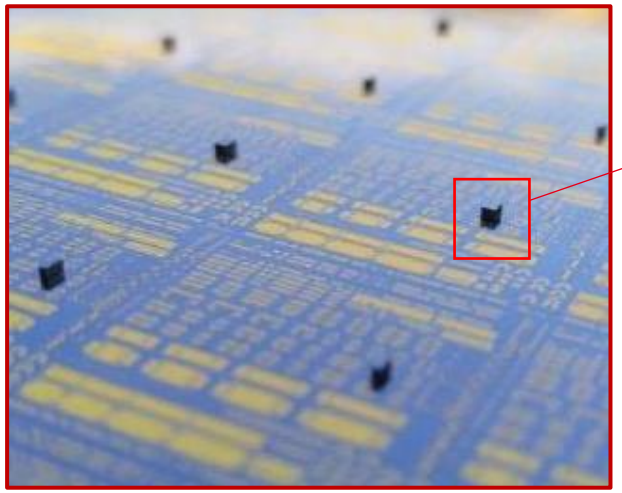


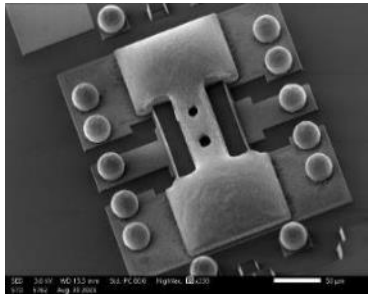
FO-WLP die first, RDL first, multi-strata, organic, silicon, glass substrates

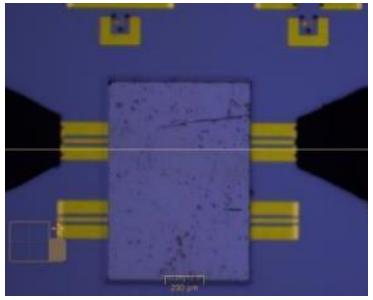
GaN HEMT on Si-CPW

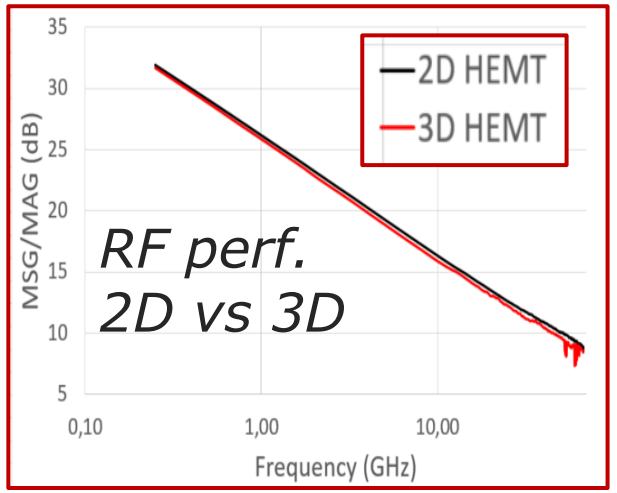
Concrete Heterogeneous 3D Assembly Results

Divay et al. VLSI'24



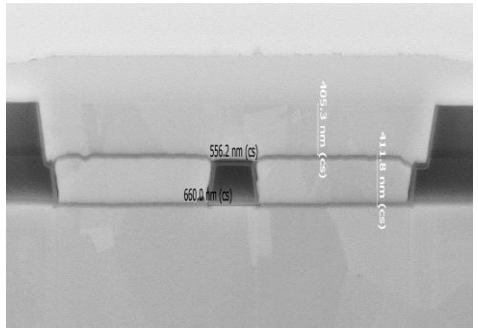


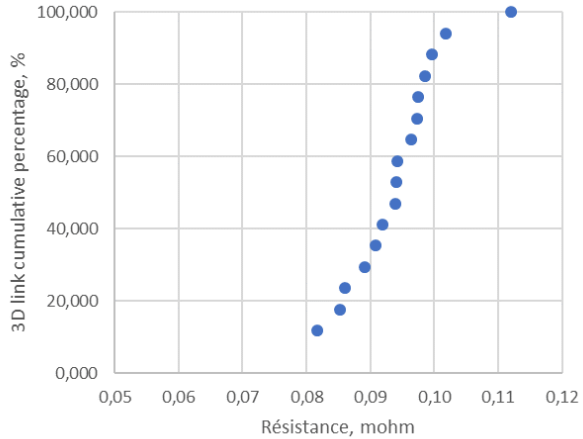




- **Assembly Yield >90%**
- **GaN HEMT functionality unaffected**
- **Negligible RF losses: < *0.5dB @ 40GHz***

Hybrid Bonding solution:

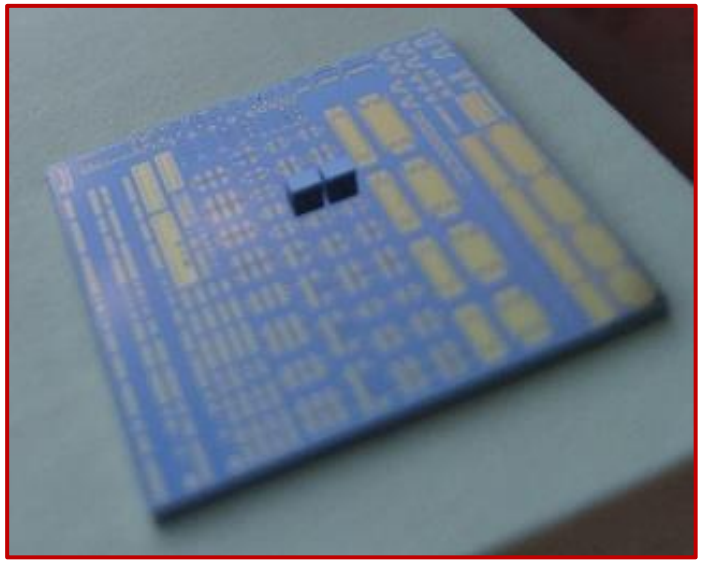


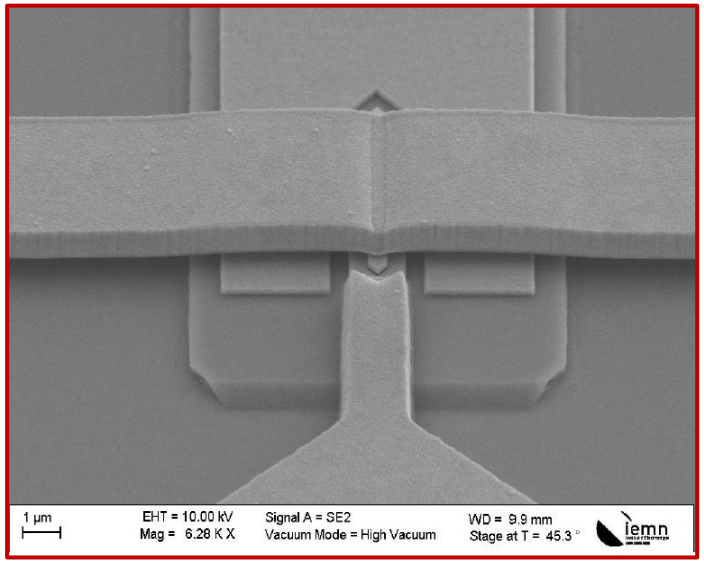


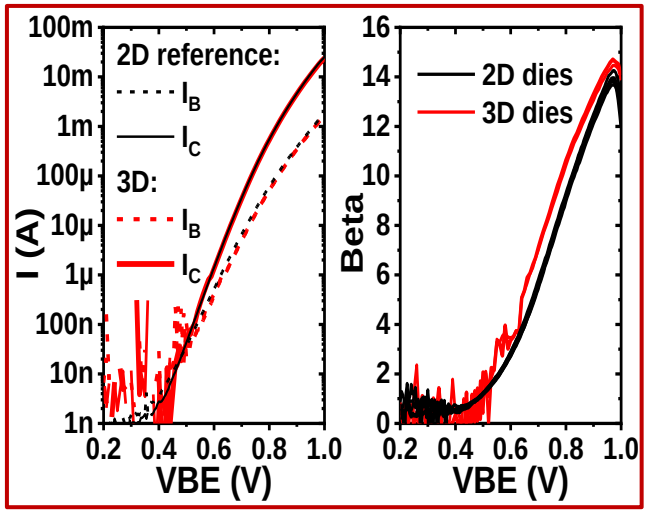
Concrete Heterogeneous 3D Assembly Results: InP HBT on Si

Oliveira et al. euMW'24

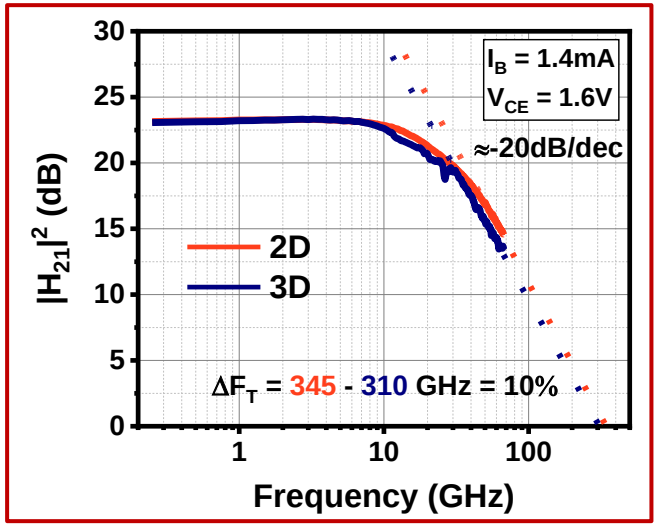
InP HBT provided by ***IEMN***







DC



RF

- **InP HBT functionality unaffected**
- **Limited Performance degradation:**

F_T decrease of 10% (345 to 310 GHz)

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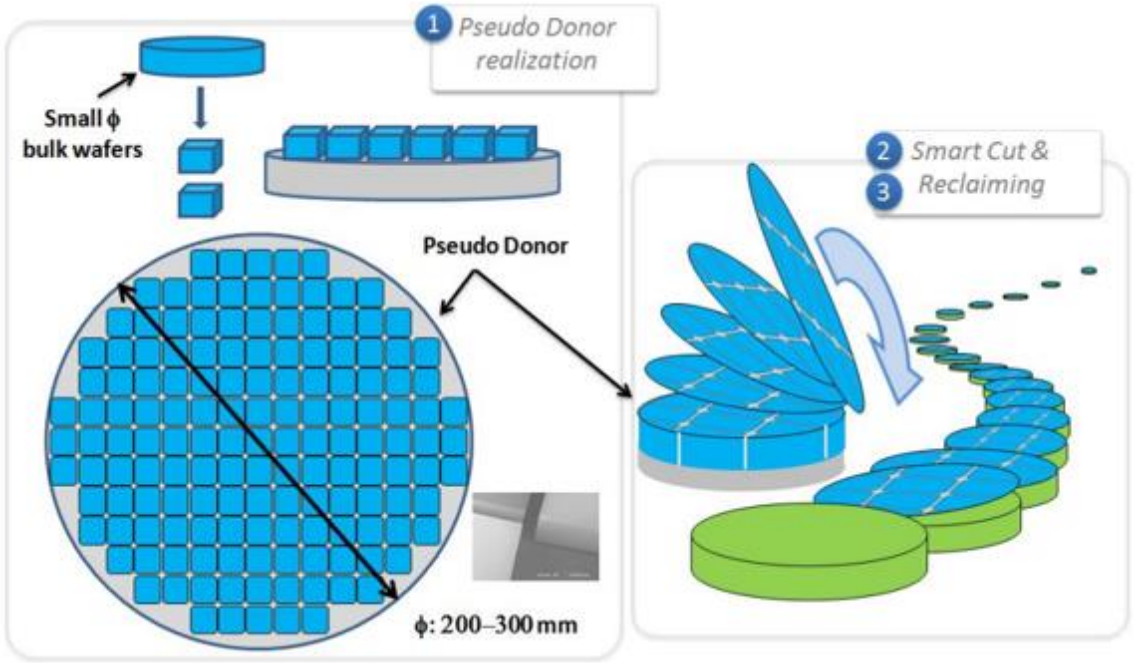
High Performance Material solution for 200-300mm

Three steps manufacturing process:

- Pseudo-donor created from a small-sized wafer with High Performance material (HPM). The wafers are diced and then bonded onto silicon.
- Pseudo-donor wafers enables the repeated transfer of a thin HPM film onto silicon, by Smart Cut™ from Soitec
- The reusability of the donor substrate for HPM saving



soitec

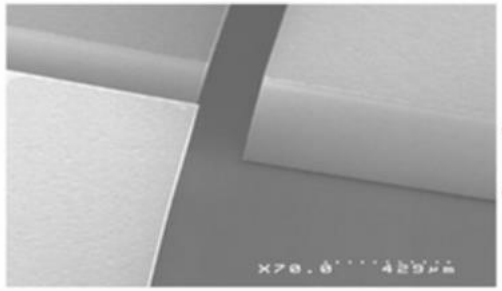
Advantages

- ❑ Pseudo-Donor wafer: from small HPM wafer
- ❑ Handle substrate: Silicon (Bulk or device wafer)
- ❑ Versatile die size and geometries
- ❑ Reuse of donor substrate

High Performance Material solution for 200-300mm

Example of layout of the tiles

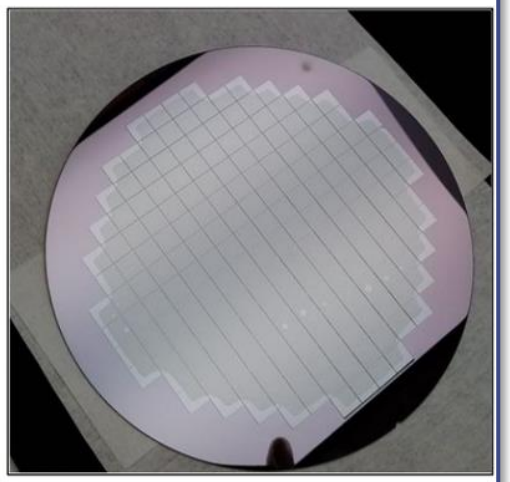
Pseudo Donor = 1x1cm² InP dies on 200 mm Si substrates



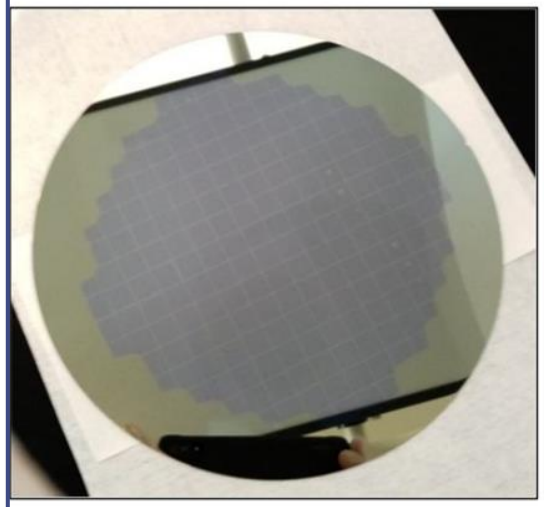
Made by tiling InP dies cut from small diameter (50-75-100 mm) Bulk InP substrates

Several hundreds µm
⇒ Many Smart Cut layers

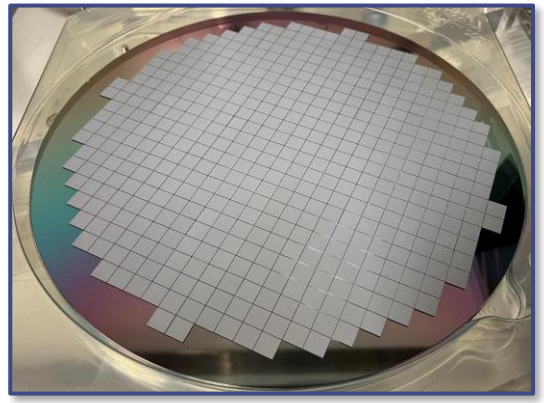
Pseudo-Donor (for reuse)



InPOSi 200 mm (Epi ready)



Path to 300mm substrate



- *B. Ghyselen, et al.,International Conference on Compound Semiconductor Manufacturing Technology, 2023*

Key Messages

- 3D integration and Bonding technologies are now used in High Volume Manufacturing
- Thanks to those technologies, material innovation is facilitated either through device co-integration or through blanket material transfer.
- III-V devices can thus be easily co-integrated with high performance CMOS tech.
- 200 & 300mm wafers can be reconstructed using thin III-V dies.
- This methodology can be applied to any other material (II-VI, diamond, 2D materials…)