soitec

OLIVIER BONNIN

Substrate engineering for the benefit of advanced devices and integration

SEMICON Europa 2025 - Materials Innovations | November, 2025

SEMICON Europa 2025 - Materials Innovations
November, 2025

OUTLINE

Anything-On-Anything for Engineered Substrates

SOI: Leveraging Best Silicon Expertise

PIEZO Materials

SiC and GaN

InP & 3D

INNOVATION AT SOITEC
250 SKILLED PEOPLE AND DYNAMIC IP FILING

>250
RESEARCHERS & INVENTORS

>25%
PhDs

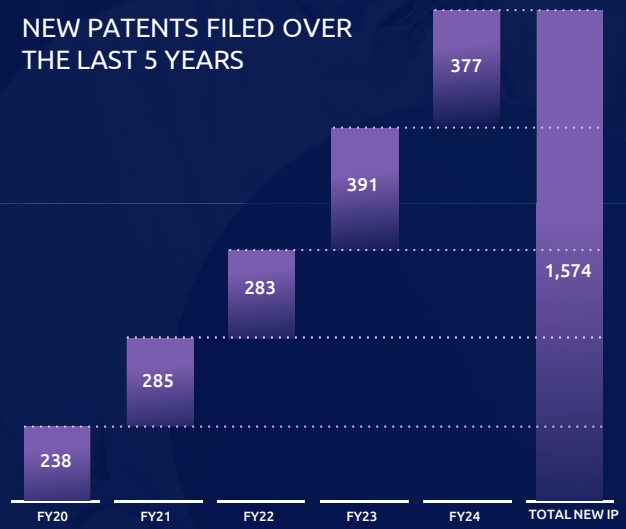
EXPANDING TEAM GLOBALLY

>14%
OF OUR REVENUE INVESTED IN INNOVATION IN FY24 (1)

>4,150
PATENT PORTFOLIO, WITH 377 NEW PATENTS IN FY24

(1) Before capitalization

NEW PATENTS FILED OVER THE LAST 5 YEARS



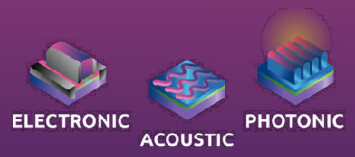
INPI 2023
TOP FRENCH PATENT APPLICANTS

#1
MID-SIZE COMPANY

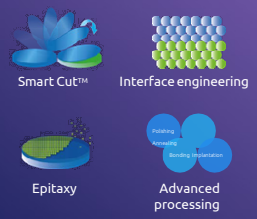
#25
IN THE GLOBAL RANKING

LEVERAGING MATERIALS SCIENCES TO ENABLE UNIQUE APPLICATIONS

Leverage
MATERIALS INTRINSIC PROPERTIES

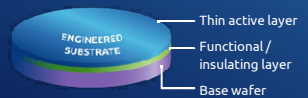


Develop
TECHNOLOGY SOLUTIONS



Design
ENGINEERED SUBSTRATES

- SOI product portfolio
- Anything-on-Anything (active layer on substrate)

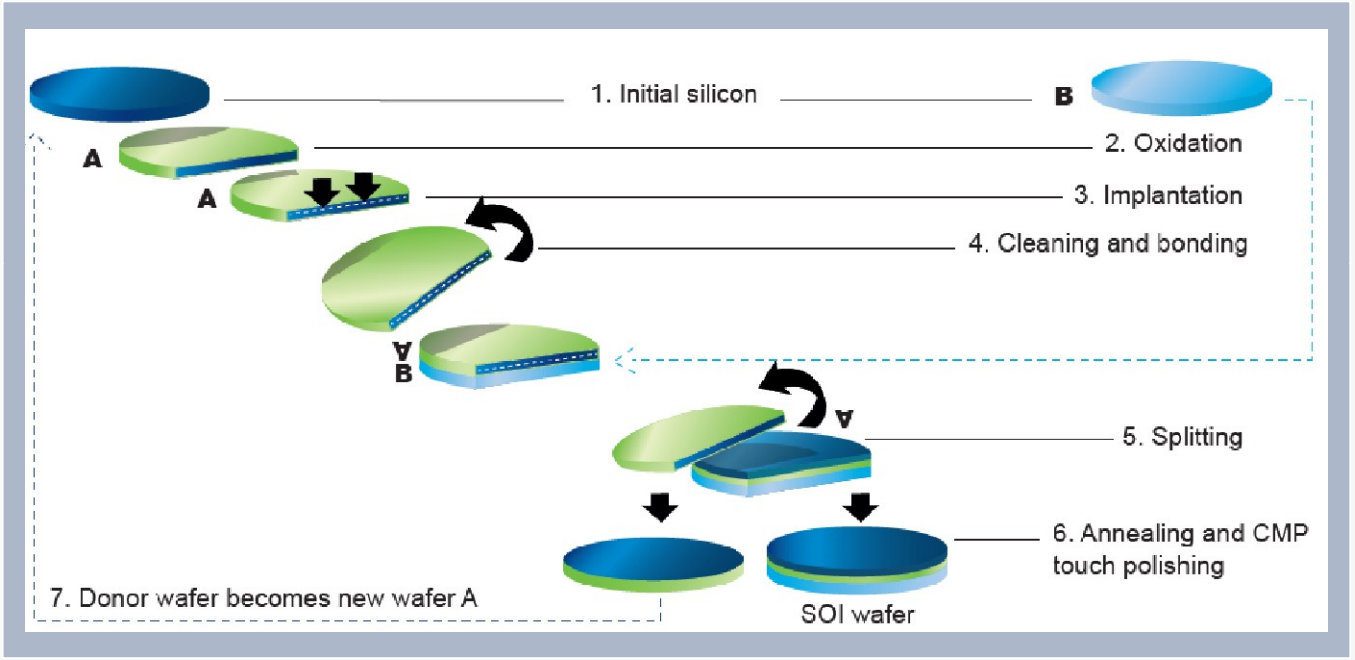


Enable
NEW PROPERTIES, ENHANCED PERFORMANCE, IMPROVED ENERGY CONSUMPTION

- Connectivity
- Low-power computing
- Energy efficiency
- Electric vehicles
- Quantum computing
- 3D integration
- Data rate & bandwidth

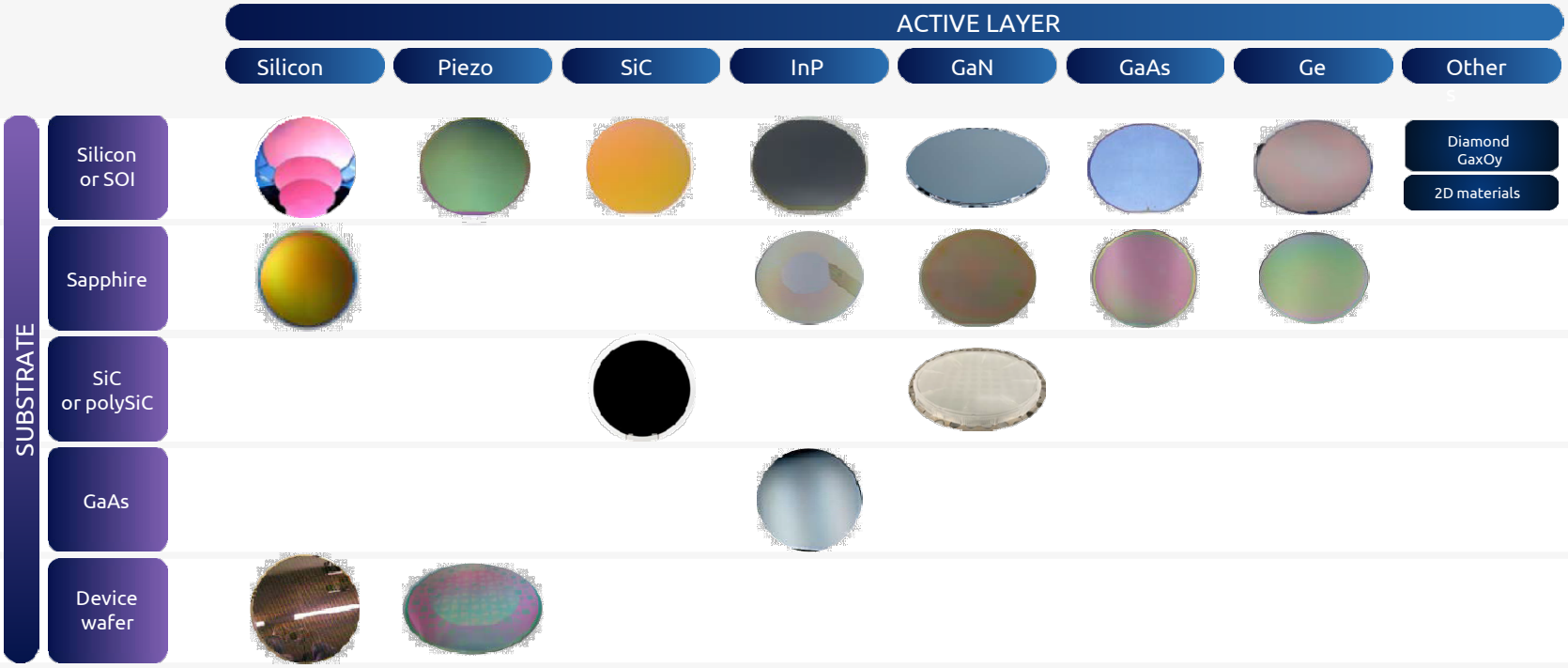
REVOLUTIONARY SMART CUT™

- Industrial Maturity (25+ years)
- Uniformity and Layer Integrity
- Sustainability with Donor Refreshing
- Flexibility of Material Integration



ANYTHING-ON-ANYTHING - SOITEC INNOVATION DNA

BEST ACTIVE LAYER(S) ON FUNCTIONAL SUBSTRATE



OUTLINE

Anything-On-Anything for Engineered Substrates Menu

SOI: Leveraging Best Silicon Expertise

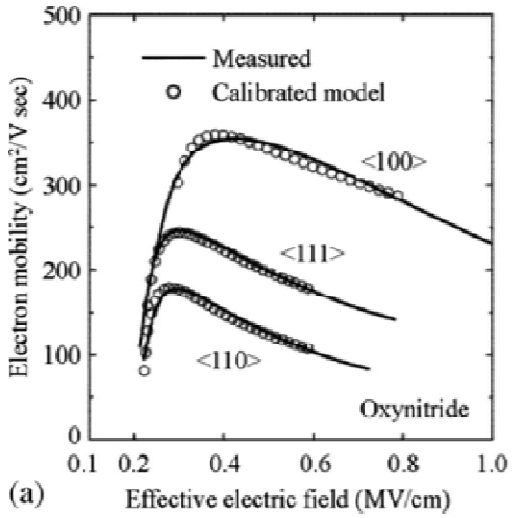
PIEZO Materials

SiC and GaN

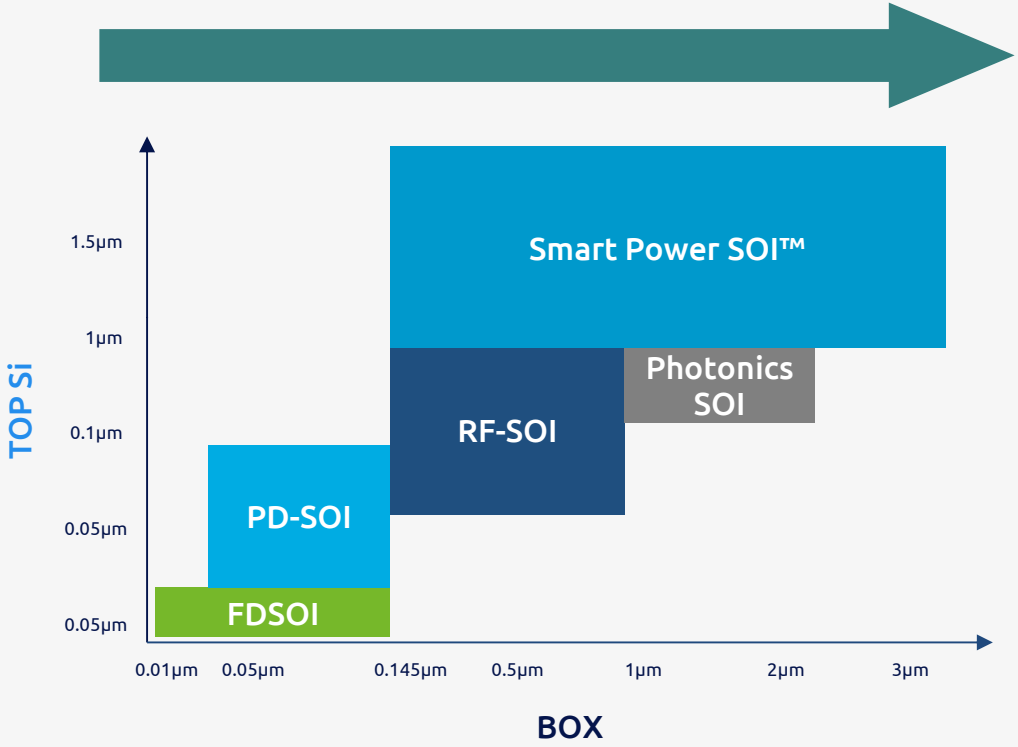
InP & 3D

SMART CUT™ VERSATILITY

Silicon On Insulator



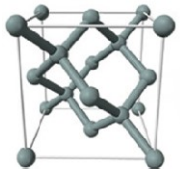
THICKNESS CAPABILITIES



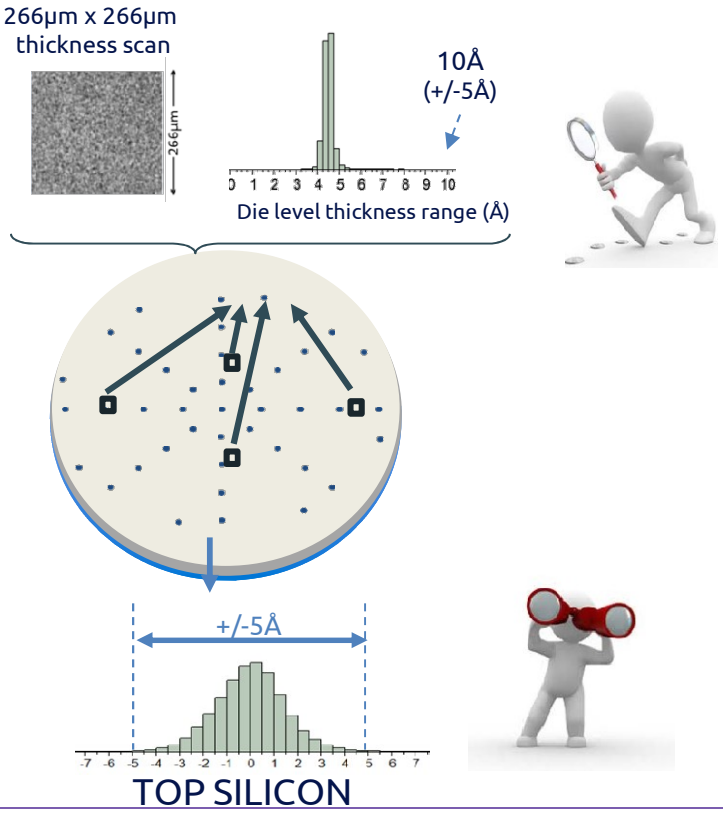
FD-SOI: THICKNESS CONTROL AT ATOMIC LEVEL… IN HVM

Millions wafers controlled at atomic level, all points, all wafers

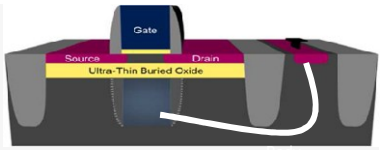
±5 Å



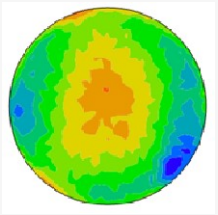
Mature process and yield in HVM

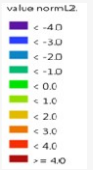


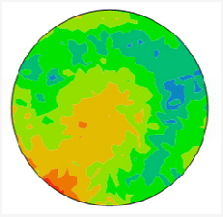
SOI THICKNESS UNIFORMITY

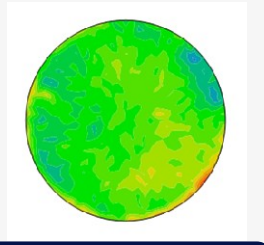


	F5X 41 pts All points all wafers dispersion	*F5X 41 pts* Mean Wafer dispersion	*F5X 625pts*
PROCESS GENERATION 1	σ = 1.5Å	σ = 0.65Å 50Kw	
PROCESS GENERATION 2	σ = 1.3Å	σ = 0.42Å 24Kw	
PROCESS GENERATION 3	σ = 1Å	σ = 0.36Å 18kw	





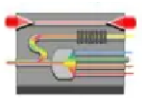




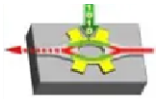
Soitec etch wafer specifically to ensure very tight thickness distribution around target: reaching now 1σ=0.32%

PHOTONICS-SOI SUBSTRATES
MATERIAL ENHANCEMENT BASED UNIVERSAL PLATFORM FOR OPTICAL ENGINE

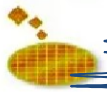
TOP SI THICKNESS CONTROL



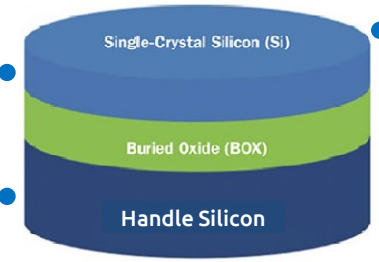
Passive Circuits
Improved Loss / Xtalk



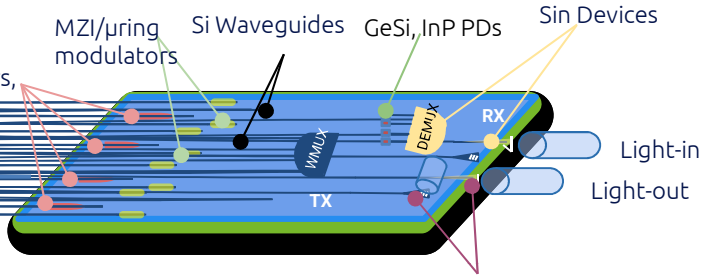
Modulators
E/O BW



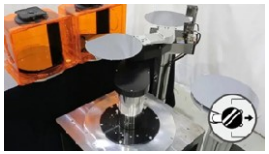
Manufacturing
Yield



Photonics-SOI

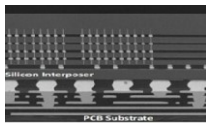


MECHANICAL STABILITY

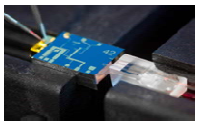


Wafer Handling

LOW BMD DENSITY

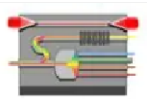


TSV Driver
Integration

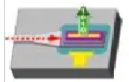


Chip-to-Fiber
Attach

TOP SI ROUGHNESS



Waveguide
Loss



Ge Photodiodes
Responsivity

BMD: Bulk Micro Defects
TSV: Through-Silicon Bias

OUTLINE

Anything-On-Anything for Engineered Substrates Menu

SOI: Leveraging Best Silicon Expertise

PIEZO Materials

SiC and GaN

InP & 3D

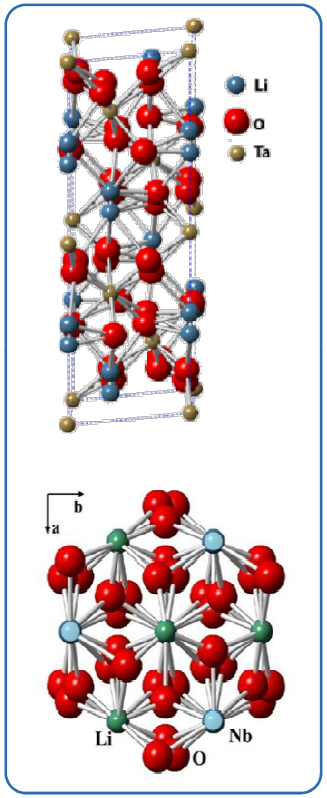
PIEZOELECTRIC MATERIALS

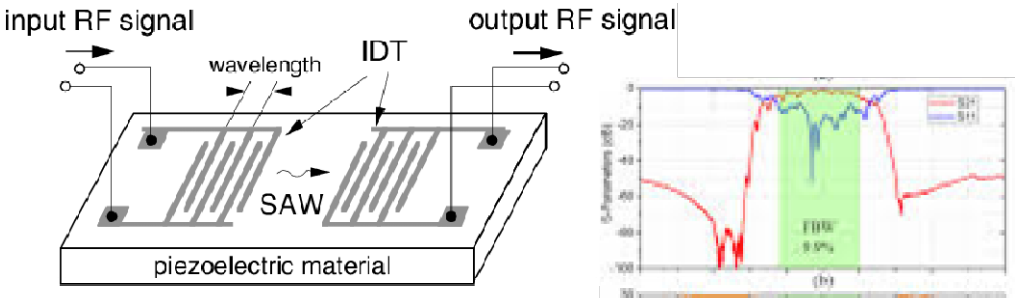
Cost
Fragility

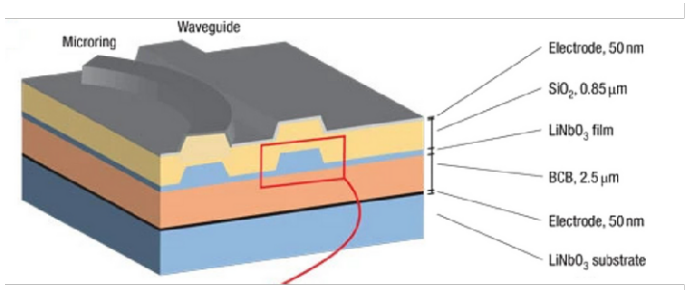
Low Acoustic Loss
Thermal Stability
Piezo Properties

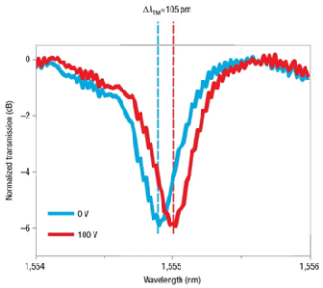
Cost
Brittleness
Lower Th Stability

High Non Linear Optical Coeff
Wide Transparency Range
Electro-optics Properties







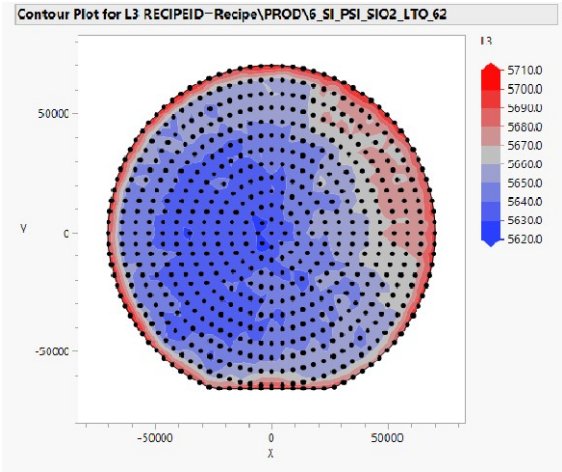


SMART CUT™ POI : LiTaO3 TRANSFER AND THICKNESS

150mm POI substrate

✔ VERY HIGH FULL WAFER LITAO3 FILM TRANSFER QUALITY

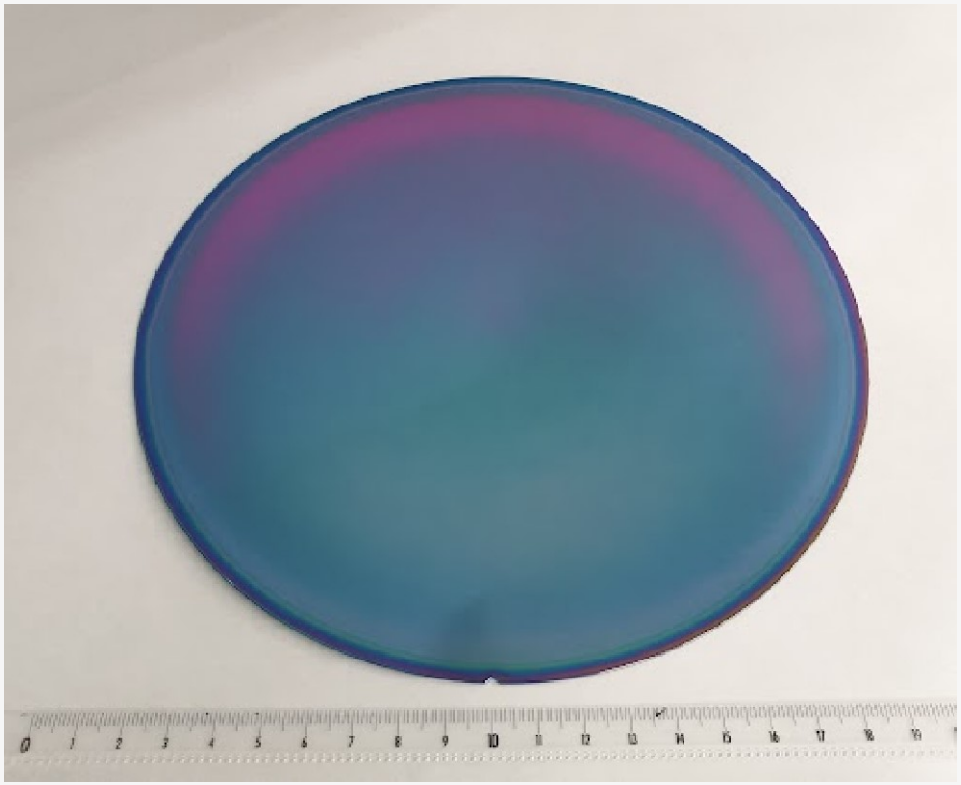
LiTaO3 LAYER THICKNESS MAPPING (nm)
565 nm LiTaO3 film target



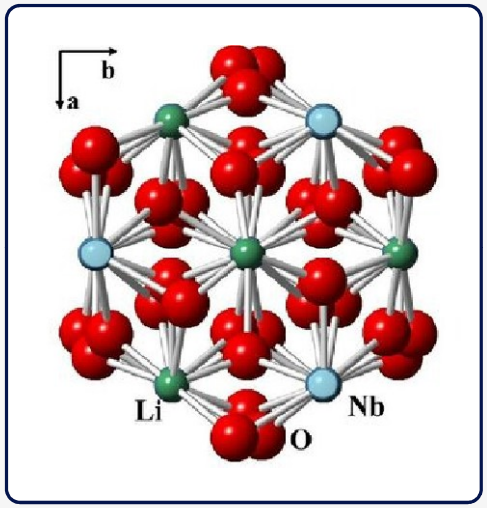
LT Thickness range = **9 nm**
NU% = (max-min) / (2.average) **~1 %**

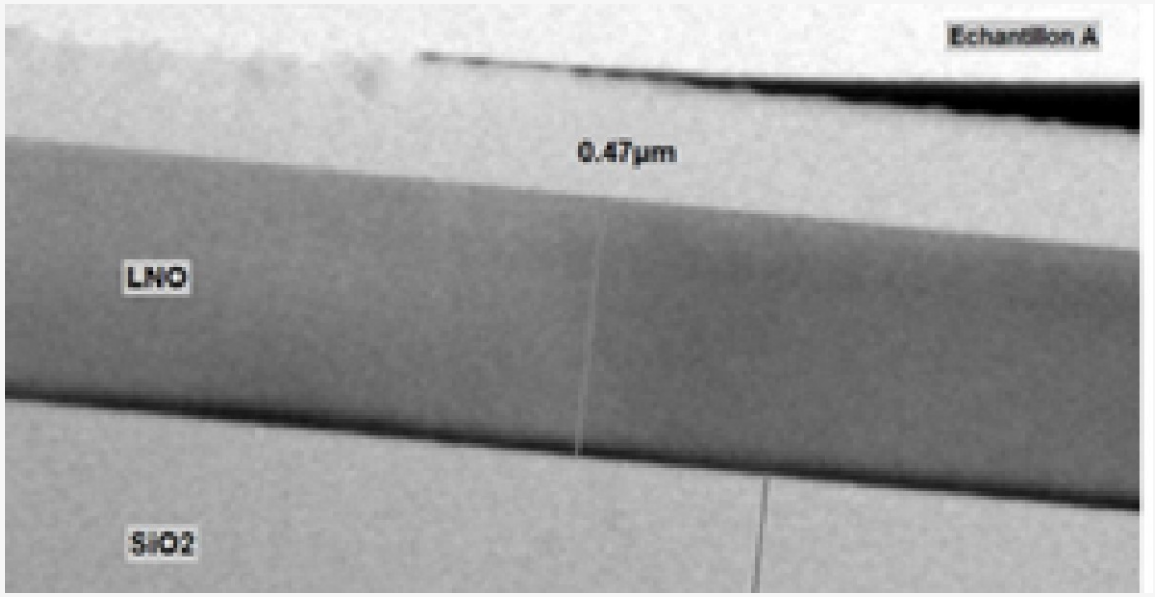
✔ TIGHT LITAO3 THICKNESS UNIFORMITY ACHIEVED

SMART CUT™ 200MM PIEZO ON INSULATOR TECHNOLOGY



PUSHING THE LIMITS OF LT BONDING FOR SMART CUT™





LiNbO3: CTE=16.7 on Silicon: CTE=4.2

OUTLINE

Anything-On-Anything for Engineered Substrates Menu

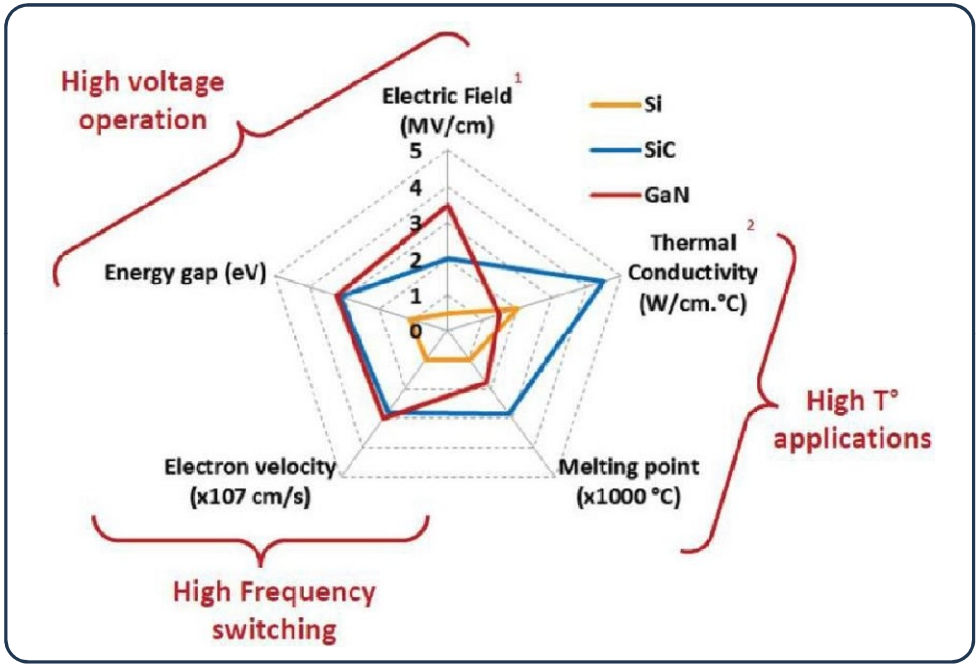
SOI: Leveraging Best Silicon Expertise

PIEZO Materials

SiC and GaN

InP & 3D

MATERIALS FOR POWER DEVICES… AND MORE

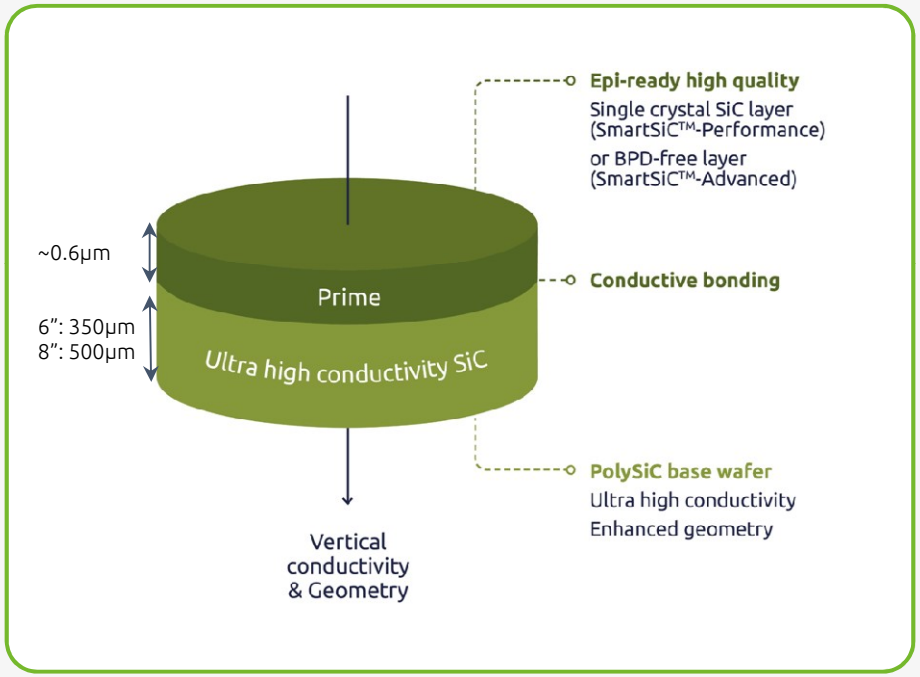


Cost & die cost
Doping/defect
Cash intensity

Energy efficiency
Low loss switching
Thermal conductivity

Janczyk, Grzegorz & Sitnik, Adam & Messina, Angelo. (2019). The “First and European SiC eigth inches pilot line" - REACTION Project as a Driver for Key European SiC Technologies focused on Power Electronics Development.

SMARTSIC™ REQUIRES A NEW CONDUCTIVE BONDING
ENGINEERED SUBSTRATES FOR POWER APPLICATIONS



The SmartSiC™ PROCESS

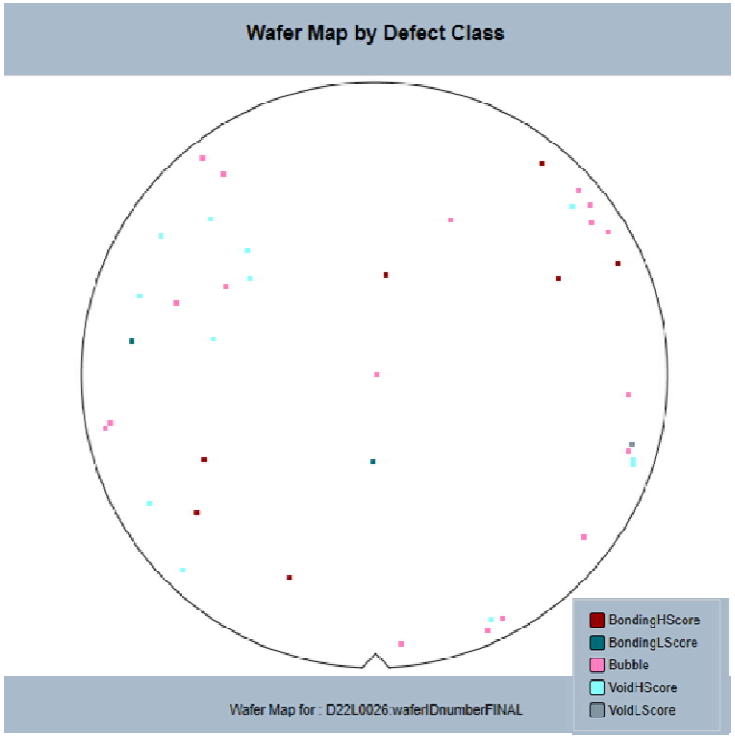
1. Ion implantation of SiC wafer

2. Bonding on handle substrate

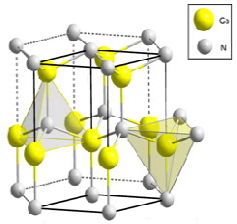
3. Layer transfer

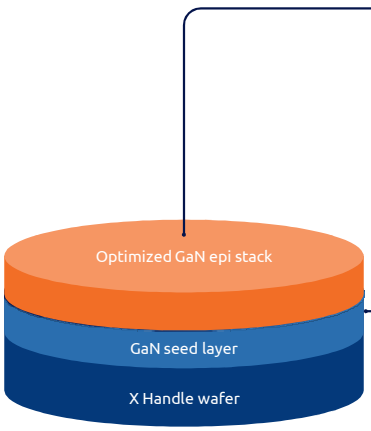
(1) Rouchier, Séverin, et al. "150 mm SiC engineered substrates for high-voltage power devices." *Materials Science Forum*. Vol. 1062. Trans Tech Publications Ltd, 2022.

AN SOI LOOK… BUT IN SILICON CARBIDE



SMARTGaN
BEST OF GaN FOR FUTURE RF & POWER DEVICES





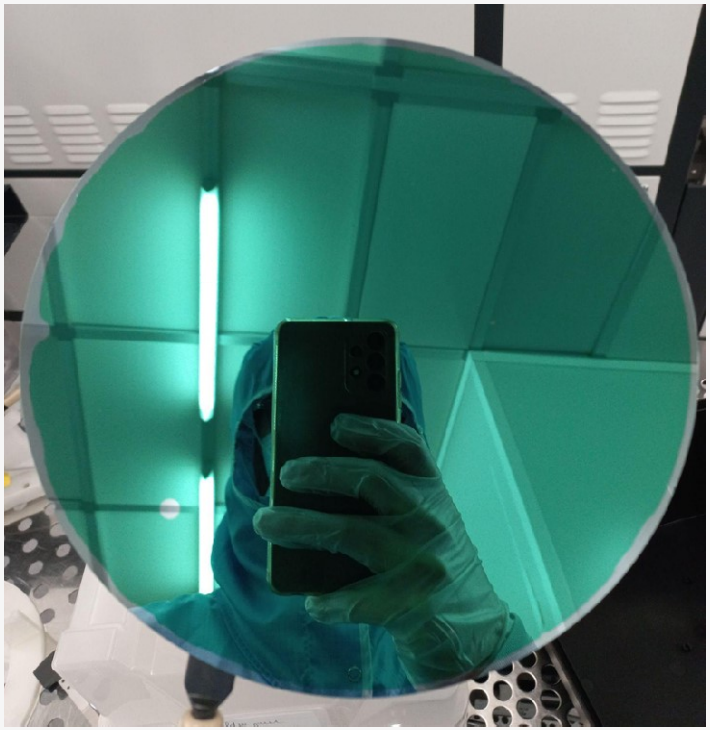
OPTIMIZED GaN EPI STACK
- For lateral HEMT devices (RF or Power)
- For vertical Power devices

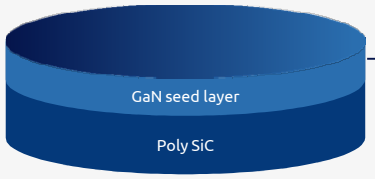
GaN SEED LAYER
- Buffer-free GaN
- Epi ready (homoepitaxy)
- Fabricated using layer transfer technology

BONDING INTERFACE
- Customized per application (electrical isolation or conductive)

X HANDLE WAFER
- Customized per application (silicon or non-silicon options)
- Thermally conductive material
- 200mm wafer size, compatible with CMOS fab
- Cost effective (scalable to very large volumes)

200mm SMARTGaN
BEST OF GaN FOR FUTURE RF & POWER DEVICES





GaN SEED LAYER
- Buffer-free GaN
- Epi ready (homoepitaxy)
- Fabricated using layer transfer technology

Conductive BONDING INTERFACE

pSiC Substrate
- Thermally conductive material
- 200mm wafer size, 300mm compatible
- Cost effective (scalable to very large volumes)

OUTLINE

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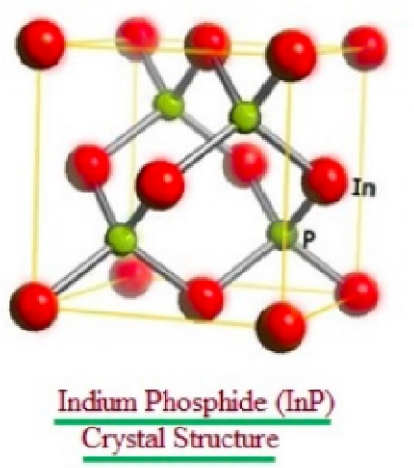
InP & 3D

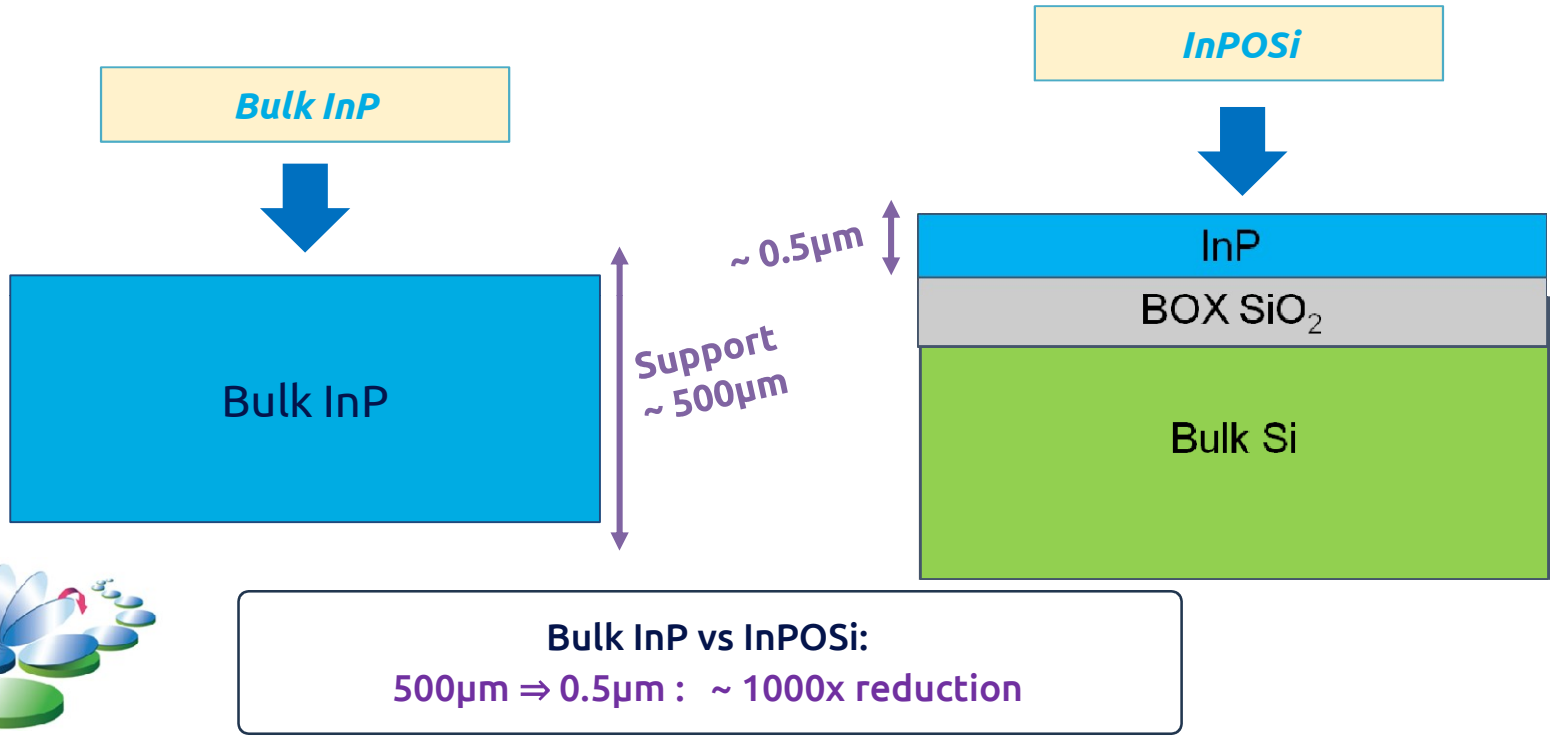
InP MATERIAL KEY ELEMENTS



High cost
Fragility
Limited wafer size
Complex fabrication
Toxicity concerns

High electron mobility
Superior Bandgap
High thermal conductivity
Low noise performance
Matching with optical com

FROM BULK InP TO InPOSi:
STRONG "INP" CONTENT REDUCTION



Bulk InP vs InPOSi:
500µm ⇒ 0.5µm : ~ 1000x reduction

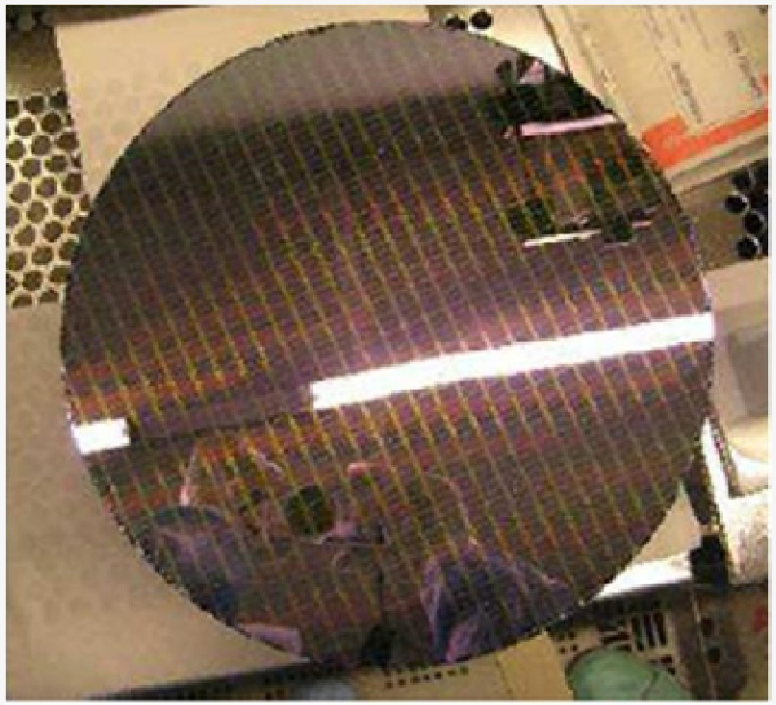
PUSHING THE LIMITS OF LT BONDING FOR 3D DEVICE DEMONSTRATION

SILICON LAYER STACKING FOR SEQUENTIAL 3D

	TECHNOLOGY CONCERNS	VALIDATION
1	Low temperature splitting	√
2	Low temperature bonding	√
3	Surface topology/voids	√
4	Si film uniformity and surface quality	√
5	Electrical properties	√
6	Si film quality and integrity	√

300mm Smart Cut™ onto a DRAM wafer - (process <500°C)

I. Radu et al., ICICDT, 2015



KEY MESSAGES

WE CAN INTEGRATE MOST ACTIVE LAYERS IN OUR ENGINEERED SUBSTRATES

PPACTG DRIVEN

LOW TEMPERATURE BONDING IS SUPPORTING NEW INTEGRATIONS

SEMICON Europa 2025 - Materials Innovations

THANK YOU