



Enhancing Sustainability in Semiconductor Manufacturing: Energy-Efficient Optical Crosslinking for Lithography Processes

Innovation for a Sustainable World

SCREEN Semiconductor Solutions Co., Ltd.

November 20, 2025

The names of company or products or services, etc. on this document are the trademarks or registered trademarks of their respective companies.

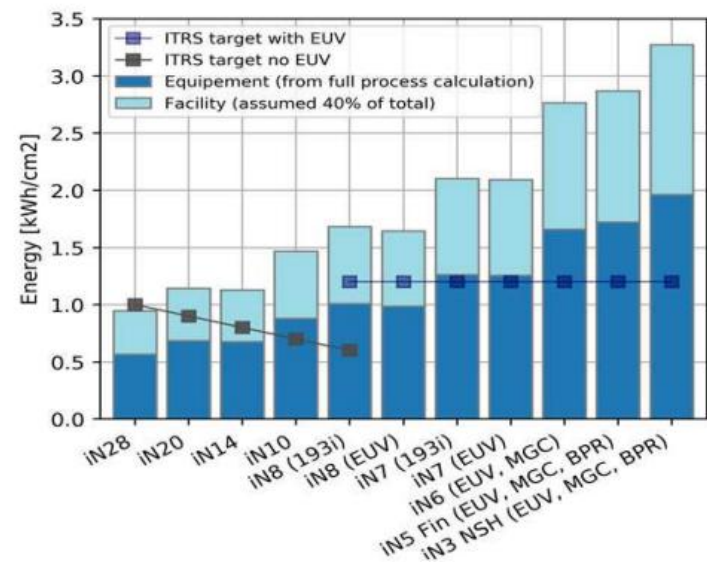
Although "TM" and "®" may not be specified in this document, it is prohibited by the Trademark Law, etc. to use them without the permission of each right holder.

本資料に記載の会社名、製品名、サービス名等は、各社の商標または登録商標です。

本資料上では「TM」「®」を明記していない場合もありますが、これらを各権利者の許諾なしに使用等することは、商標法等で禁止されています。

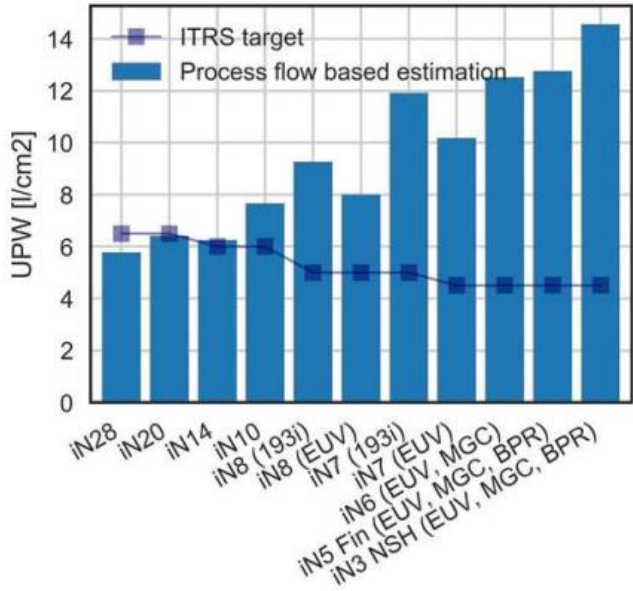
Process miniaturization has great environmental impact

Energy



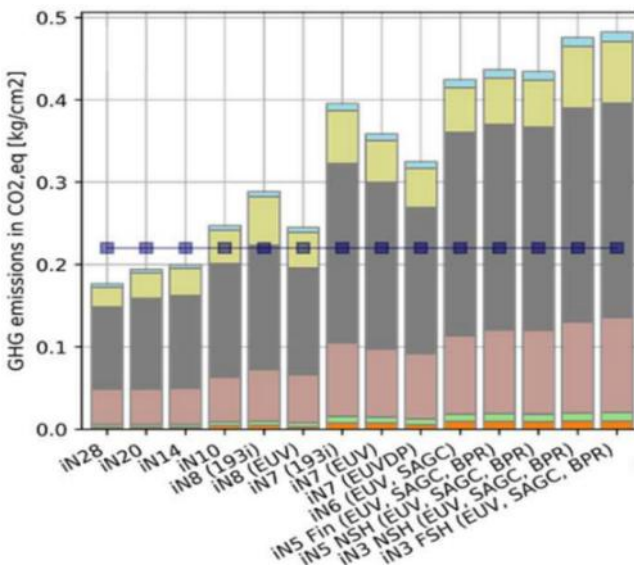
Total manufacturing electricity per cm² for full process flows (300mm wafer = 706cm²). Facility energy is projected assuming 40% of the total energy.

UPW



Total Ultra Pure Water (UPW) usage in liters per cm² for full process flows from iN28 to iN3 for 300mm wafer equivalent.
ITRS guidelines shown as reference.

CO₂



GHG emissions in kg CO_{2,eq} per cm² of wafer, per node, calculated using the GHG protocol for electronics industry of IPPC.

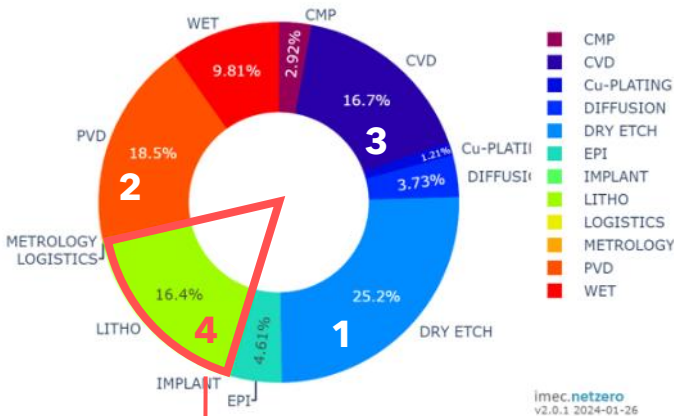
Sustainable scaling of chip manufacturing is a major industry challenge

L.-Å. Ragnarsson et al., "Environmental Impact of CMOS Logic Technologies", 2022 6th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Oita, Japan, 2022, pp. 82-84)
M. Garcia Bardon et al., "DTCO including Sustainability: Power-performance-area-cost-environmental score (PPACE) analysis for logic technologies", Technical Digest - International Electron Devices Meeting (IEDM) 2020-Decem, 41.4.1-41.4.4

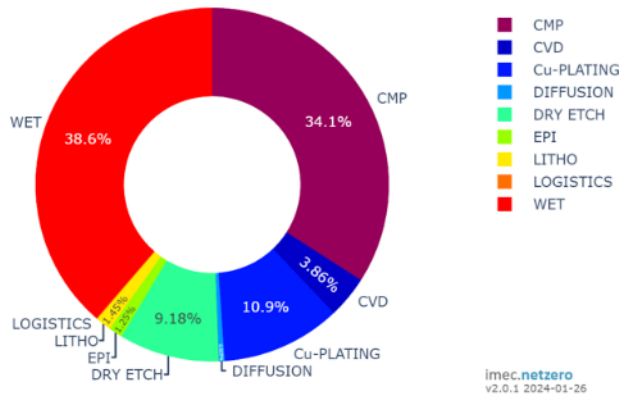
High impact problems in semiconductor manufacturing

N5

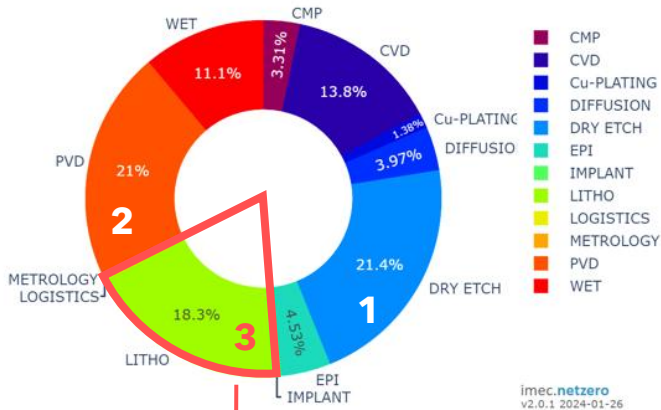
Scope 1 + 2 total emissions



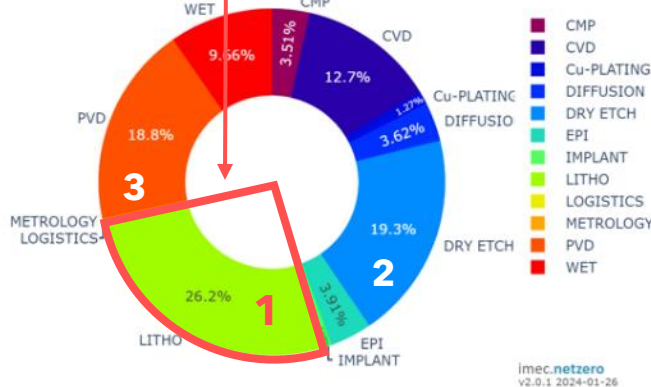
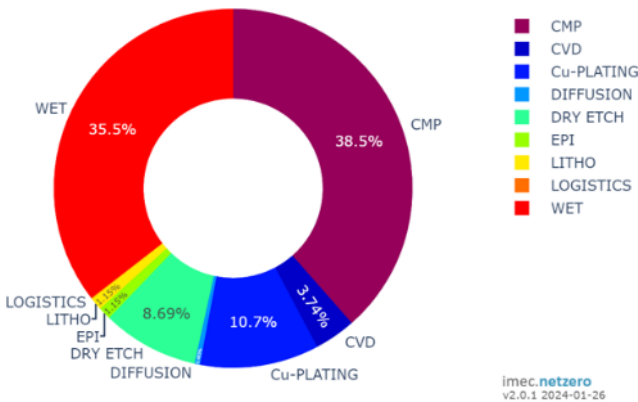
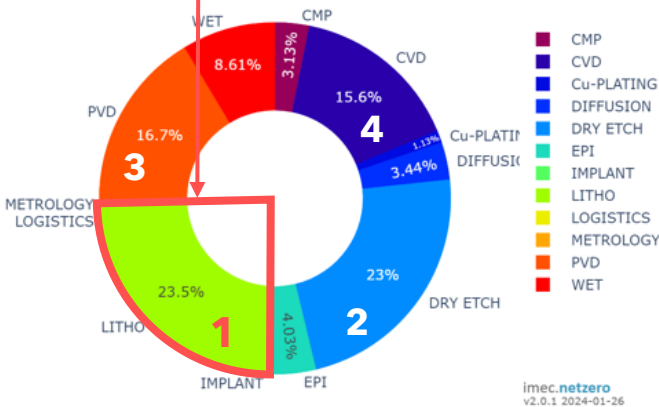
UPW usage



Full electric energy consumption

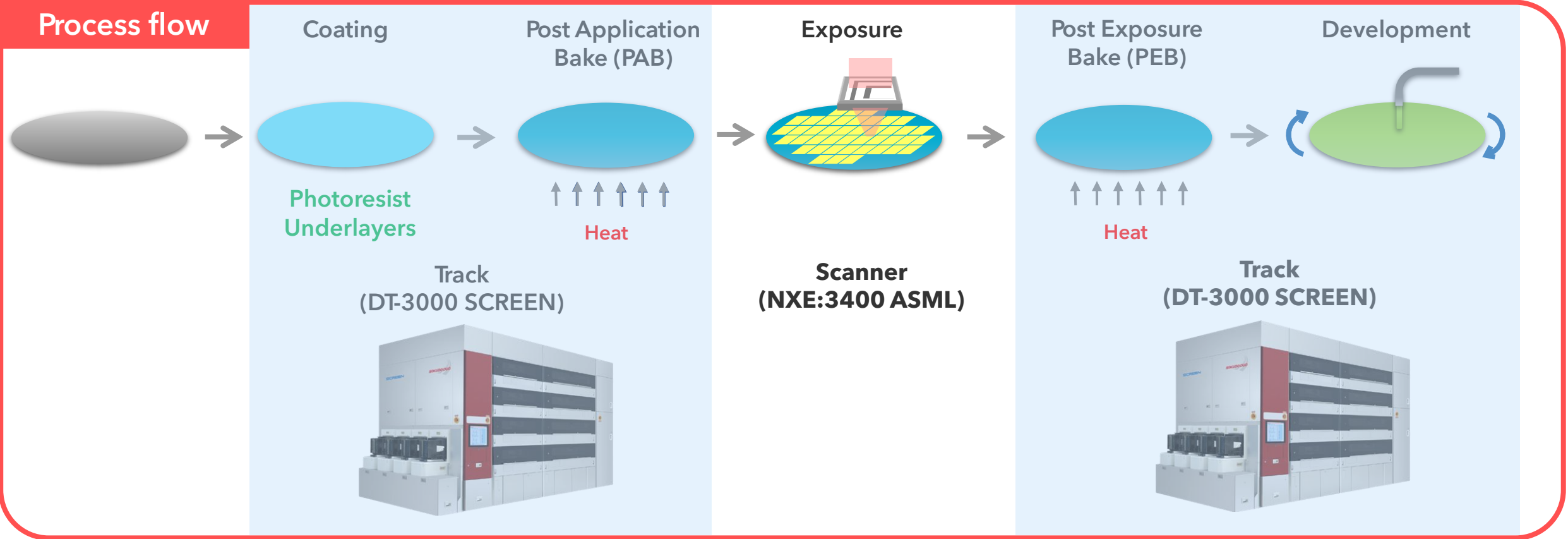


N3

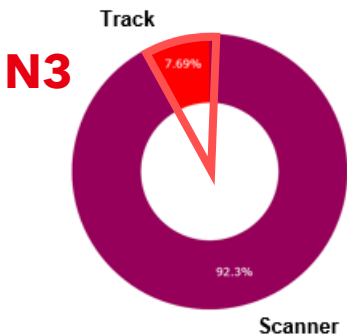
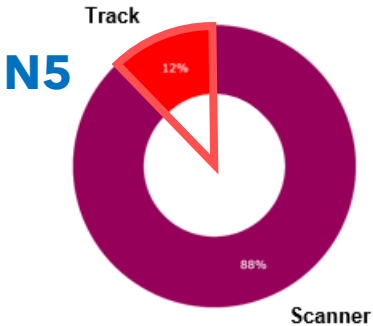


Electricity consumption rated as a top problem to address in the lithography area!

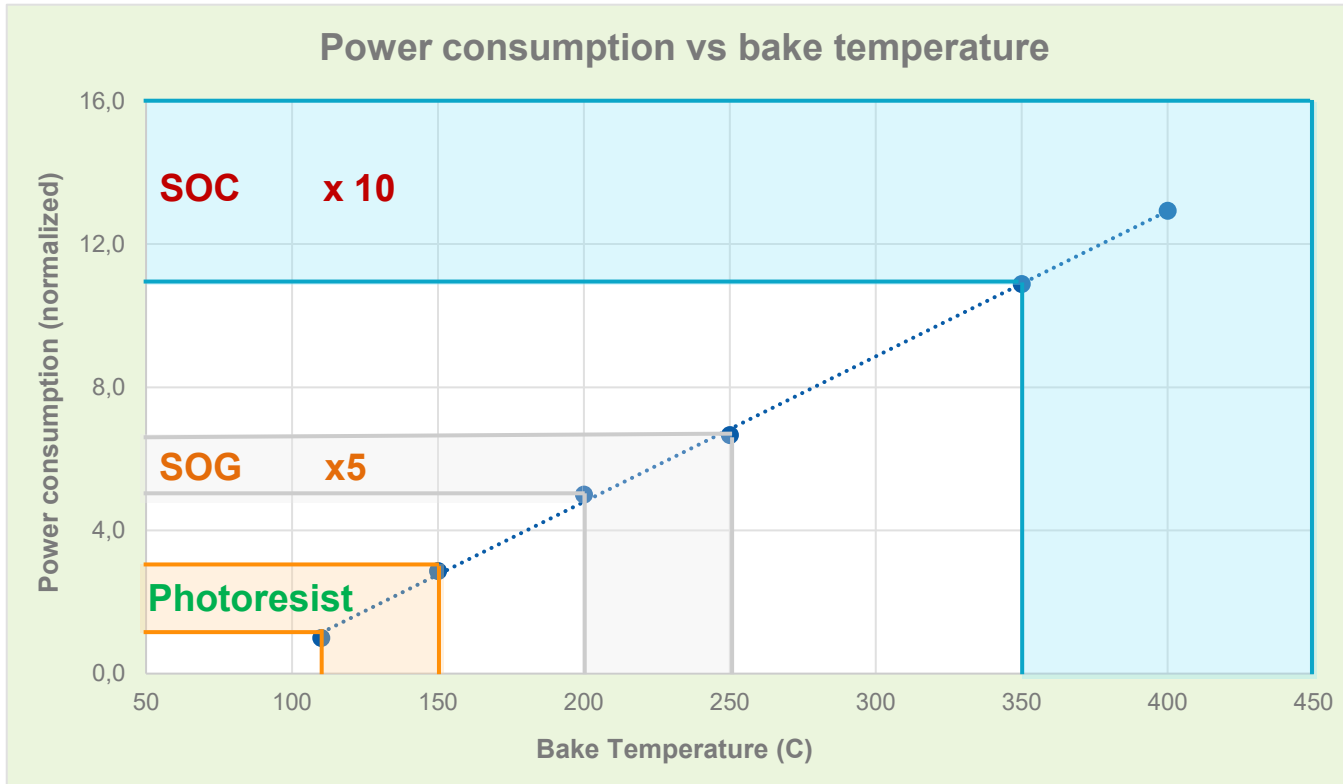
Standard litho evaluation flow



Full electric energy
consumption on Litho
Area

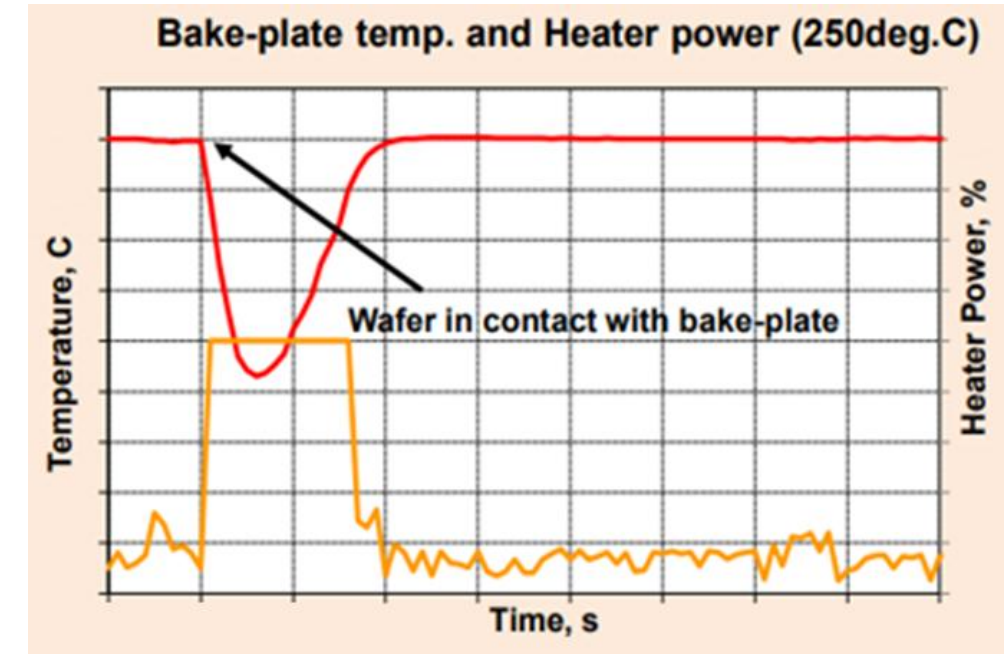


Energy-saving during bake process



Due to the high temperatures required, the baking of underlayer materials is one of the top track energy consumers

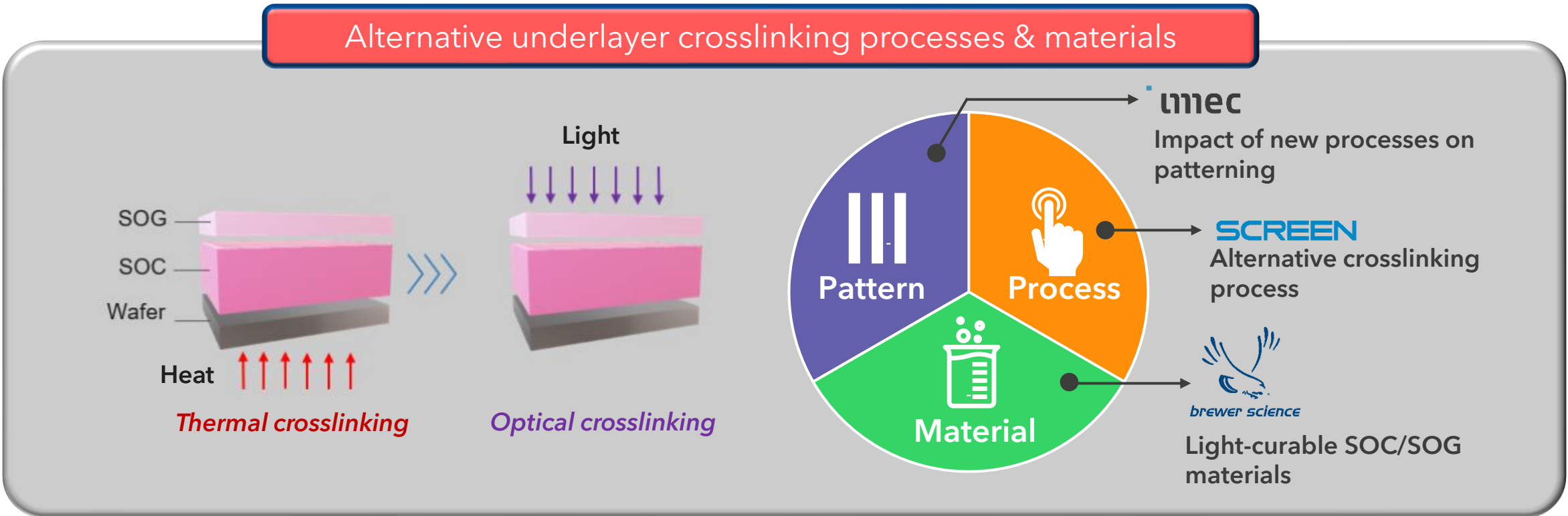
Thermal crosslinking processes require constant electricity supply:



- Track needs to keep bake temperature 24h/day
- Every time a wafer is exchanged, extra heater power is needed to keep the hotplate temperature

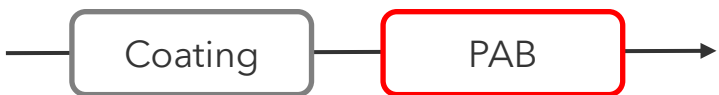
A joint effort towards more sustainable track processes

Alternative underlayer crosslinking processes & materials



Traditional:

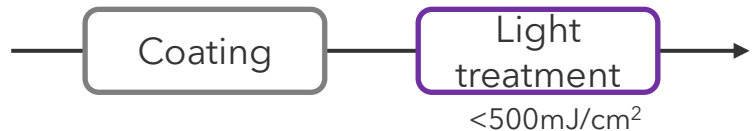
Thermal crosslinking process



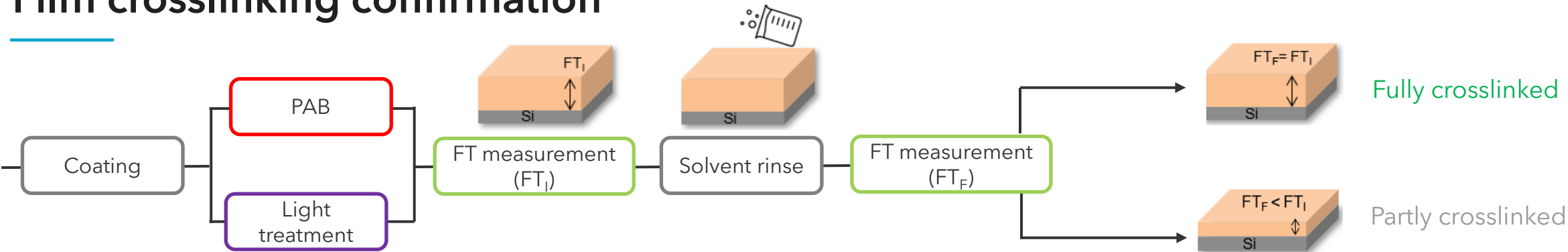
New

concept:

Optical crosslinking process



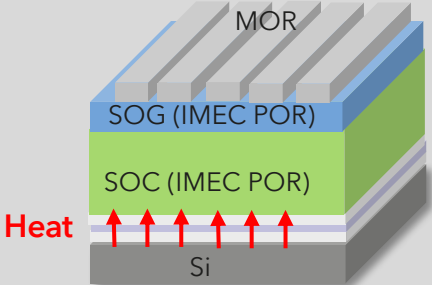
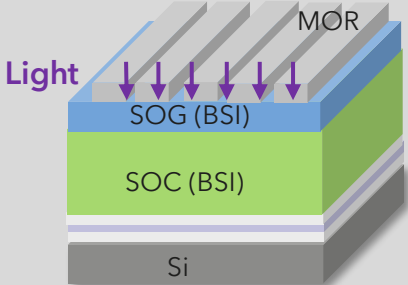
Film crosslinking confirmation



Thickness loss after strip: > 5% < 5% 0%		Bake Temperature		
		Spin-On Carbon (SOC)		
		Thermal curable (IMEC POR)	Light curable (BSI)	
		180°C → 350°C	No bake	No bake
Exposure dose (mJ/cm ²)	0			
	50			
	100			
	200			
	800			
	1000			

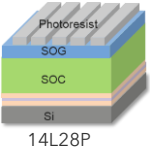
SOC & SOG light curable materials can be fully crosslinked without heat, using very low dose

Patterning Performance assessment

	Thermal crosslinking	Optical crosslinking
Material Stack		
SOC	Bake 1: 180°C 60s Bake 2: 350°C 60s	200mJ/cm ²
SOG	220°C 60s	200mJ/cm ²
Pattern	14L28P	

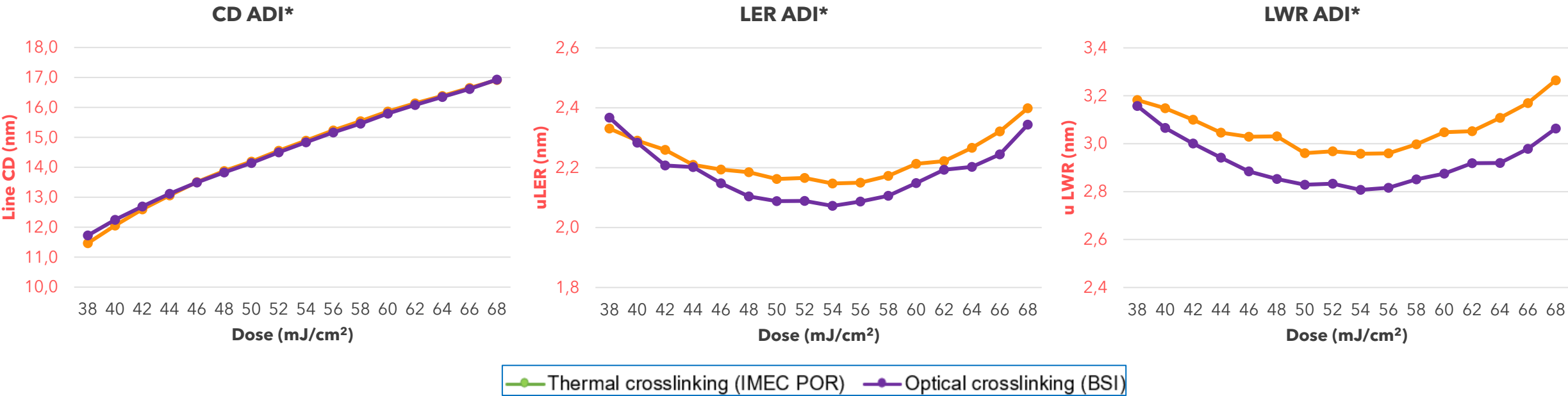
How does the performance of a stack composed with underlayers optically crosslinked compare to a standard stack?

Assessment of Patterning Performance



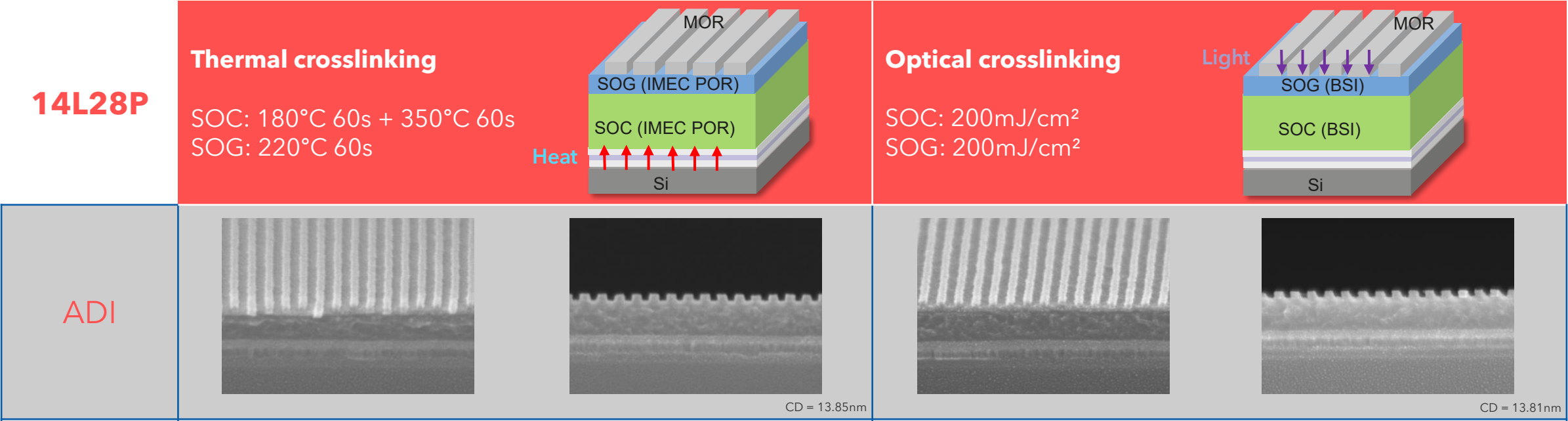
*20 images collected per dose

Crosslinking mechanism	SOC curing	SOG curing	Dose-to-size (mJ/cm ²)	uLER (nm)	uLWR (nm)	DOF (nm)	EL (%)
Thermal crosslinking (IMEC POR)	Bake 1: 180°C 60s Bake 2: 350°C 60s	220°C 60s	50	2.16	2.96	90	24.27
Optical crosslinking	200mJ/cm ²	200mJ/cm ²	50	2.09	2.83	98	26.69



Optical crosslinked materials show very competitive lithography performance

Cross-section SEM images



Cross-section images for both approaches are showing comparable profiles

Is optical crosslinking a truly energy efficient approach?

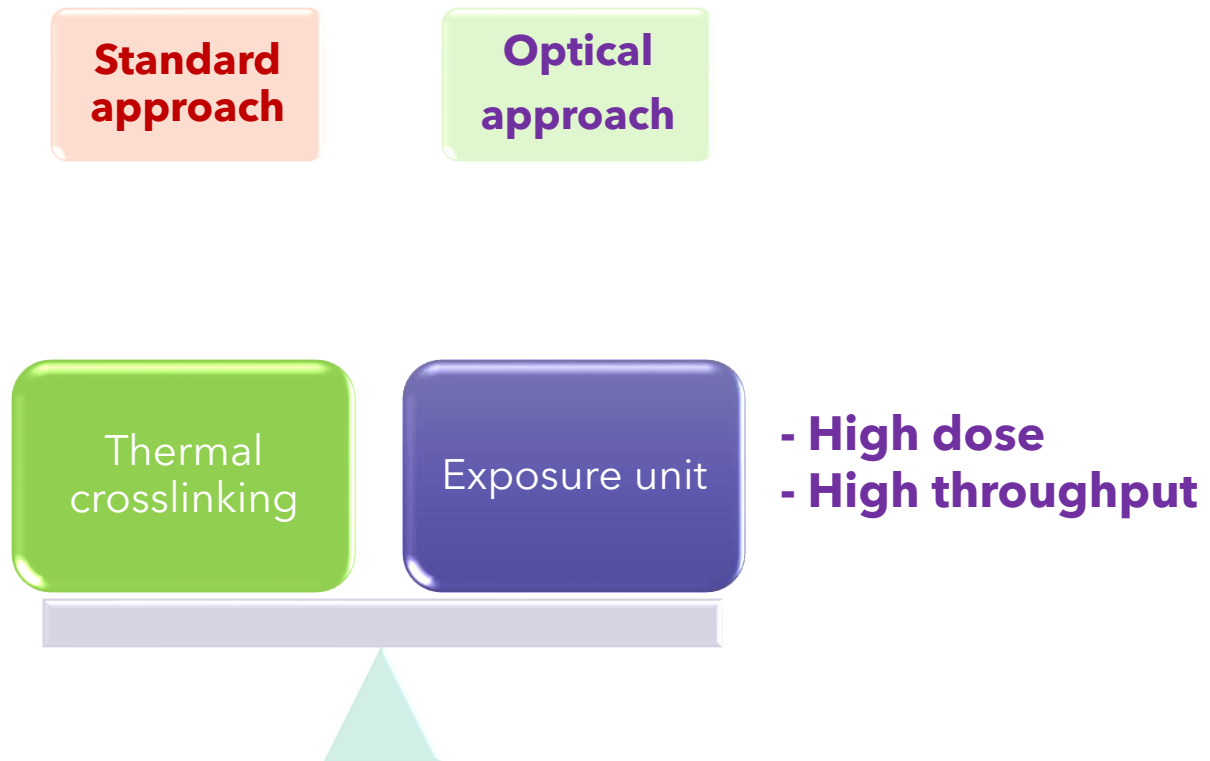
Power measurements carried out under imec SSTS umbrella:



Sustainable Semiconductor
Technologies and Systems

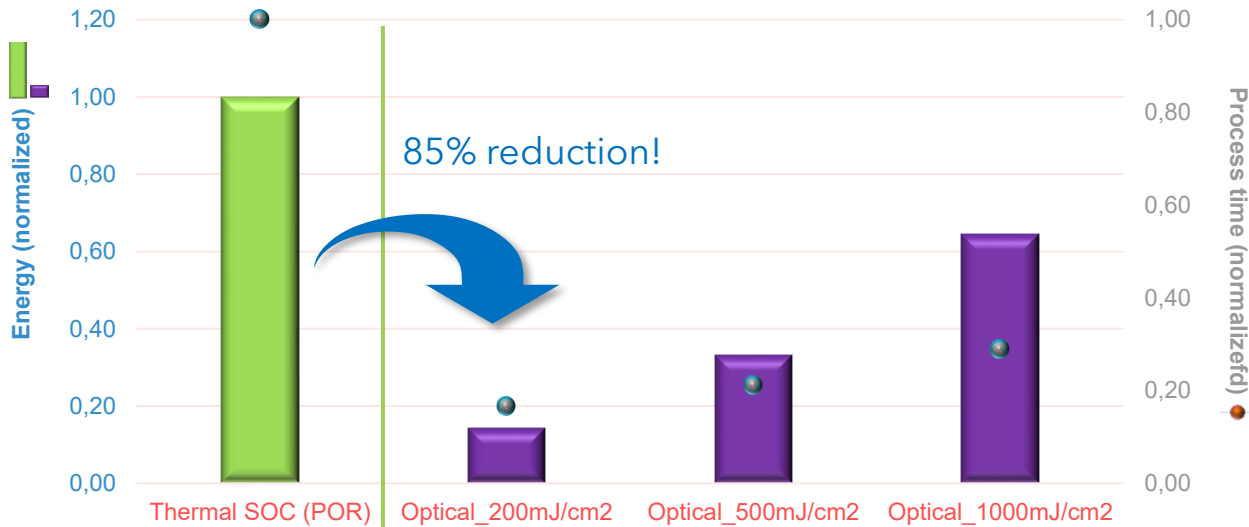


SCREEN DT-3000

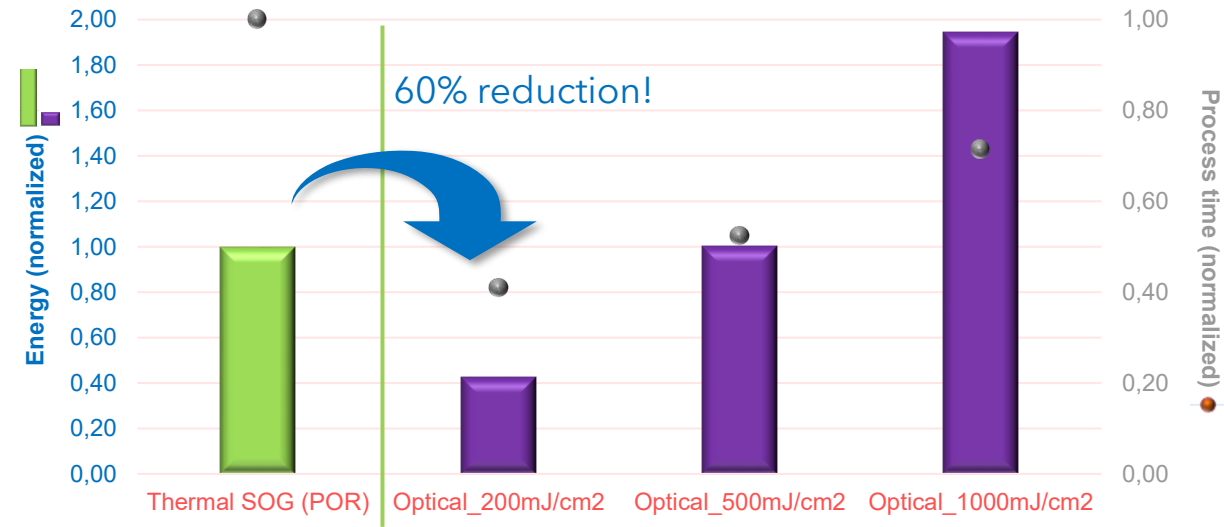


Process benchmark

Spin-On Carbon



Spin-On Glass

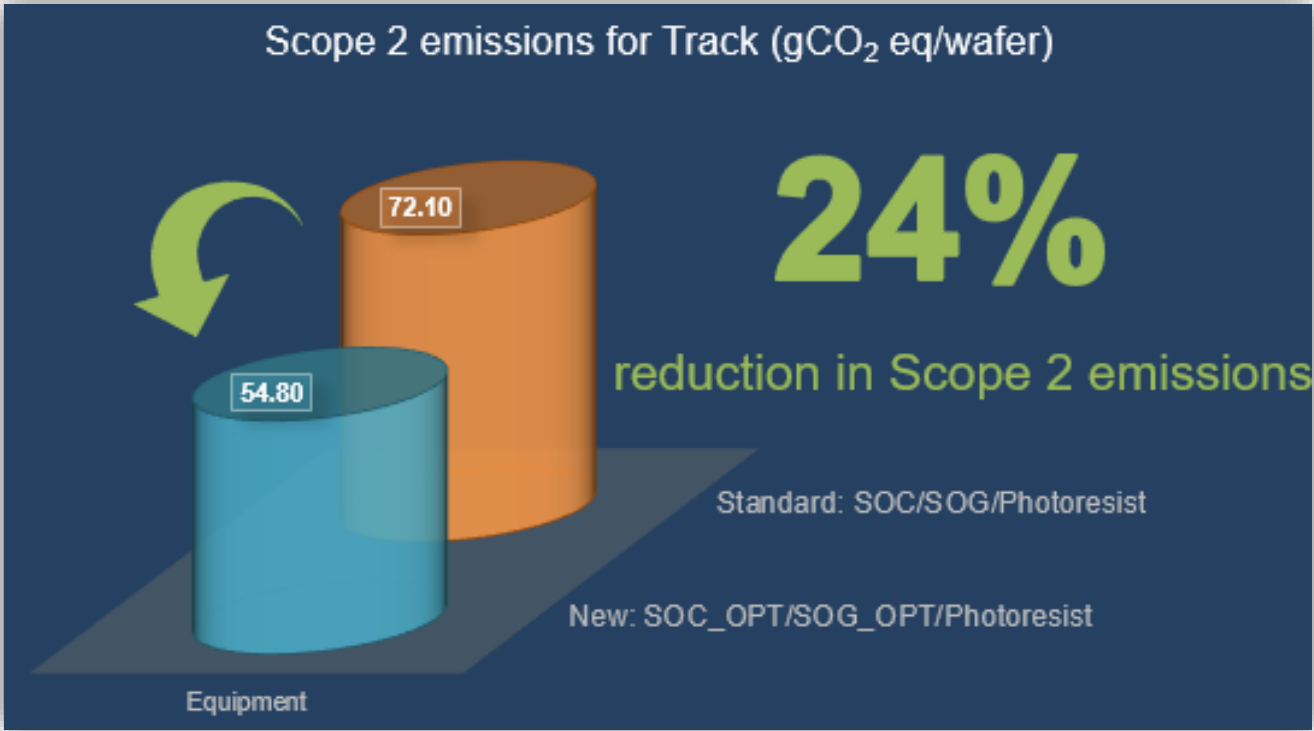
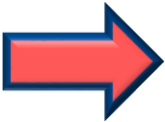
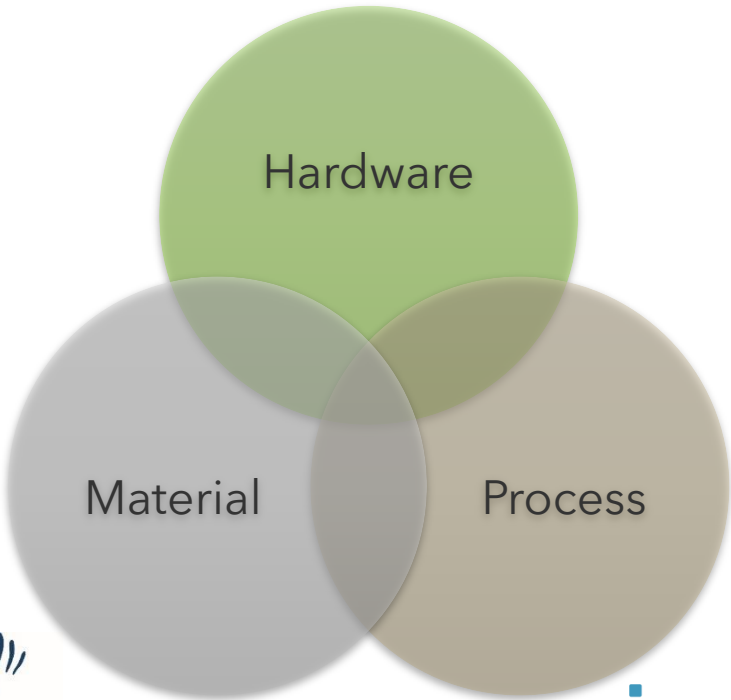


Optical crosslinking leads to significant savings of energy and process time, without compromising litho performance

Take-away

Collaboration across the semiconductor supply chain is THE KEY to create a more sustainable industry!

SCREEN



umec



SCREEN is continuously seeking and evaluating solutions to reduce greenhouse gas emissions and material utilization for a more sustainable semiconductor industry

Acknowledgements:

SCREEN

Takumi Mikawa
Ian Brown



Veerle Van Driessche
Jakub Koza
Daniel Sweat

umec

Lars-Ake Ragnarsson
Emily Gallagher
Andrea Firrincieli
Cedric Rolin
Bram Vangestel
Alexander Dockx



A Better Tomorrow With Our Partners



Innovation for a Sustainable World

人と技術をつなぎ、未来をひらく

