ADVANCED 3D STACKING TECHNOLOGY FOR HIGH PERFORMANCE COMPUTING

SEMI 회원사의 날 2025

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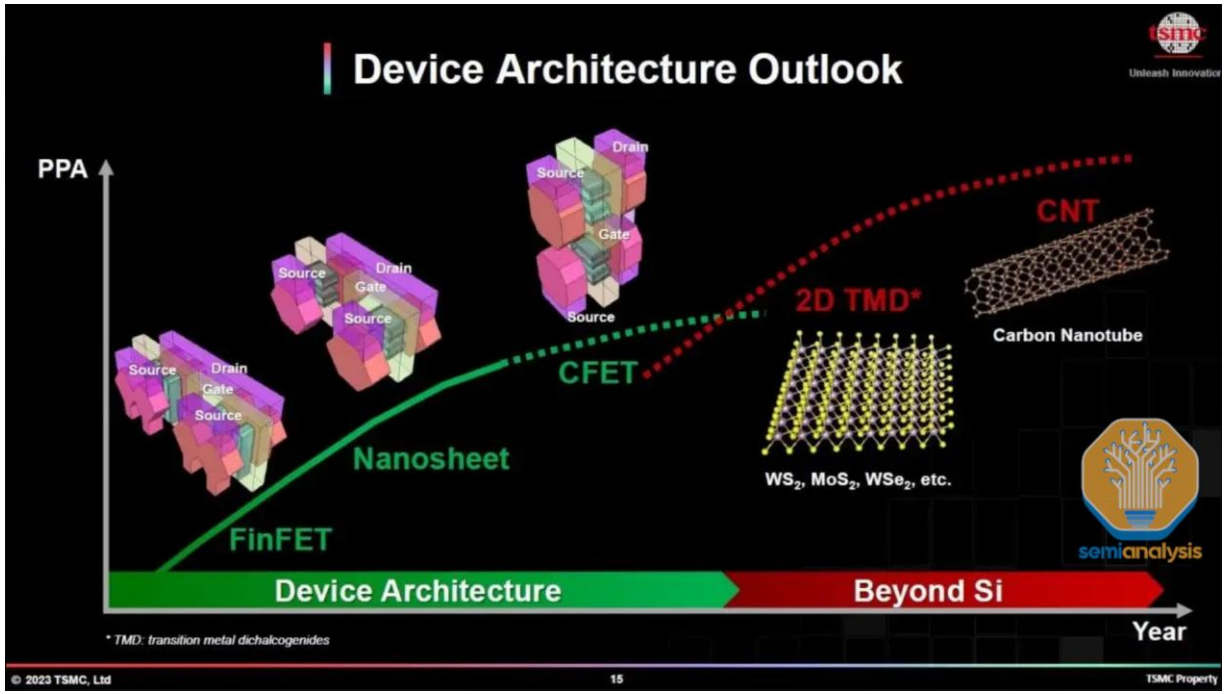
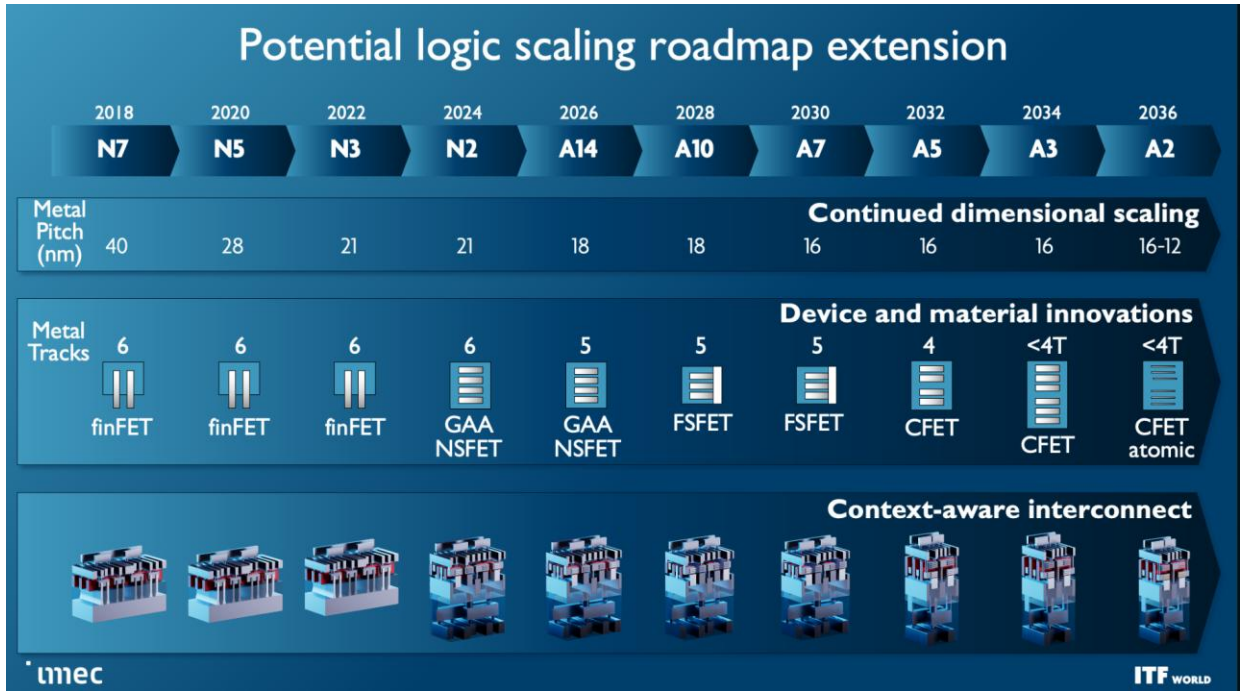
Importance of Interconnection : Limitation of Logic Devices



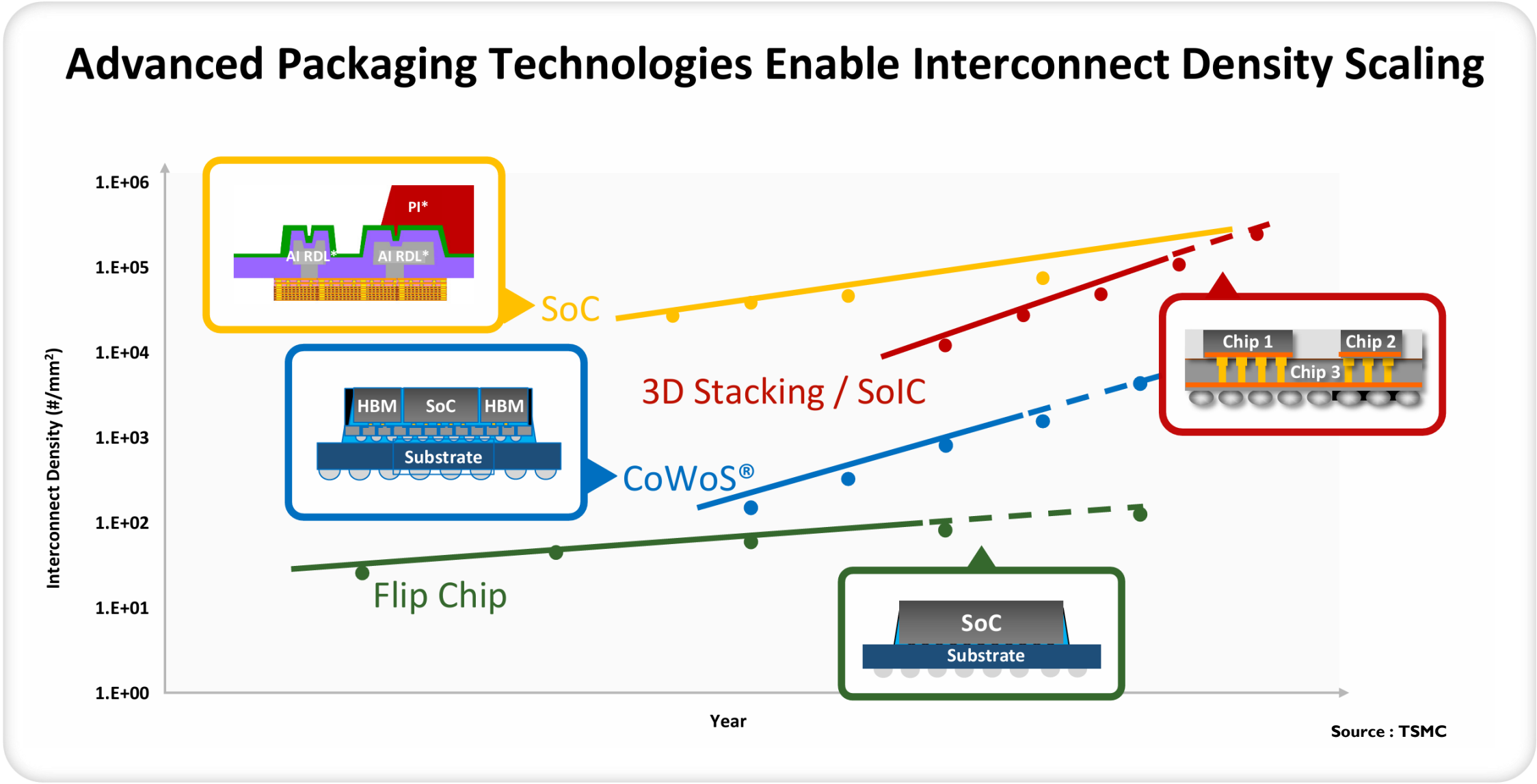
Ref: TSMC



Ref: IMEC

- Existing Si-based devices currently lack clear alternatives for post-CFET technology. Research is expected to focus on the development of new chalcogenide materials (2D Chalcogenide, Carbon, etc.).
- Along with improving the performance of existing devices, the development of interconnection technology is emerging as a critical development issue (e.g., F2F Bonding, BSPDN).
- Vertical integration simultaneously achieves performance, power efficiency, and cost optimization, leading innovation particularly in the fields of Artificial Intelligence (AI) and High-Performance Computing (HPC).

3D packaging tech. CAN overcome in-fab. technology



Revolutions of 3D Stacking Technology in Logic Devices Developments

•**Improved Performance and Bandwidth** Achieved over 10x higher bandwidth and low latency through vertical interconnect (TSV). Electrical reliability of 3D stacking in synchronous design proven by applying F2F hybrid bonding technology. (ARM Co.)

•**Heterogeneous Integration** Maximized system-level efficiency through vertical integration by separately manufacturing logic, memory, and analog circuits through their respective processes. TSMC's CoWoS and Intel's EMIB 2.5D/3D packaging technologies provide optimal system support.

•**Cost Efficiency** Improved yield and reduced manufacturing costs by dividing large single chips into smaller chiplets. Maintained compatibility with existing silicon-based circuits through low-temperature (400◦C or below) stacking processes.

•**Reduced Power Consumption** 10 to 100 times lower driving power consumption due to shortened signal paths. 19% performance improvement without redesigning additional cache directly into TSV. (AMD 3D V-Cache)

Cu Hybrid Bonding Technologies

pitch scaling & density in 3D Interconnect

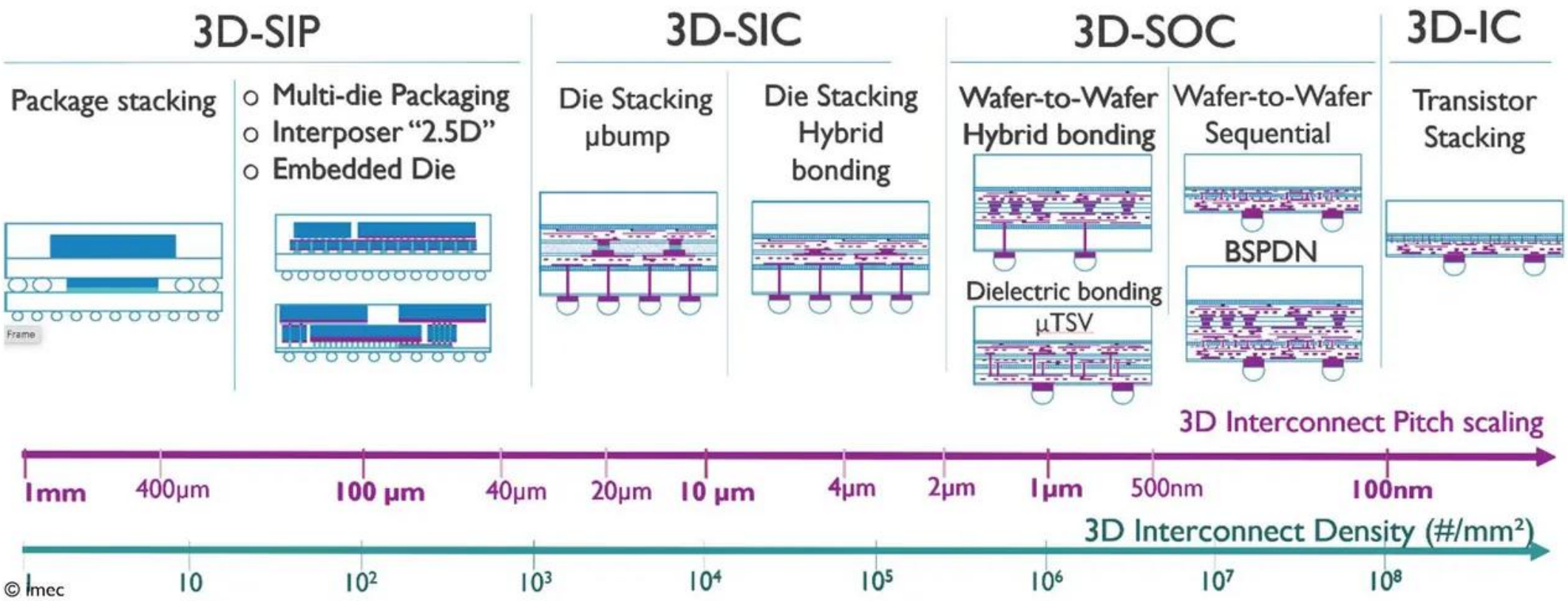


Figure 1: The imec 3D interconnect technology landscape

Two Different pathway for Chip Stacking Technology

Feature	Normal Hybrid Bonding with TSVs	Face-to-Face (F2F) Hybrid Bonding
Inter-Die Connection	Hybrid bond for surface connection, TSVs for vertical through-silicon connection.	Direct hybrid bond of active surfaces (metal layers).
TSV Requirement	Essential for vertical connectivity through silicon.	Not needed between the directly bonded F2F layers for communication, but may be needed for external connectivity.
Interconnect Pitch	Fine, but TSV size can be a limiting factor for ultimate density.	Can achieve the absolute finest pitches (sub-micron).
Silicon Area Usage	TSVs occupy silicon area.	Frees up silicon area where TSVs would otherwise be placed for inter-die communication.
Latency/ Performance	Very good due to short TSV paths.	Potentially the lowest due to direct metal-to-metal connection.
Thermal Management	Generally more straightforward as active layers can be on the outer sides for easier cooling.	More challenging due to active layers facing each other, requiring innovative solutions.
Fabrication Complexity	Complex due to TSV processing.	High, primarily due to extreme surface preparation and alignment requirements.
Yield	Impacted by both hybrid bonding and TSV yields.	Highly sensitive to surface quality and alignment, making KGD challenging.
Applications	HBM, 3D stacked memory, high-performance computing.	Advanced image sensors, high-performance logic-on-logic or logic-on-memory integration.

Multi Die Hybrid Bonding Technologies

Multi-Die Hybrid Bonding : High Bandwidth Interconnect Technology

1. Ultra-Fine Pitch Scaling and Electrical Performance

• Sub-Micron Cu-Cu Bonding: Investigations into pitches ≤1 µm revealed that as Cu pad size and pitch decrease, initial resistance and its variability increase, while bonding yield drops. However, high-temperature testing can densify the bond, reducing resistance and improving yield.

• Surface Preparation: Pre-bonding surface protection and cleaning (e.g., FTIR, Raman spectroscopy) are crucial for maintaining low resistance and high yield at these fine scales.

2. Microstructural Optimization

• Metastable High Defect Density Cu: Research has highlighted the benefits of metastable fine-grain Cu films for hybrid bonding

• Cu Protrusion Control

3. Process Innovations

•Surface-Activated Bonding

•TSV Reveal and Cleaning: Direct Si/Cu grinding with in-situ cleaning and electroless Ni–B plating effectively exposes TSVs

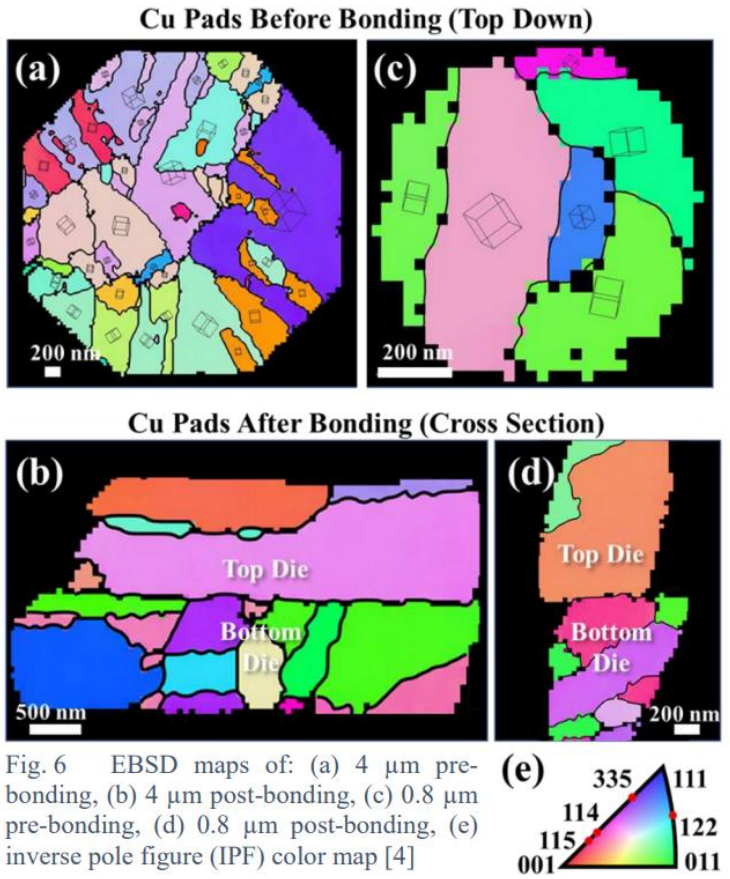


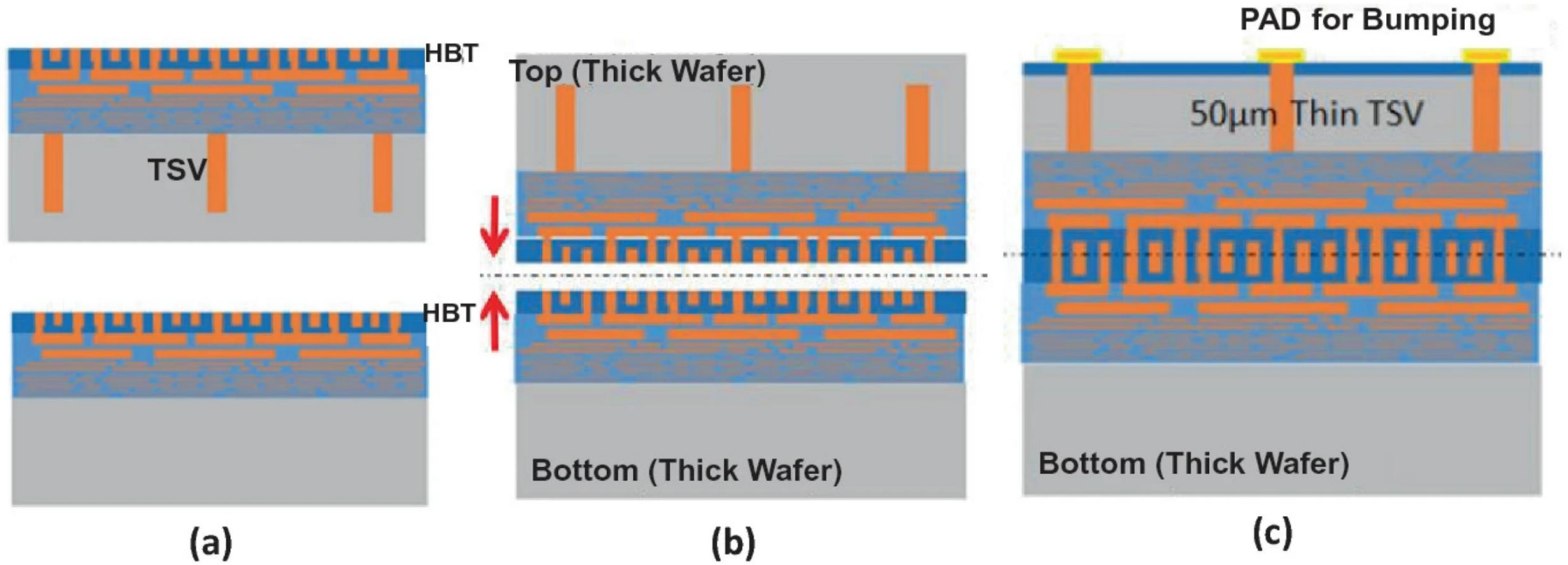
Fig. 6 EBSD maps of: (a) 4 µm pre-bonding, (b) 4 µm post-bonding, (c) 0.8 µm pre-bonding, (d) 0.8 µm post-bonding, (e) inverse pole figure (IPF) color map [4]

Ref : 2025 ECTC, IBM

Face to Face Hybrid Bonding Technologies

F2F Hybrid Bonding : High Density 3D Interconnect Technology in Wafer Scale

- Wafer to wafer bonding technology
- 3D device integration technology that creates high-density interconnects between chips without TSVs through direct bonding.



a Top wafer with TSV and bottom wafer without TSV. **b** Top and bottom wafers undergoing F2F bonding. **c** Revealed TSV (thinned) side is the bump/pad terminal side [27]

Ref : Global Foundries

Face to Face Hybrid Bonding Technologies

F2F Hybrid Bonding : High Density 3D Interconnect Technology in Wafer Scale

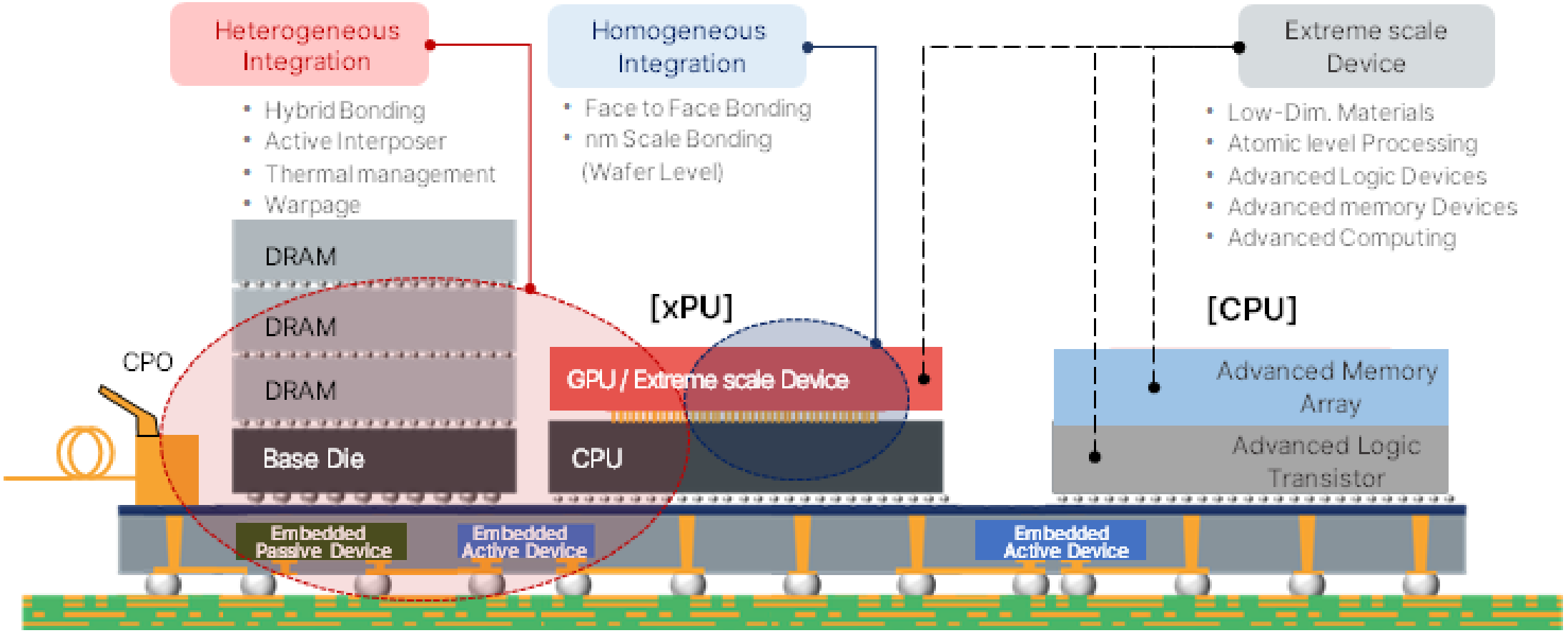
- **Next-Generation High-Performance Chiplet Packaging Technology**
- Die-to-die copper direct bonding without micro bumps
- Overcoming the limitations of existing TSV-based methods

- **Ultra-fine Pitch Interconnect Structure (Sub-10μm)**
- Removes TSV area overhead with pitches below 10μm
- Shortened signal path through direct die-to-die connection

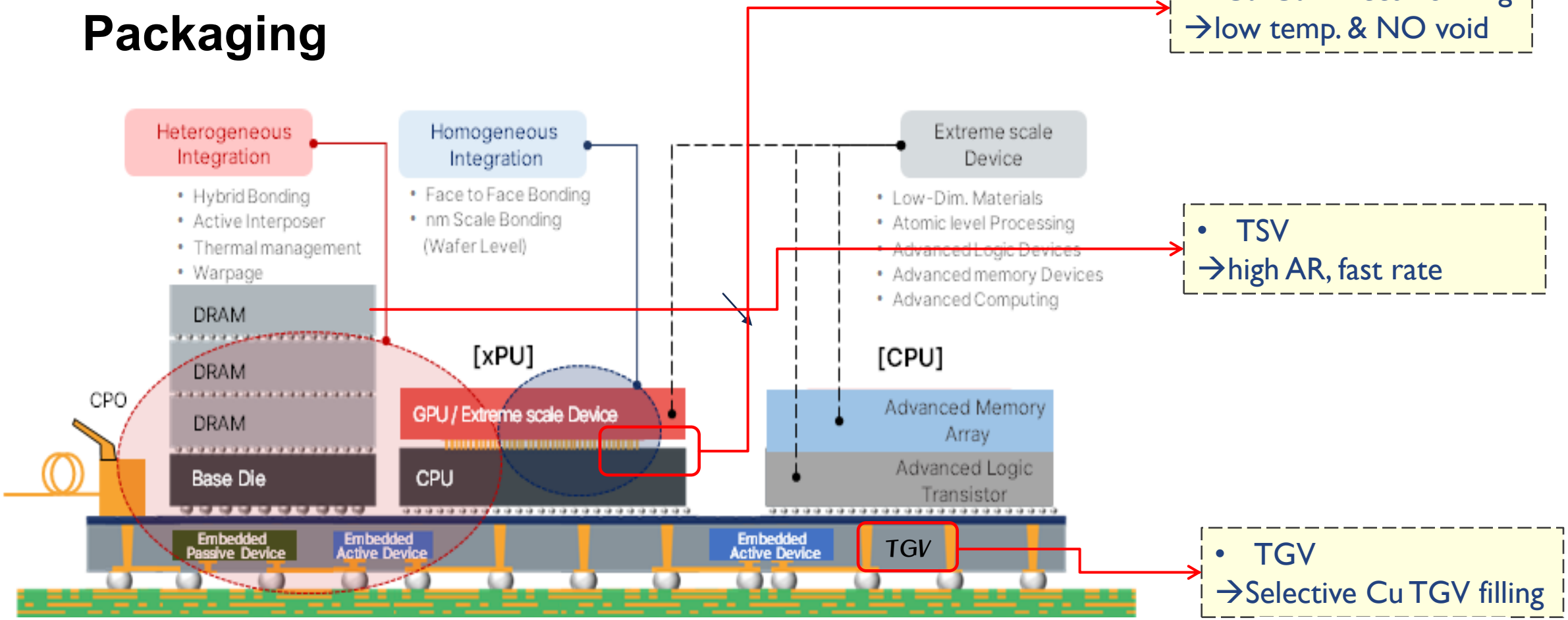
- **No Micro Bumps**
- Up to 90% reduction in parasitic capacitance
- Improved power efficiency and speed

Parameter	TSV-Based 3D ICs	F2F Hybrid 3D ICs	Improvement
Interconnect pitch	10-20μm	0.5-2μm	10× denser
Critical path latency	120 ps	65 ps	46% lower
Cross-die wirelength	500-1000μm	50-200μm	80% shorter
Power-delay product	0.5 pJ/bit	0.02 pJ/bit	25× better

Future Technology Platform for High Performance Computing



Metalizations focused on 3D Advanced Packaging



- Cu-Cu Direct Bonding
→low temp. & NO void

- TSV
→high AR, fast rate

- TGV
→Selective Cu TGV filling

Materials Characteristics of Metal Candidates

		Al	Au	Ag	Cu	W	Ru	Nl alloy
Resistivity (μΩ-cm)		2.66	2.35	1.59	1.67	5.6	7.1	7.0~10
ΔR/ΔT at 0–100 °C (10^{-3}/K)		4.5	4.0	4.1	4.3	4.4	4.1	1.1
Melting point (°C)		660.1	1063	960.8	1083.4	3422	2334	1425
Atomic weight (amu)		26.982	196.967	107.868	63.54			
Young's modulus (GPa)		70.6	78.5	82.7	129.8			
Yield strength (MPa)		55	130	172	216			
Hardness (HV)		15	20–30	25	51			
D_o (cm^2/s) for diffusion		1.71	0.67	1.89	0.78			
Q (eV) for diffusion		1.48	1.96	2.01	2.19			
D (cm^2/s) at 100 °C		2.1×10^{-20}	2.2×10^{-27}	1.1×10^{-26}	2.1×10^{-30}			
-Zq (effective charge)		6.5–16.4 q	5.9–7.4 q	9.4–23.4 q	3.7–4.3 q			
Thermal conductivity (W/cm)		2.38	3.15	4.25	3.98	1.7	1.2	~0.4
Availability of deposition and etching technique	Sputtering	Yes	Yes	Yes	Yes	yes	yes	yes
	Evaporation	Yes	Yes	Yes	Yes	yes	yes	yes
	CVD	Yes (?)	?	?	Yes	yes	yes	?
	Plating	?	Yes	Yes	Yes	?	yes	yes
	Wet etching	Yes	Yes	Yes	Yes	yes	yes	yes
	Dry etching	Yes	?	?	?	yes	yes	yes
Electromigration resistance		low	high	very low	high	high	high	high
Corrosion resistance in air		high	very high	low	low			

- Direct Bonding
→Cu & Al(?)

- TSV & TGV
→Cu, Ni alloy(?)

- Nano-TSV
→Ru, W, Cu(?)

- Ru
→ short electron mean free path

- Ni Alloy (Invar)
→ Low Coefficient of Thermal Expansion (CTE)

유창섭 박사 Thesis

Glass as an interposer or core

- **Advantages of glass Interposer**

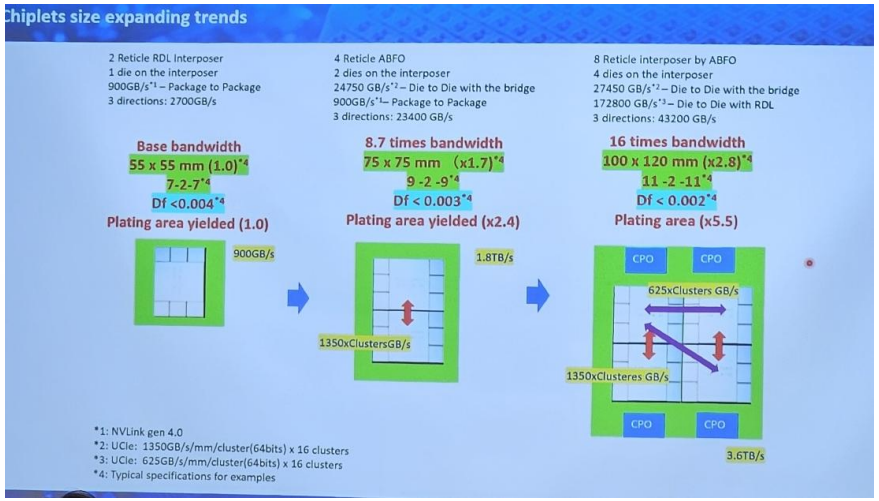
1) Low electrical loss (NO need of passivation)
2) Low cost
3) Easy to make the large size and thin thickness
4) Tailored coefficient of thermal expansion (CTE)
5) CAF safty

- **Disadvantages of glass Interposer**

1) Easy to cracks
2) Easy to break
3) Transparency
4) Comparably large Size of Via
5) Difficult to utilize thin layer

기판·인터포저 코어	실리콘	유기		유리
		적층(laminate)	팬아웃	
Material properties				
표면의 거칠기(nm)	<10	400-600	> 1000	<10
열팽창계수(CTE)(ppm/K)	2.9-4	3-17	16-30	3-9
영률(소재의 유연함) (GPa)	165	10-40	22	50-90
Moisture absorption	0	0.04%	1-2.5%	0
열전도율 (W/m.K)	148	0.9	0.5-0.75	1.1
Physical Dimensions				
패키징 사이즈 (mm)	35x35	70x70	50x50	100x100
웨이퍼·패널 사이즈	300 mm	710 mm²	300 mm / 510 mm²	710 mm²

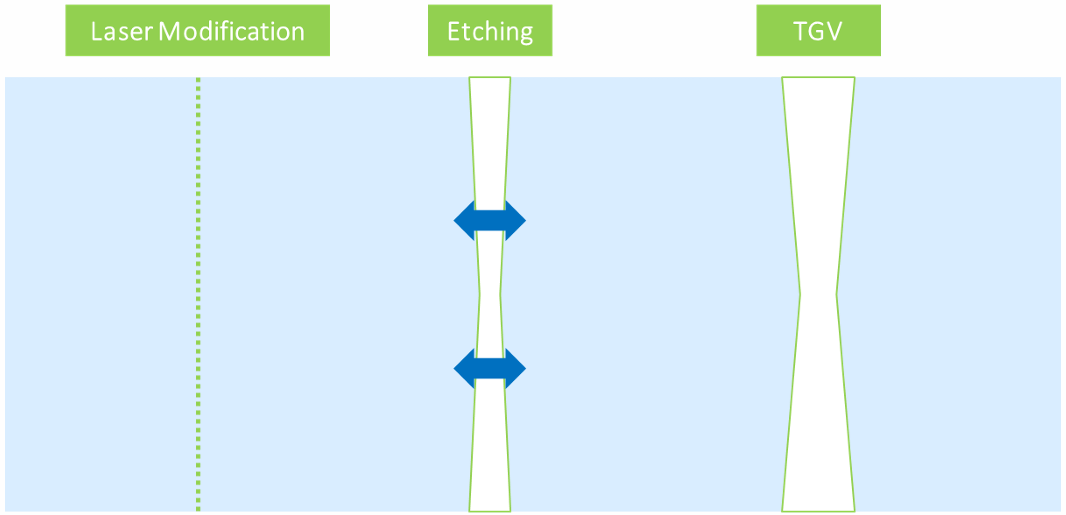
Ref : CHIMES, US
서울경제 modified



Ref : SBR Tech.

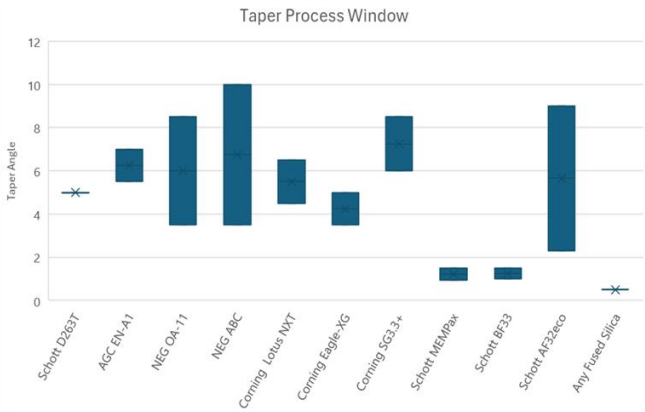
I. VIA FORMATION PROCESS : LIDE

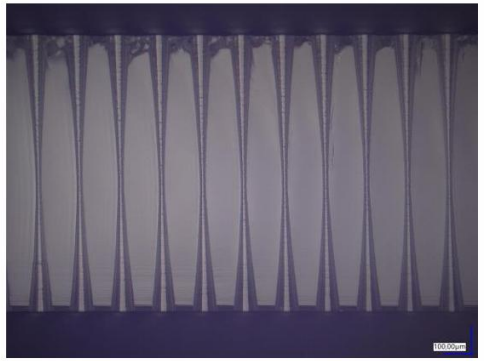
LIDE: HVM PROCESS COMPATABILITY



In the **first step**, glass of **up to 1mm** can be structured by a **single laser pulse**. Pulse positioning accuracy is >5µm Cp >1,33.

In the **second step**, the laser structured substrates are wet etched. The laser-modified regions display a much higher etch rate than the bulk material. The result is the formation of hourglass shaped holes with a tunable taper.





1000 µm Thickness

Ref : LPKF

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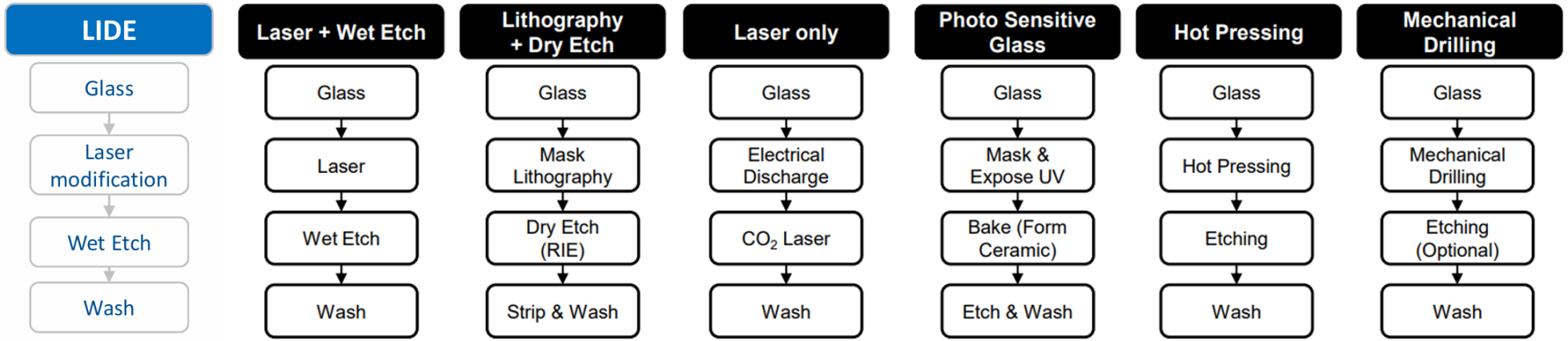
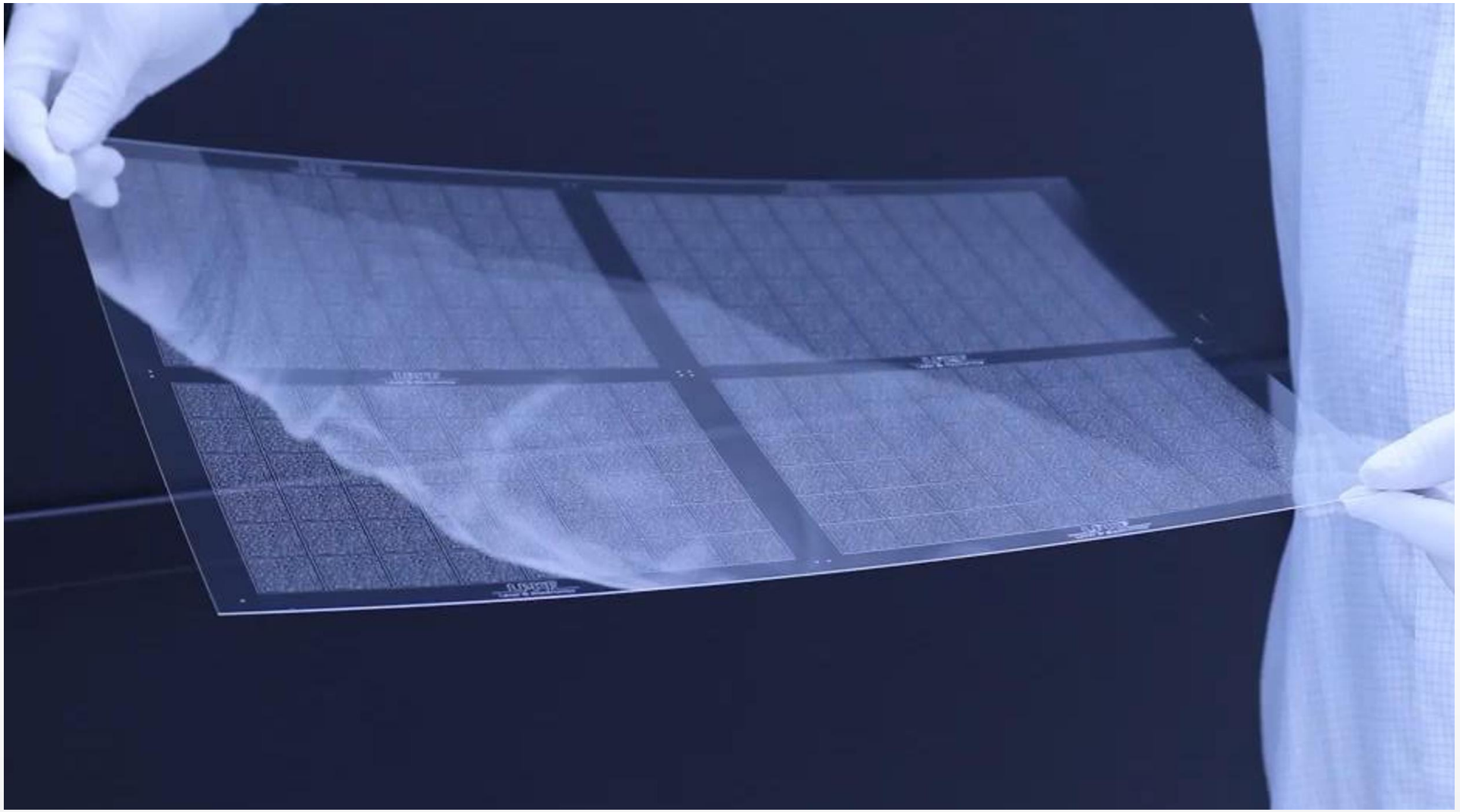


No Thermal Stress						
No Defects						
All-In-One TGV, Cavity, Cutting						
HVM capability						
All Glass Types						

Technologically LIDE is the superior process to generate microstructures in glass and provides the scalability necessary for HVM.

Ref : LPKF

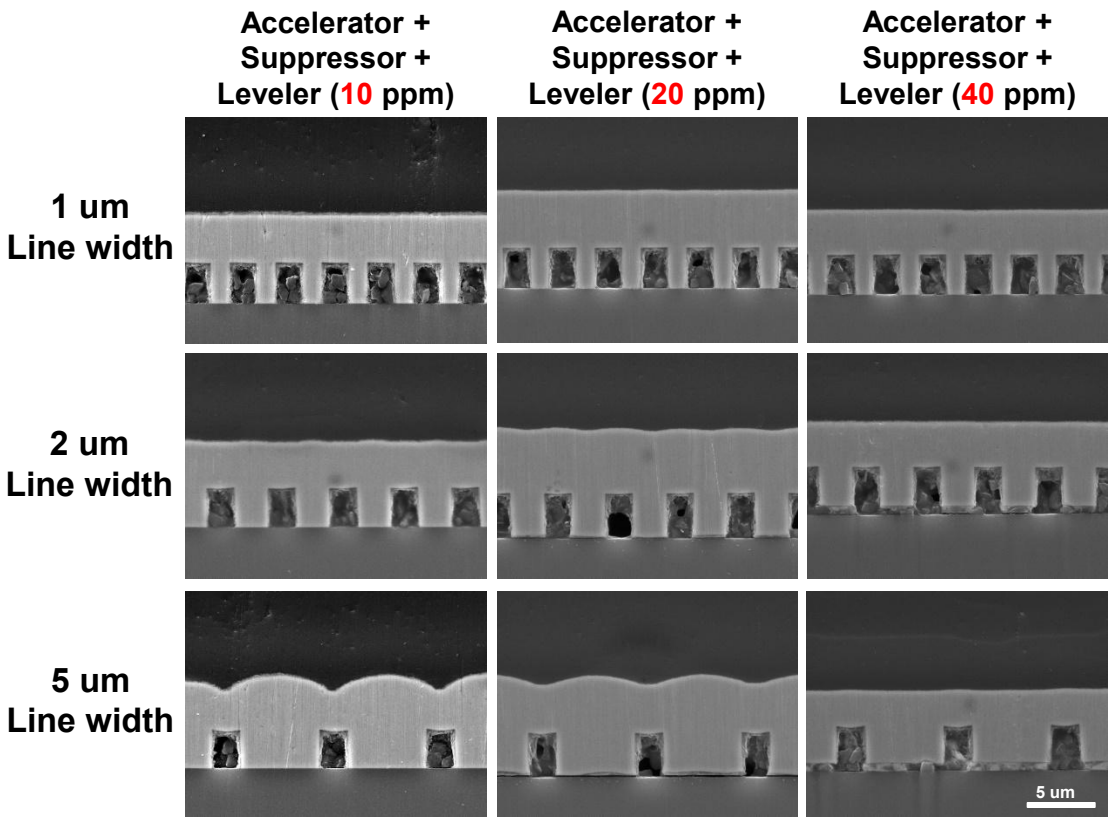
I. VIA FORMATION PROCESS : LIDE

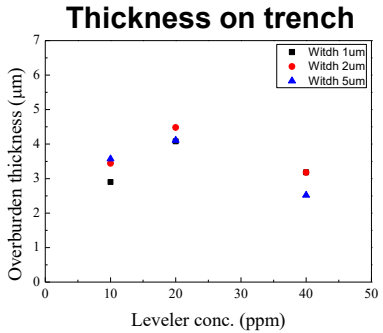


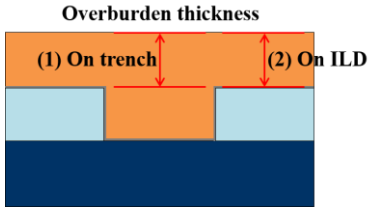
Ref : LPKF

III. Untact Polishing of Cu for Glass Substrate

Cu filling with additives – Accelerator + Suppressor + Leveler

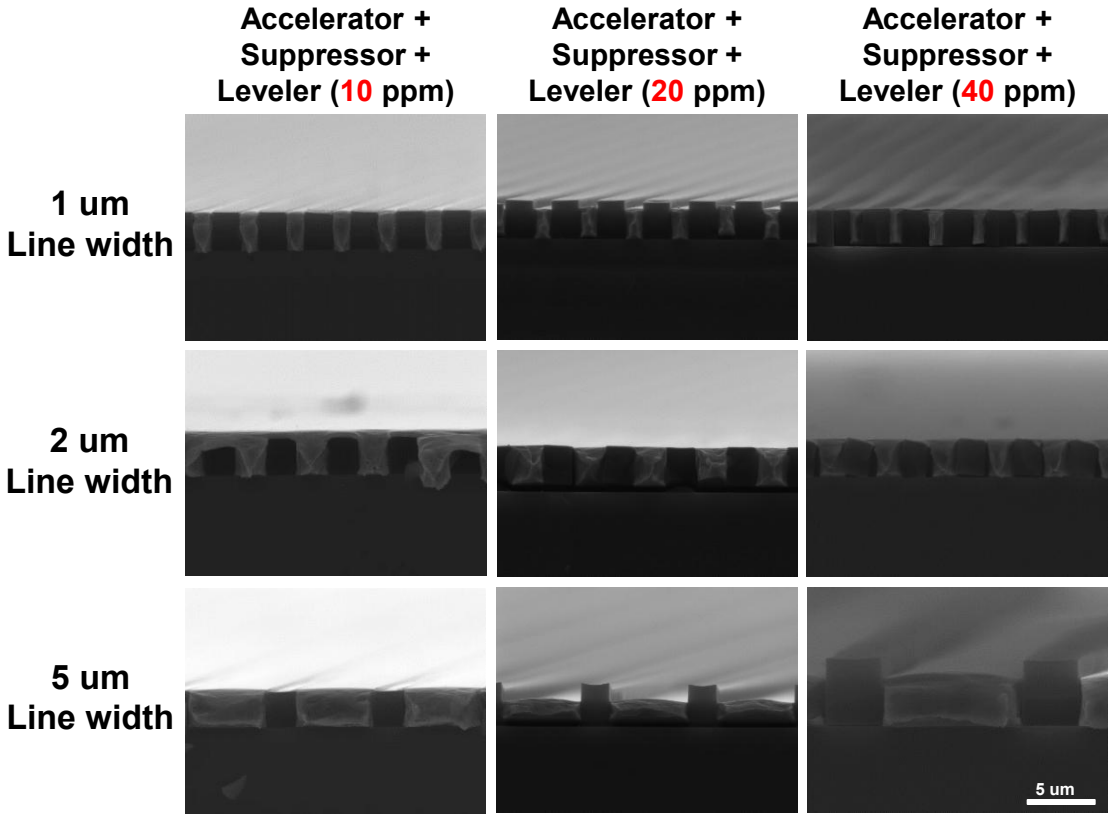


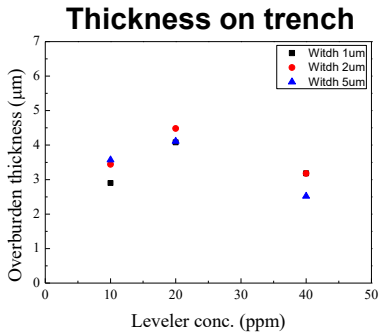


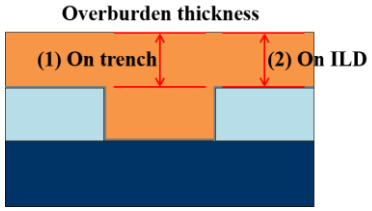


III. Untact Polishing of Cu for Glass Substrate

After Cu electrochemical polishing

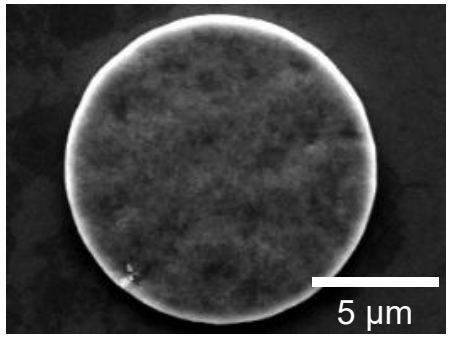


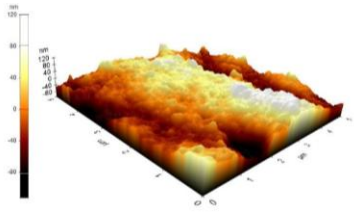




III. Untact Polishing of Cu for Glass Substrate

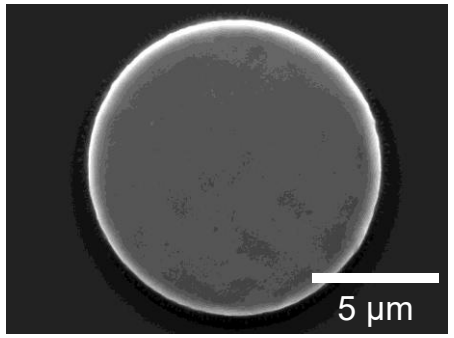
Cu plating ①

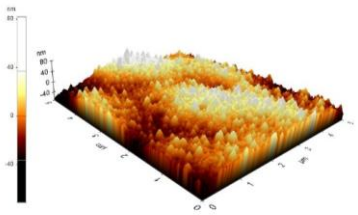




R_a: 34.8nm

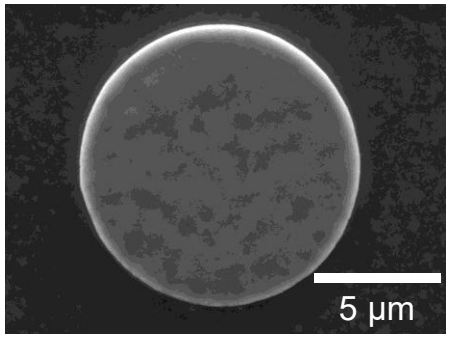
Electropolishing ②

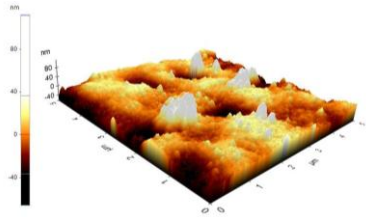




R_a: 14.8nm

Ti barrier etching ③



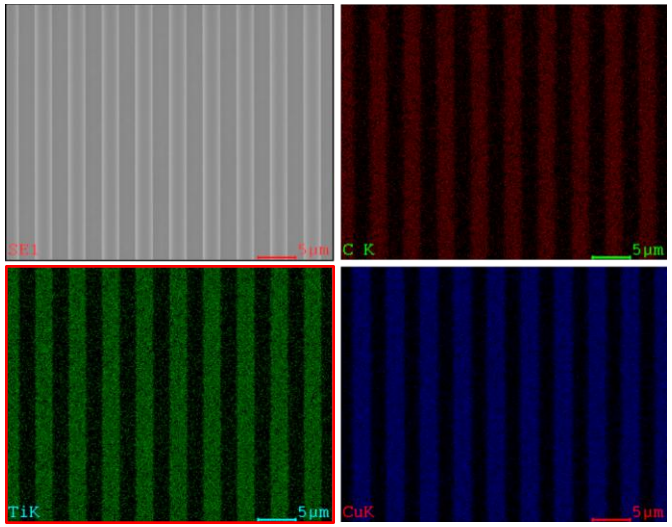


R_a: 13.8nm

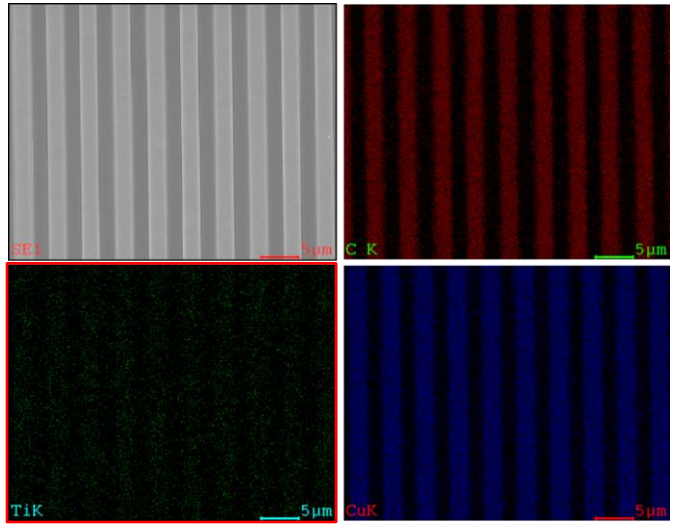
III. Untact Polishing of Cu for Glass Substrate

Top EDS analysis

Cu EP without barrier etchant

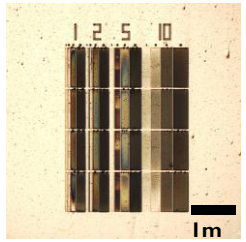


Cu EP with barrier etchant

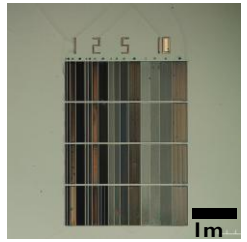


Barrier layer removal during the EP process

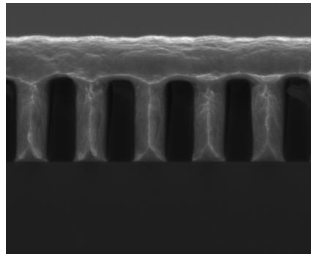
III. Untact Polishing of Cu for Glass Substrate

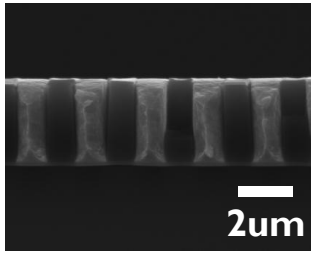


Before EP

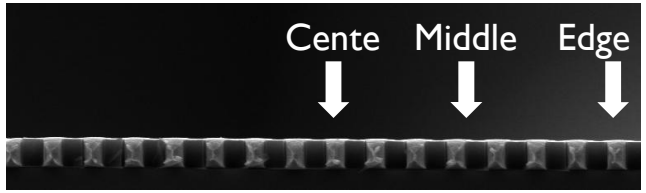


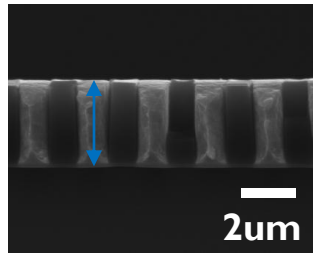
After EP





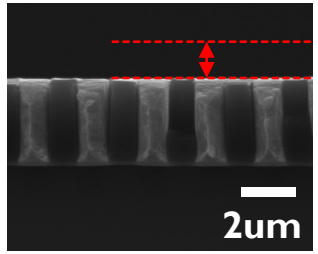
Overall Uniformity : ~ 3.5 %





X 4

Uniformity(%)=[(Max-Avg)/Avg]*100
Avg.: average thickness value among edge, middle, and center
Max.: Maximum thickness value among edge, middle, and center



X 4

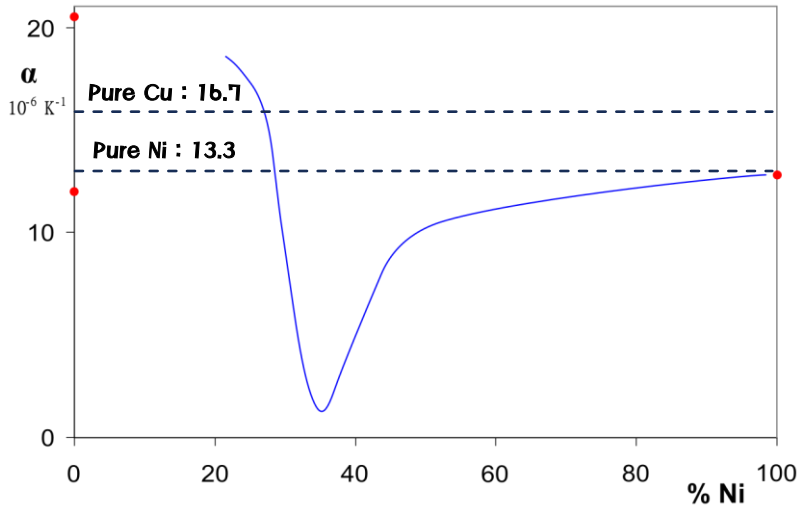
EP rate(μm/min)=Decreased thickness/process time

III. Low CTE Metal Filling for Glass Substrate

Ni or Ni Alloy (~Invar) : CTE manageable metal for Glass

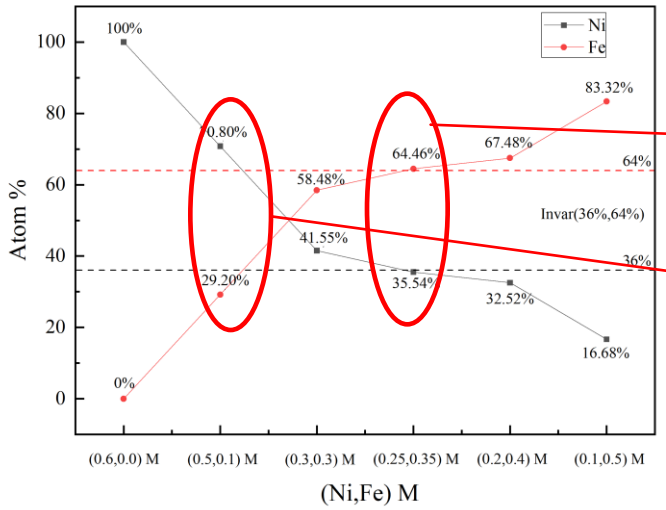
➢ **Thermal expansion coefficient of Metals**

Material	CTE (10^{-6}/°C)
Copper	16.7
Nickel	13.3
Iron	12.3
Glass	4 – 9
Invar (Ni36Fe64)	**0 - 1.2**

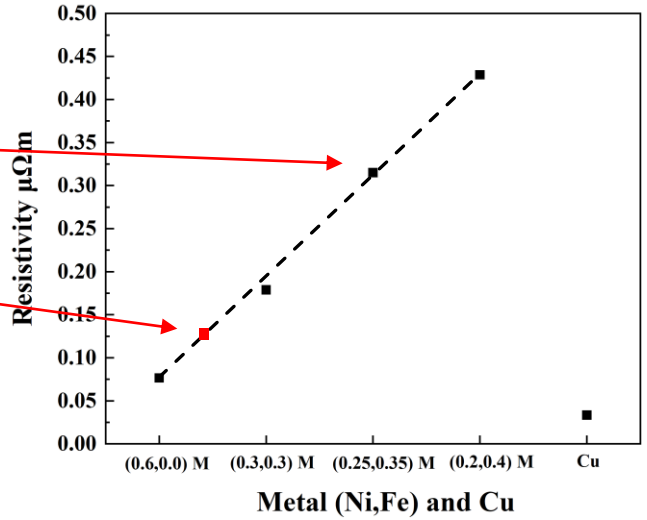


III. Low CTE Metal Filling for Glass Substrate

Composition variation



Resistivity variation

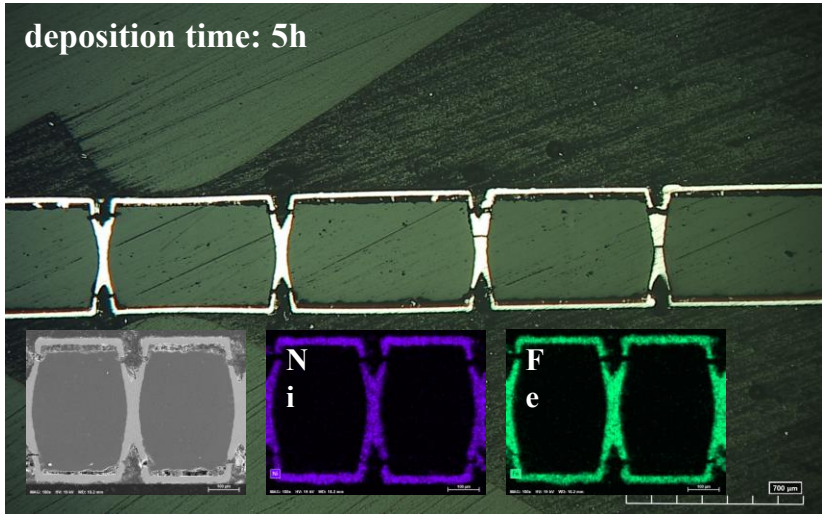


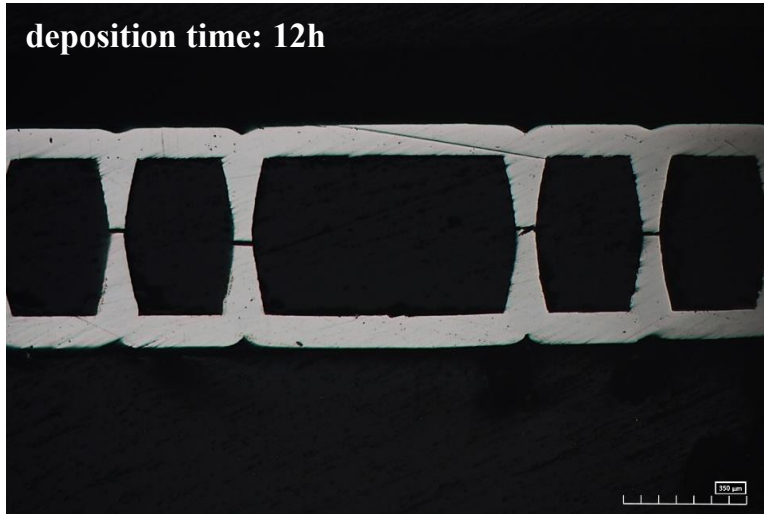
CTE of Electrodeposited alloys :

- Ni70Fe30 = 11~12 (unclear)
- Ni65Fe35 = 3 ~ 6

III. Low CTE Metal Filling for Glass Substrate

- **Filling Behavior of Ni Alloys**

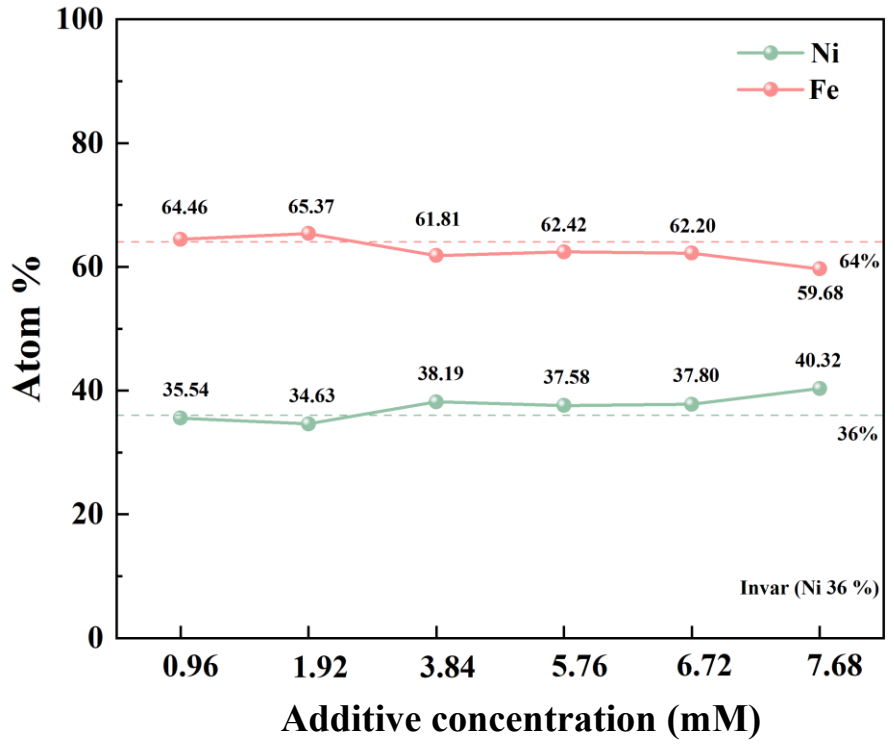




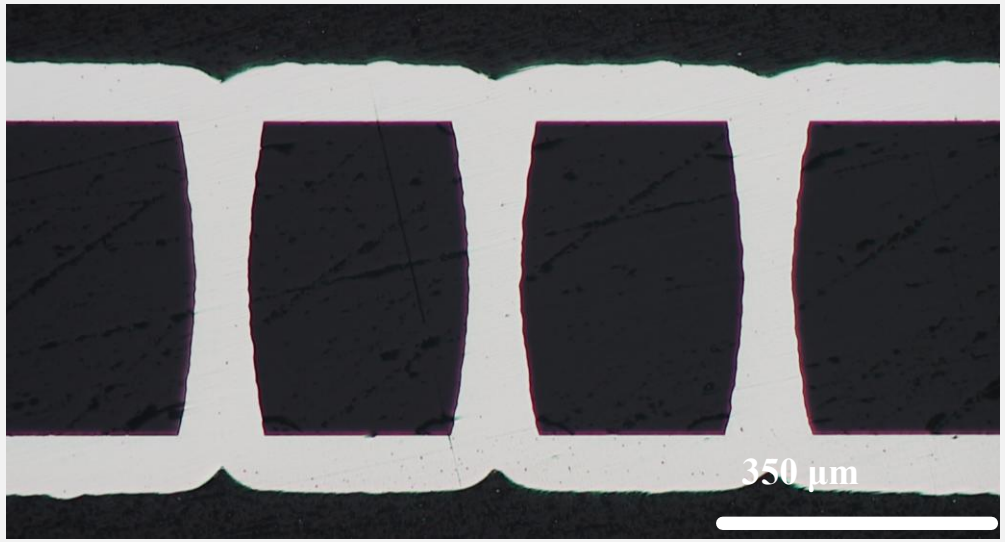
Ni 0.6 M
Fe 0.6 M

III. Low CTE Metal Filling for Glass Substrate

deposition time: 12h



✓**Alloy composition remains within a narrow range across different additive concentrations.**



Properties of Ni-Fe alloy

Alloy Properties	Electroplated Ni-Fe Alloy
Composition (Atom%)	37.58% Ni, 62.42% Fe
CTE (10^{-6}, K^{-1})	7.27
Glass Wafer CTE (10^{-6}, K^{-1})	7.2
Electrical Resistivity (Ωm)	2.37×10^{-7}
Internal Stress (MPa)	42.56

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