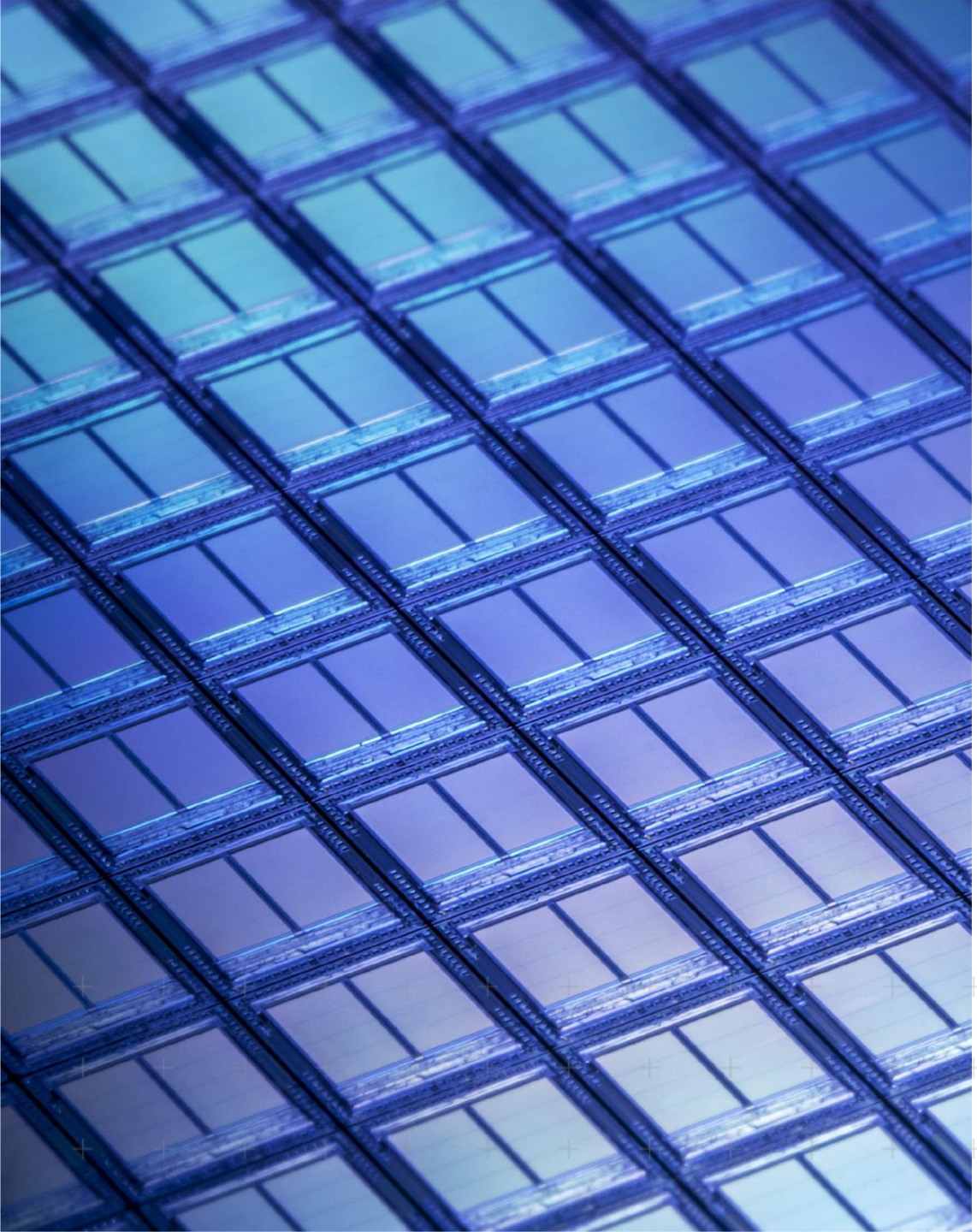


Implications on Wafer Processing of the move from Pluggable to Co-Packaged Optics

Dave Thomas

Vice President, SPTS Product Management

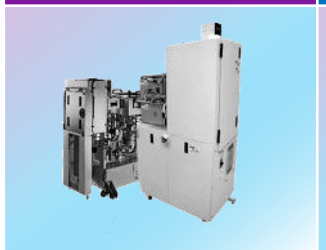
27 June 2025

Contents

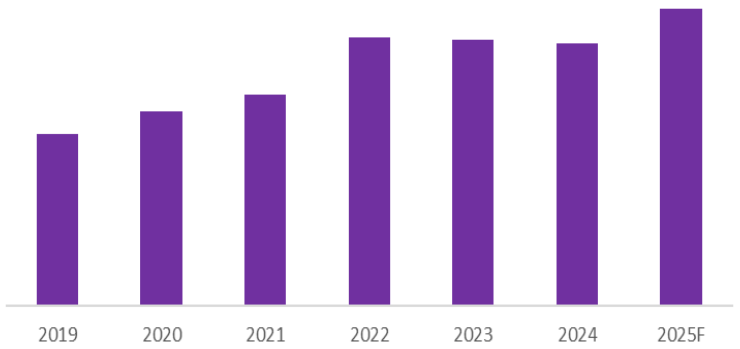
SPTS Introduction

KLA UK/'SPTS Division'

Product Portfolio

Plasma Etch **SPTS Omega®**	Plasma Dicing **SPTS Mosaic™**
	
Vapor Release Etch **Primaxx® & Xactix®**	PVD **SPTS Sigma®**
	
PECVD **SPTS Delta™ SPTS Osprey®**	Molecular Vapor Deposition **SPTS MVD**
	

Revenue Trend



Strong Revenue Growth

Markets & Customers

Fast growing, diverse

- **Advanced Packaging** – Top 5 semi device makers, top 3 OSATs
- **Photonics** – the leading compound semi device makers
- **Power** – 7 of the top 10 device makers
- **RF** – 8 of the top 10 PA device makers
- **MEMS & Sensors** – 95% of the IDMs + Foundries

New Factory – Officially Open

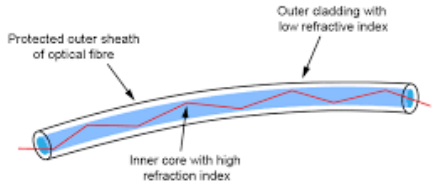
April 2023

April 2024

May 2025

Photonics

Device Types & Applications



Device type	End markets	Wafer type & size	Comments
A. Passive Optical Devices			
Dielectric waveguides	Telecom, Datacom	Si, Glass, 6-8”	Optical interconnect for Visible λ.
Si Photonics (waveguides)	Datacom	Si, SOI, 8-12”	Optical interconnect for IR λ. Data centres, HPC.
Lenses & Diffractives	Phones, Wearables	Si, GaAs, Glass, 6-8”	Cameras/sensing, AR/VR.
B. Active Optical Devices (Optoelectronics)			
LEDs	Displays, Lighting	Sapphire, Si, 6-8”	Displays, automotive, decorative & general lighting.
Edge Emitting LASERs	Telecom, Datacom, Phones	Mainly InP, 3-6”	Long haul, fibre to home, optical interconnect, face recognition.
VCSELs	Phones, automotive	Mainly GaAs, 4-6”	Face recognition, distance sensing, gesture control.
A+B = Co-Packaged Optics			
Heterogeneous integration	**Multiple**	**Si, 8-12”**	**Active chiplets or layers on SiPho substrates.**

Telecom

Datacom

Automotive

Lighting

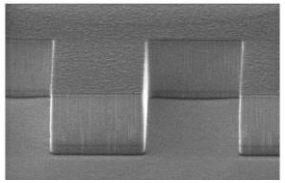
Consumer

Photonics

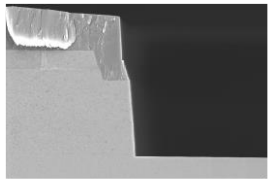
Discrete Devices

Etching for Discrete Photonics

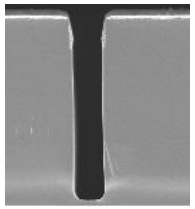
Planar Waveguides



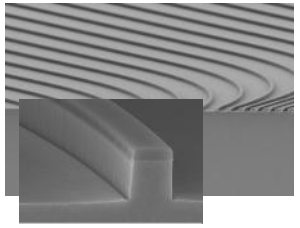
Ge doped core etch
~6µm deep



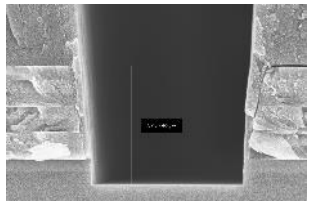
SiOx
10µm deep



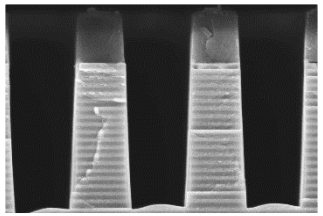
SiOx
28µm deep



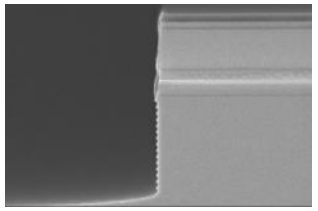
Si waveguide
1.2µm deep



SiO_2/Nb_2O_5 … x4
1.8µm deep

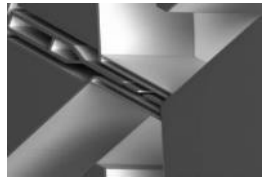


Nb_2O_5/SiO_2 etch …x19
~4µm deep



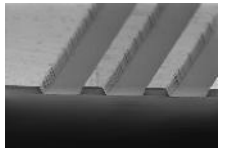
Ox/Si/Ox/Si waveguide
~5µm deep

Optical MEMS

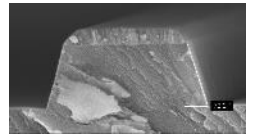


Deep Si etching

Modulators

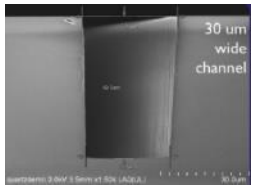


$LiNbO_3$ etch
5µm deep



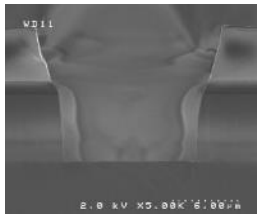
$LiNbO_3$ etch
0.35µm deep

Bio-Photonics

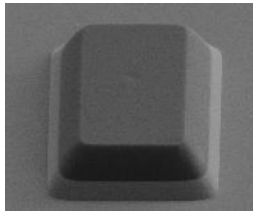


Glass etch
50µm deep

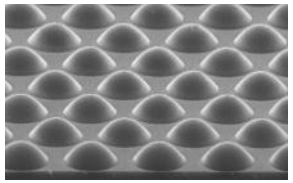
LEDs



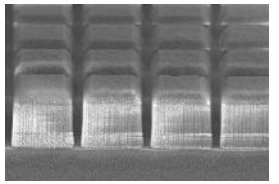
GaN or GaP etch
~6µm deep



GaN etch
~1.3µm deep

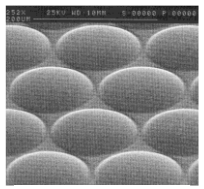


Sapphire etch
~1-2µm deep

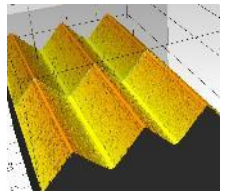


µLEDs
~1.7µm deep

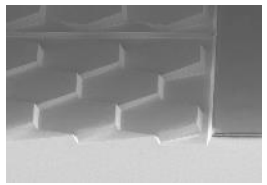
Wafer Level Lenses



Glass etch
25µm diam



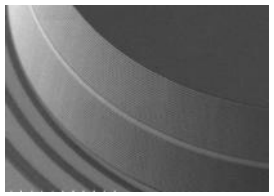
Glass etch
~4µm deep



GaAs etch
4µm deep

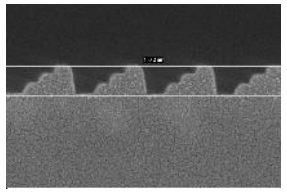
LASERs

InP or GaAs etch
2-5µm deep

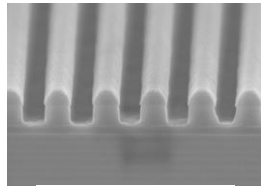


VCSEL etch
2-12µm deep

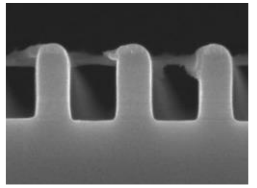
Diffractive Devices



SiN etch
~0.15µm deep



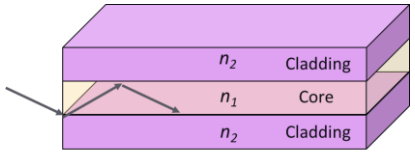
GaAs etch
~0.5µm deep



TiO_2 etch
~0.25µm deep

Si etch
~60µm deep

CVD for Passive Photonics

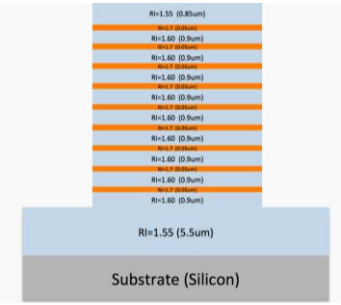


$n_1 > n_2$ for total internal reflection

Planar Waveguides (Visible λ)

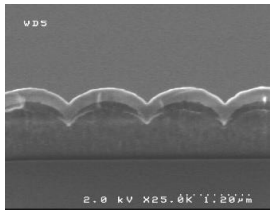
- **Core layer deposition**
  - WIW & WTW RI control
  - Low compressive stress
- Ge doped oxide
  - 6-8µm thick
- SiO_xN_y
  - 6-14µm thick
  - NH_3-free for low optical loss
  - Single or multi-layer

	Ge-Doped Core As deposited	Ge-Doped Core Post anneal
Deposition(um)	7.5052	7.1171
Substrate	150mm Si	150mm Si
Deposition rate	0.458	0.434
WIW thickness non-uniformity	0.66	1.01
WTW thickness non-uniformity	0.26	0.21
Refratctive Index(RI)	1.45842	1.46326
WIW RI non-uniformity	±0.0001	±0.0001
WTW RI non-uniformity	±0.00004	±0.00005
Stress on Si substrate without annealing	-34	-219
Plasma Clean Frequency	7um	7um



Lenses

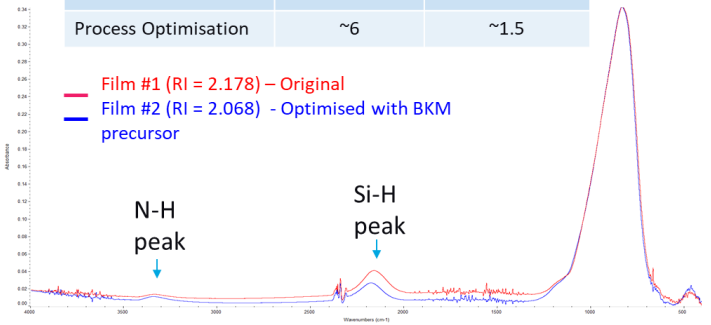
- LT TEOS ARC



Planar Waveguides (Infra-red λ)

- Best optical transmission = lowest H in SiNx
- LPCVD achieves this but needs ~800°C
- PECVD SiNx naturally contains more H
  - SiH_4/NH_3 or $SiH_4/N_2/H_2$ common precursors
  - Move to alternative precursors
- [H] characterised through FTIR
- Better is to measure optical loss

Film	Si-H peak area/thickness	N-H peak area/thickness
Previous BKM	~10	~1
Process Optimisation	~6	~1.5

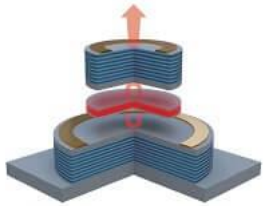


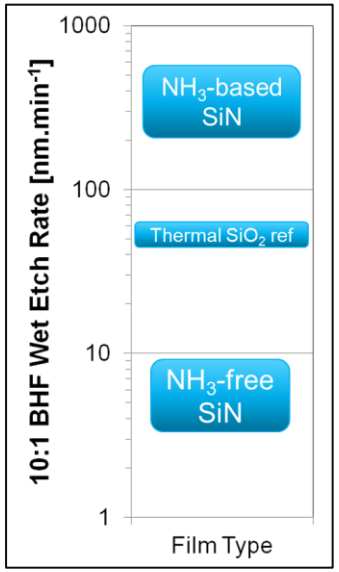
FTIR Spectroscopy for PECVD SiN

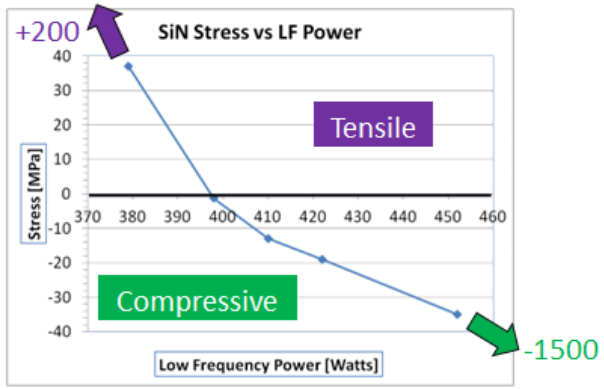
CVD for Active Photonics

VCSELs (GaAs)

- SiN or SiO ARC layers
- SiN stress/bow compensation
- Hard-masks
- SiN final passivation

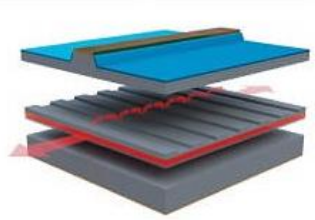


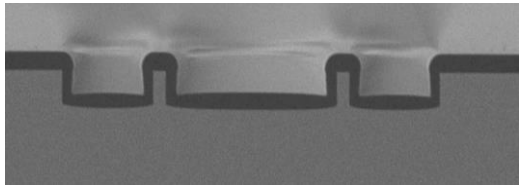


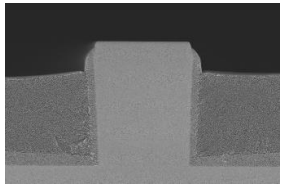


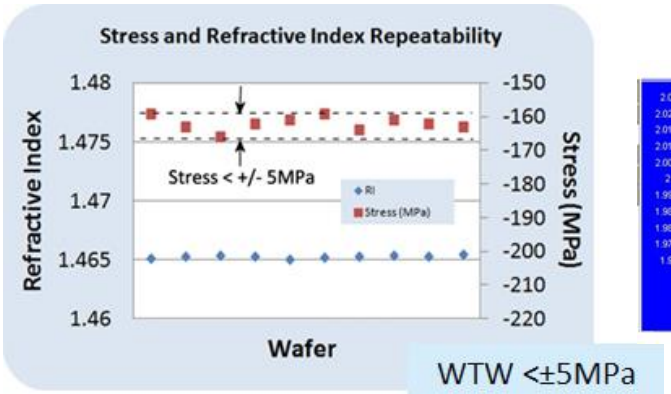
EELs (InP)

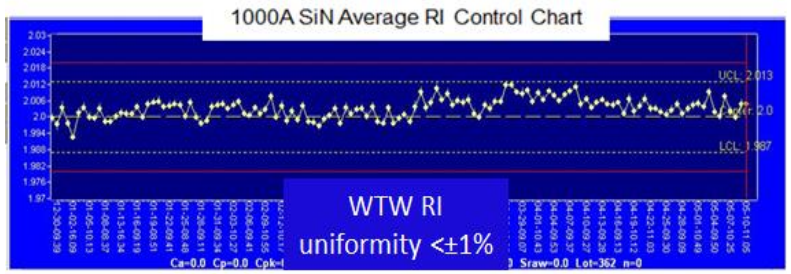
- SiN/SiO stack for Ridge coverage
- Stress control
- Hard-masks
- SiN final passivation







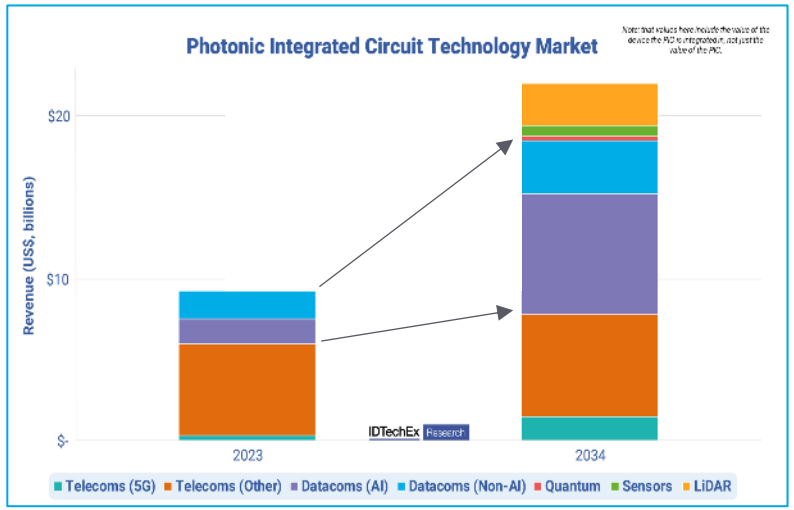


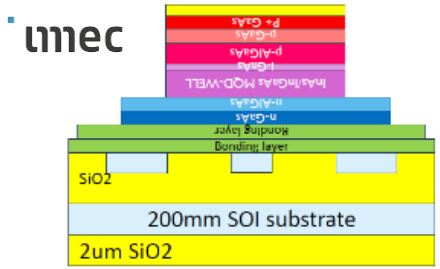


Photonics

LASERs

- Telecom & Datacom are main markets
  - VCSELs mainly smartphones (face & proximity) today → 50% Datacom by 2027
  - InP EELs mainly Telecom today (long haul) → 65% Datacom by 2027
- Coherent & Lumentum are key players
  - Both reporting weak demand for Telecom & high demand for Datacom (AI driver)
  - Both optimistic/positive in earnings calls
- Larger wafers
  - IQE's first GaAs on Si VCSEL wafer at 8"
  - imec's GaAs EEL on 200mm SOI
  - Improves manufacturability
  - Allows SiPho, compound & CMOS integration





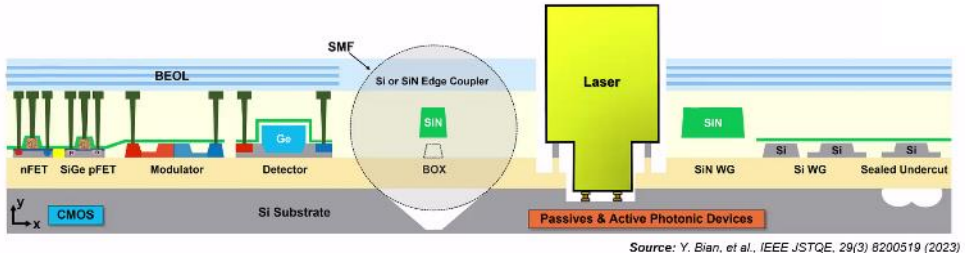
Source:Yole 2024, IDTechEx 2024

Photonics

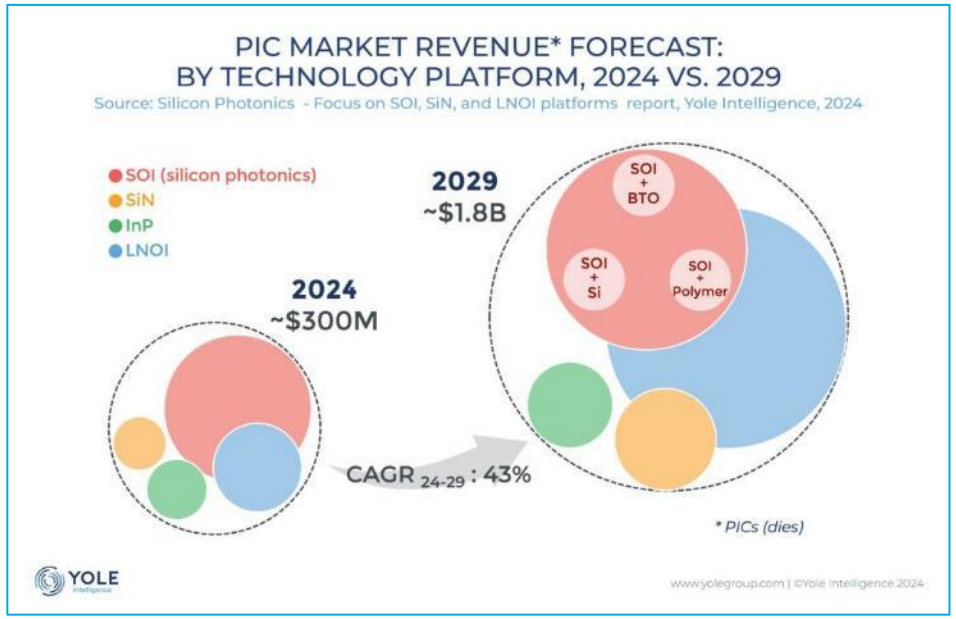
Heterogeneous Integration/Co-Packaging

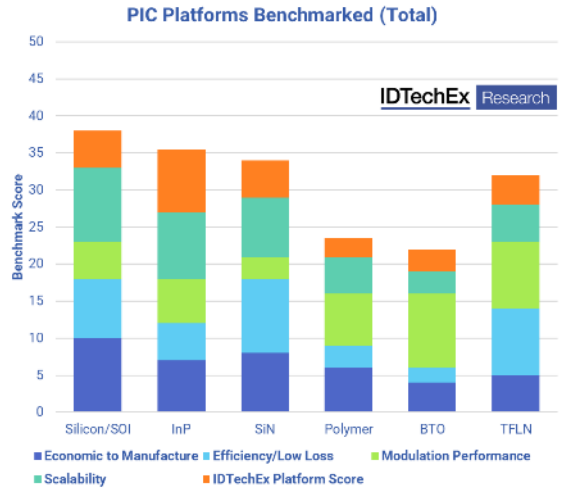
Co-Packaged Optics Market

- Optical transceiver market $10.5B in 2022 → $24.6B in 2027
- Data Centres need short range, high speed, low power, connections
- InP or GaAs needed for the optical engine
- KLA engaging with key players
- Emerging requirements
  - Low loss SiNx CVD waveguides
  - Si micro-machining & TSVs
  - Fiber couplers & lenses
  - CVD bonding dielectrics
  - 300mm Compound Semi processing
  - 2.5D interposer ‘packaging’
- Emerging material type is $LiNbO_3$
  - Low optical loss, high bandwidth



Source: Y. Bian, et al., IEEE JSTQE, 29(3) 8200519 (2023)

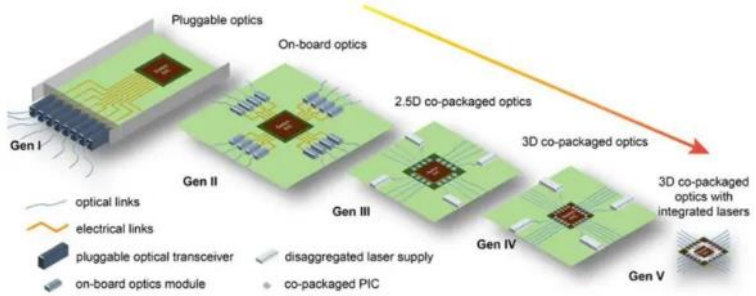


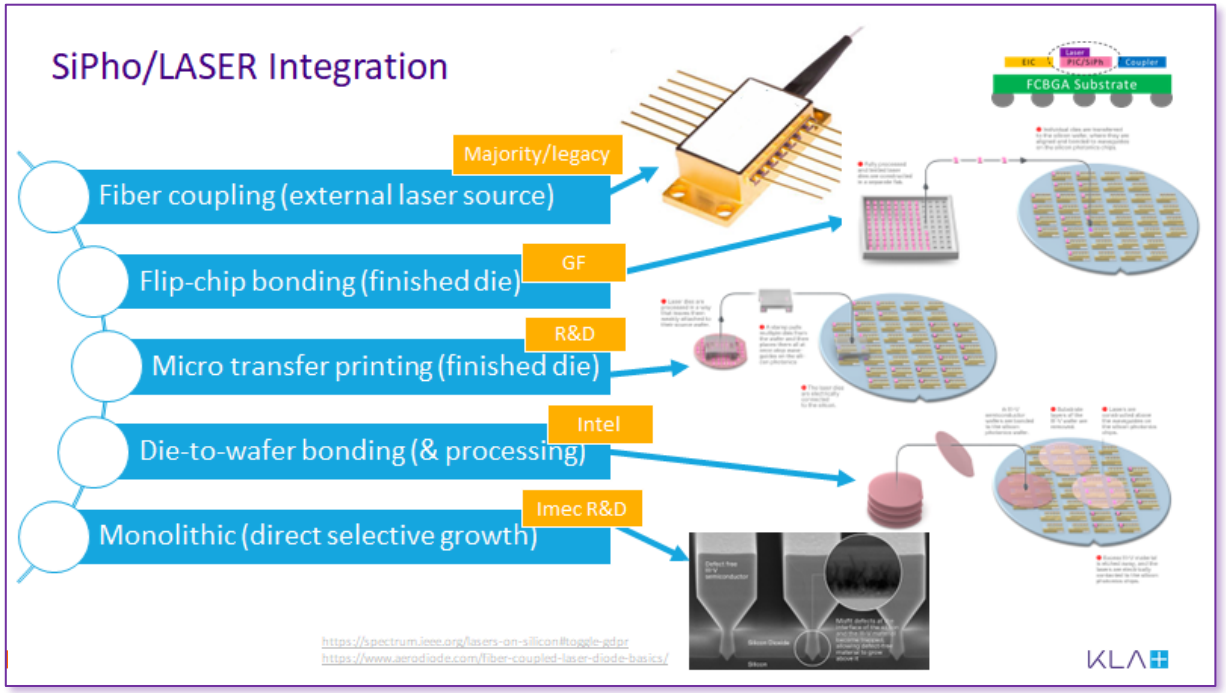


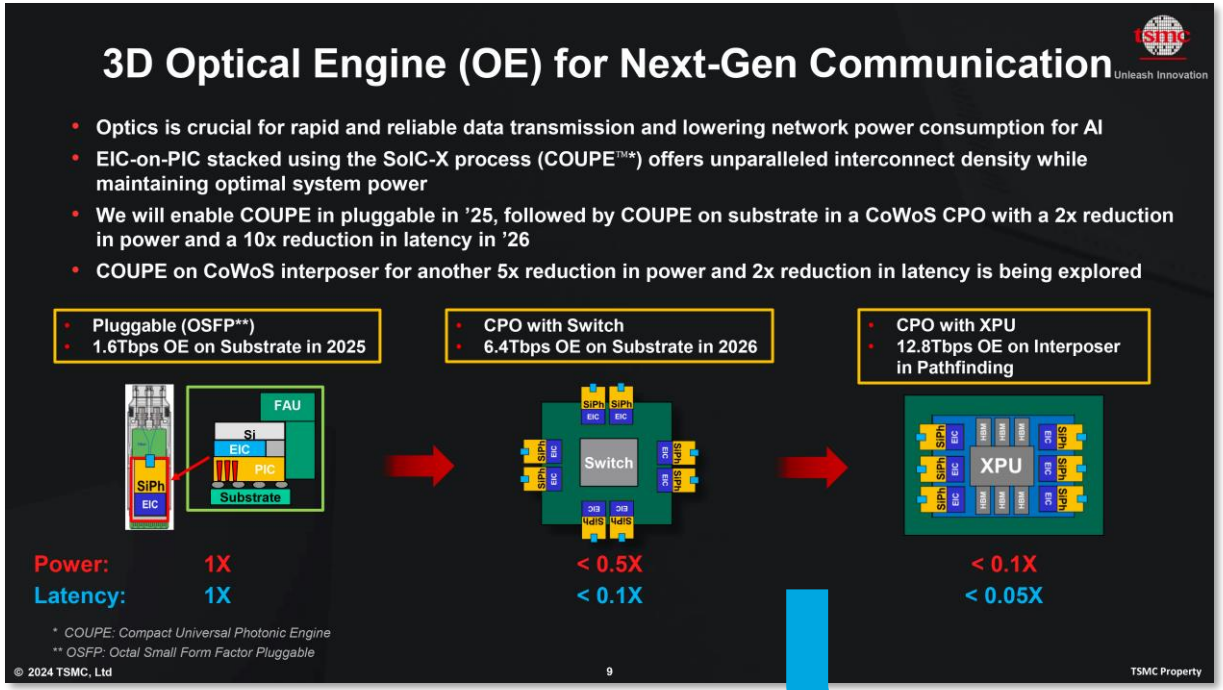
Structure of a Lithium Niobate Thin Film with Silicon Substrate and SiO2 Isolation Layer

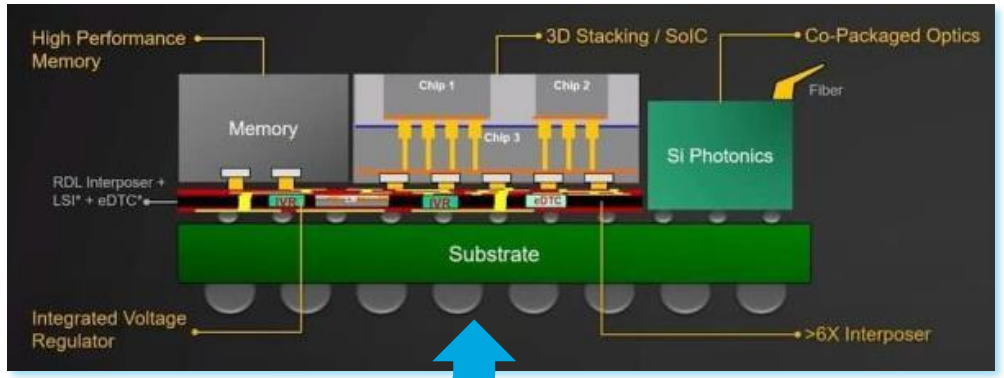
Sources: Yole at PIC 2023, IDTech 2024 & IEEE 2023

Integration Methods







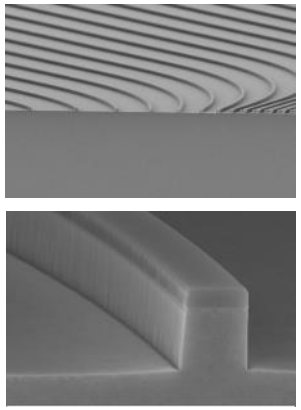


Source: AnandTech April 2024

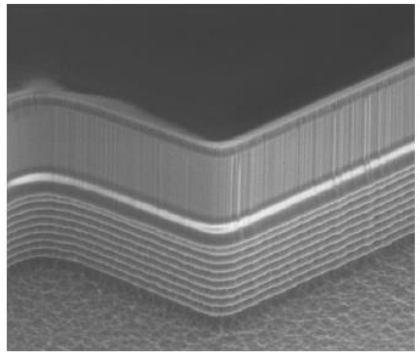
Co-Packaged Optics – Early Examples

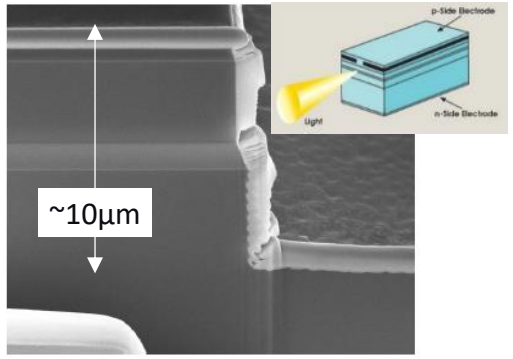
200mm Wafers

Deep multi-layer w/g



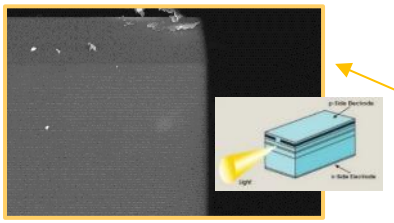
Si waveguides
~1µm deep



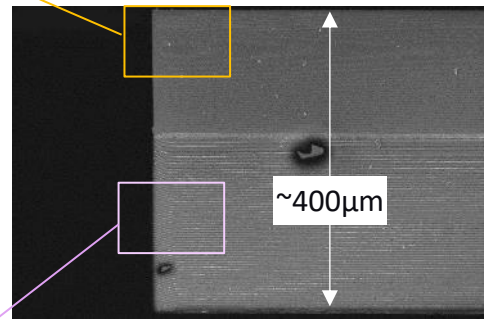


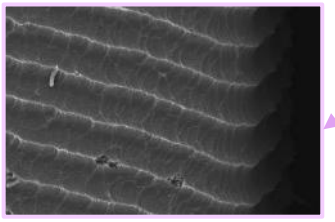
Die to wafer bonding (Si & InP)

Plasma Dicing



Si waveguide
(100nm scallops)



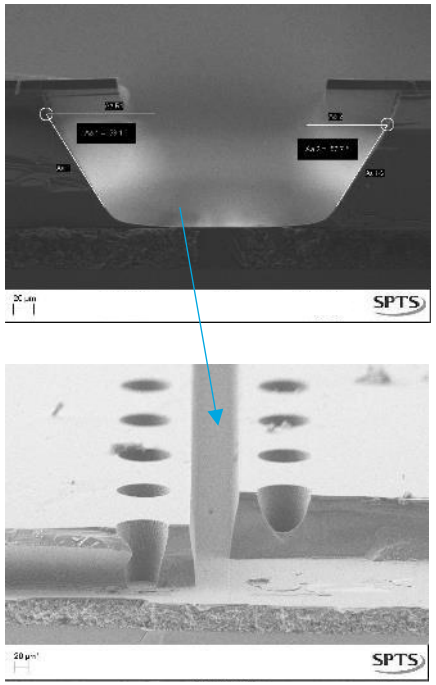


Si base
(2µm scallops)

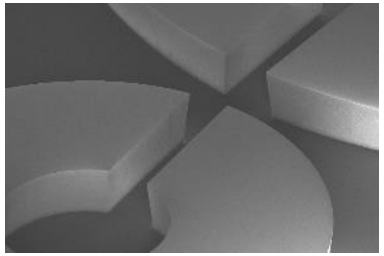
Die to Die bonding (Si & InP)

Co-Packaged Optics – The Role of Si Micromachining?

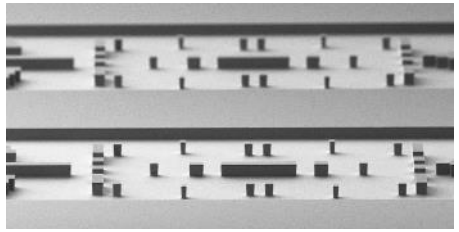
Trenches

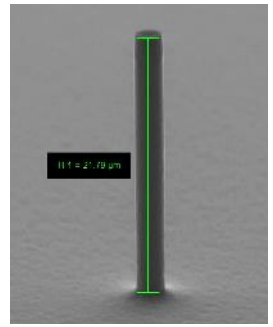


Cavities

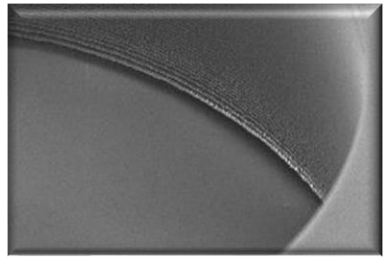


Annular

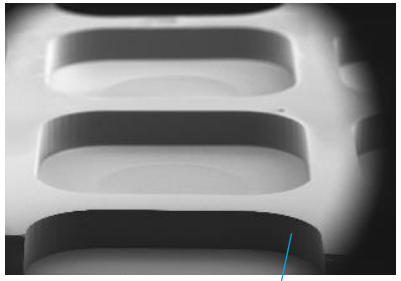


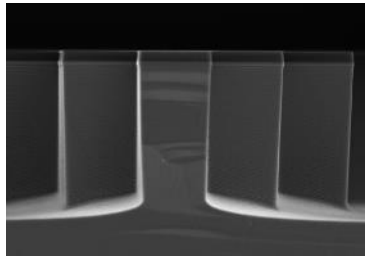


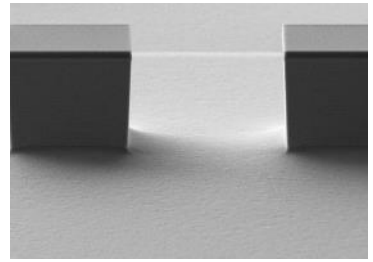
22µm deep Pillar



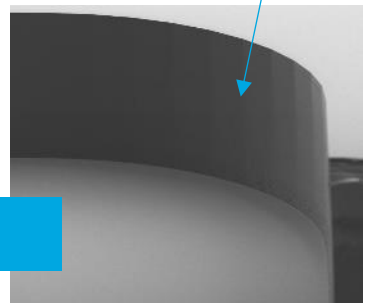
400µm diam Circular



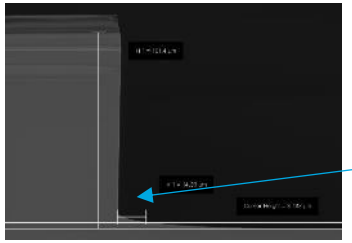


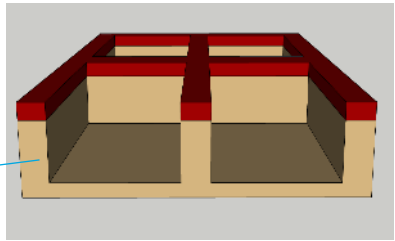


Rectangular



500µm deep

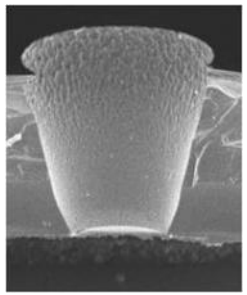




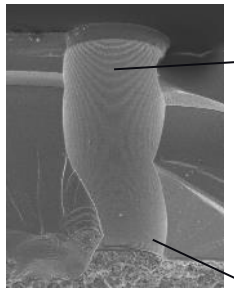
Fiber alignment & die placement/manipulation

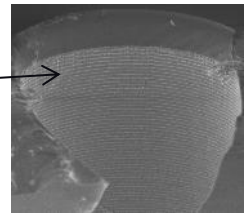
Co-Packaged Optics – The Role of TSVs?

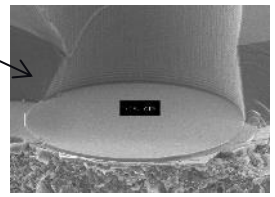
Via Last (Macro)



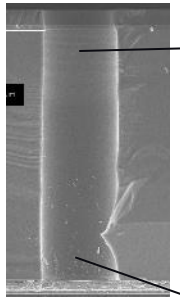
Top ~85µm
Base ~47µm
Profile ~77°

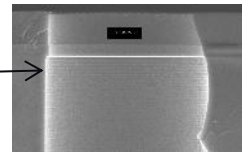




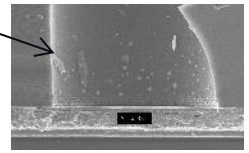


75 x 150µm
Sc ~200nm
Profile ≤91°





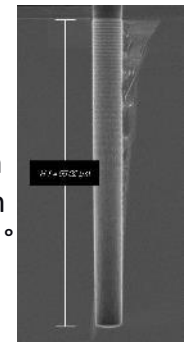
20 x 80µm
Sc ~100nm
Profile ~90°



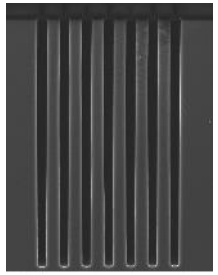
Apparent wall curvature due to cleave

Via Middle

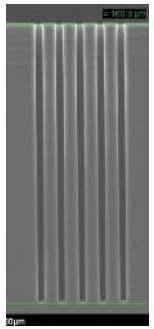
10 x 100µm
Sc ~70nm
Profile 90°



5 x 55µm
Sc ~70nm
Profile 90°

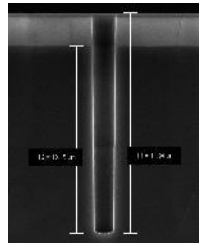


8 x 180µm
Sc <200nm

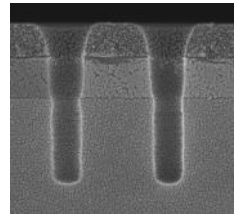


4 x 160µm
Sc <50nm

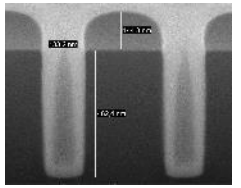
Micro & Nano



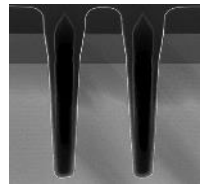
1 x 10µm
Sc ~0nm



120 x 350nm
Sc ~0nm



0.13 x 0.5µm
Sc ~0nm



90 x 300nm
Sc ~0nm

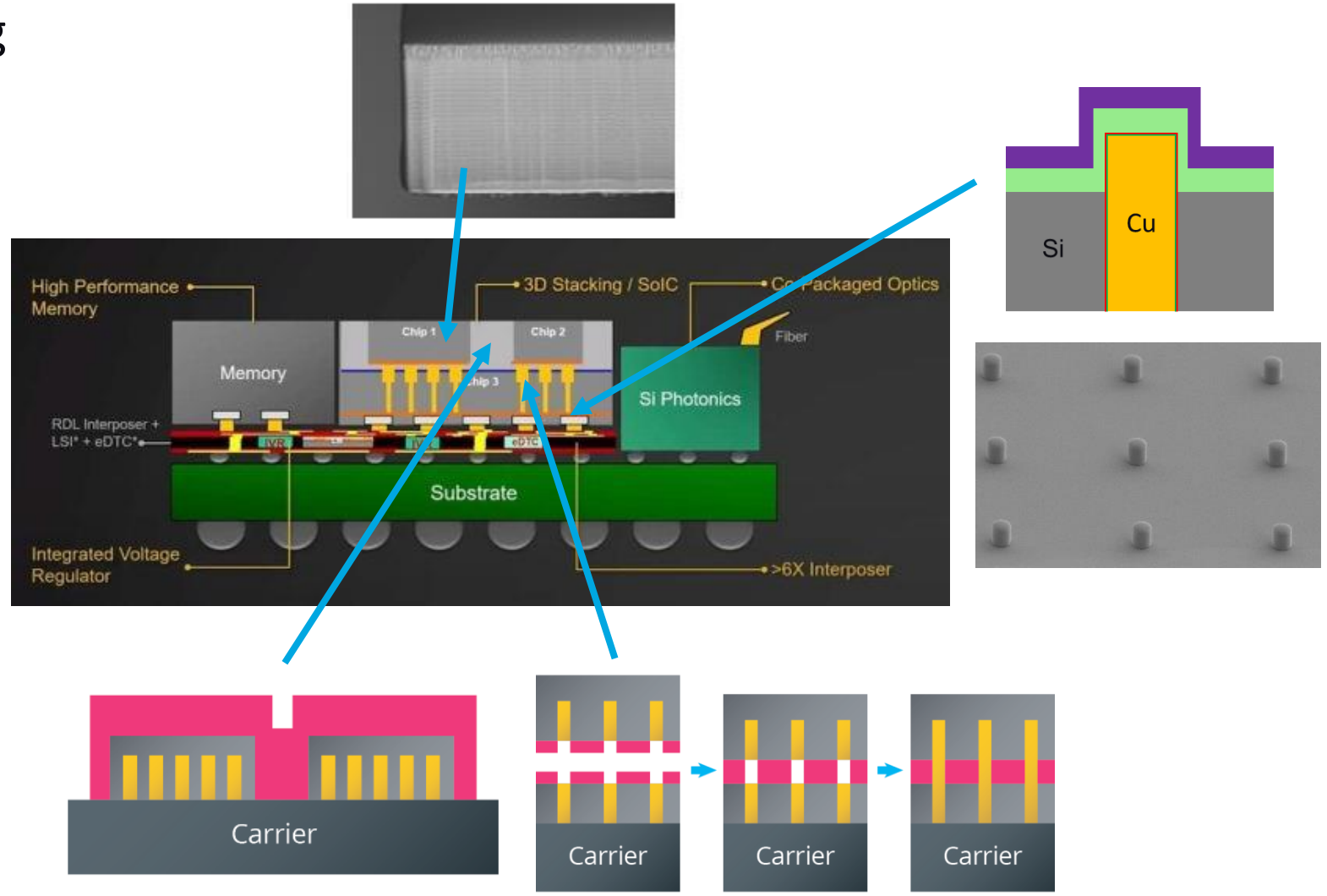
Continuous process
SF_6 + passivant

Switched (Bosch) process
SF_6/C_4F_8 cycling

Co-Packaged Optics – The Role of TCB & HB?

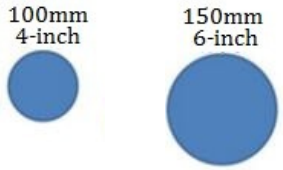
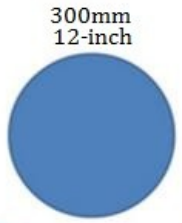
- Thermo-compression bonding
  - Via Reveal Etch
  - Via Reveal CVD*
  - UBM metals for RDL
- Hybrid Bonding
  - Plasma Dicing
  - Bond layer SiCN CVD* (BonDi)
  - Inter-die TEOS gap-fill CVD* (Di-Fill)
  - PVD for RDL
- Package
  - PVD for heat-sink layers

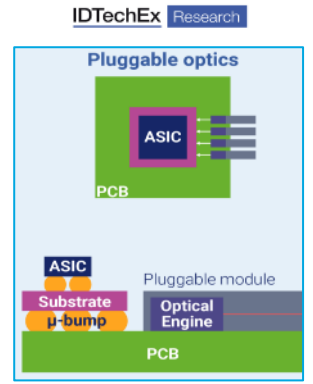
* Low temperature CVD (125-250°C)

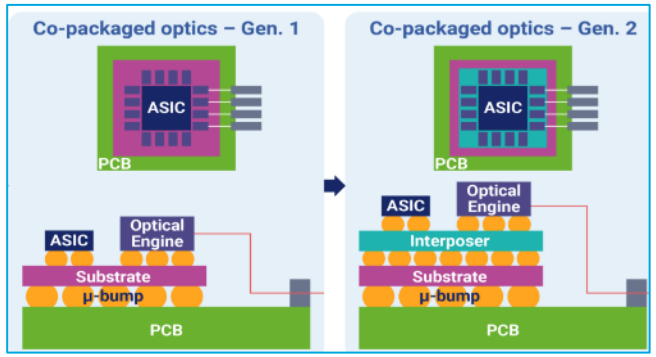


Supply Chain Observations

Dissimilar Companies & Technologies

	Discrete Photonics (Optically active)	+	Si Photonics (Optically passive)	+	Advanced Packaging	=	Heterogenous Integration & Co-Packaging
• Wafer type	InP, GaAs, GaN, LNO		Si, SiNx		Molded die, Si, Glass		
• Wafer size							
• Example companies	eg. Coherent, Lumentum …		eg. GF, Intel, Samsung, TSMC, TowerJazz, imec, FhG …		eg. Amkor, ASE, JCET, TSMC …		
• Competencies	Optoelectronics Compound layers		Waveguides Si-based layers		Wafer-level packaging Si-based chips/layers		
• Company size (Revenue/year)	~$2-6B		~$2-130B Up to 65x		~$5-130B Up to 65x		





Pluggable ⟷ ‘Normal’ supply chain ⟷

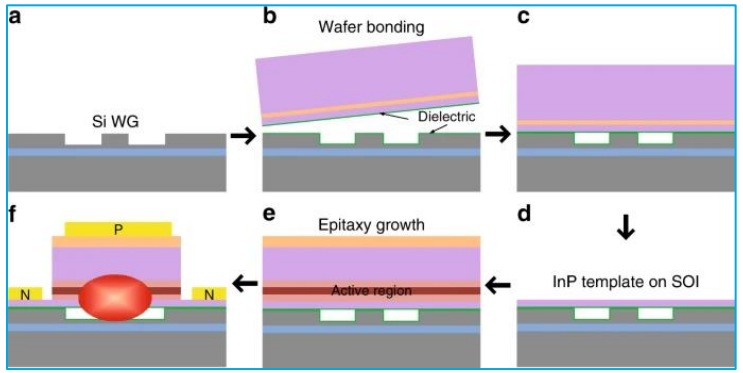
CPO → Greater technical co-working → Optoelectronics/compound semi know-how

Processes Required at 300mm

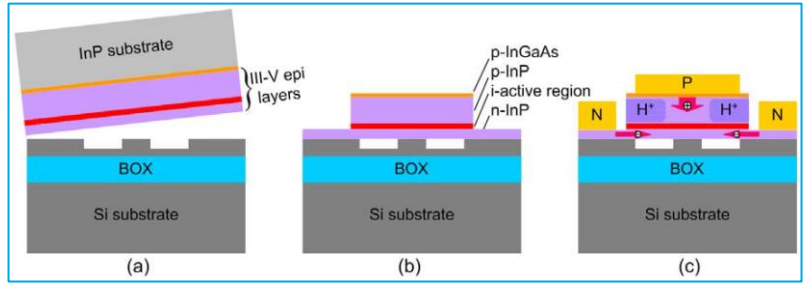
Outside of Typical AP Steps

- CPO requires
  - Emitters, modulators, detectors, waveguides, couplers …
- CVD
  - Waveguides - SiO, SiN, α-Si & doping
  - Bow compensation*
  - Anti-reflection coatings*
  - Hard-masks
- PVD
  - p-side & n-side contacts*
  - Stress control
  - Step coverage
  - Optical films*
- Etch
  - SiN/SiO etching for waveguides & hard-masks
  - Si etching for cavities & TSVs*
  - Metal oxides eg. TiO, NbO & LNO*
  - Compound layer etching – InP, GaAs/AlGaAs, GaN ….*
  - Lenses & optical couplers*

* new/emerging requirements



Source: Nature 2019



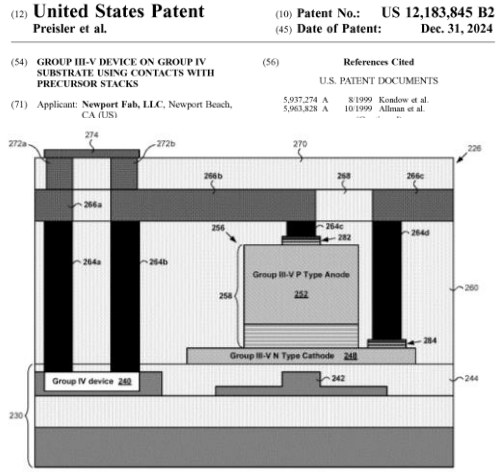
Source: Semiconductor Science & Information Devices 2019

Summary

- CPO market is rapidly emerging to address connectivity for AI Data Centres
- Pluggable options exist today
  - Established supply chain
  - ‘Partitioned’ or ‘segregated’ technical competences/know-how
- Full heterogeneous integration means …
  - Fabs processing materials they are not familiar with
  - Technology sharing, licensing, M&A, ground up development ….
- Diverse mix of applications required for integration
  - New Si-based processes …. Waveguides, cavities, TSVs, via reveal, bonding layers, plasma dicing ….
  - New compound layer processes …. GaAs, InP, GaN, LNO ….
- Nvidia announced SpectrumX CPO network switch
  - ‘Joint inventions & collaborations with TSMC, SPIL, Coherent, Lumentum ….’
- TowerJazz named Coherent as JDP partner for their 1.6Tb/s optical transceivers

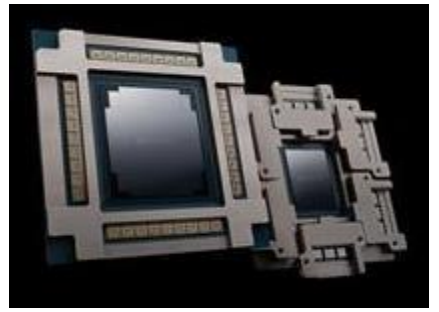
SAMSUNG

Source: Samsung June 2024



TOWERJAZZ

Source: TowerJazz Dec 2024



NVIDIA

Source: Nvidia March 2025

KLA