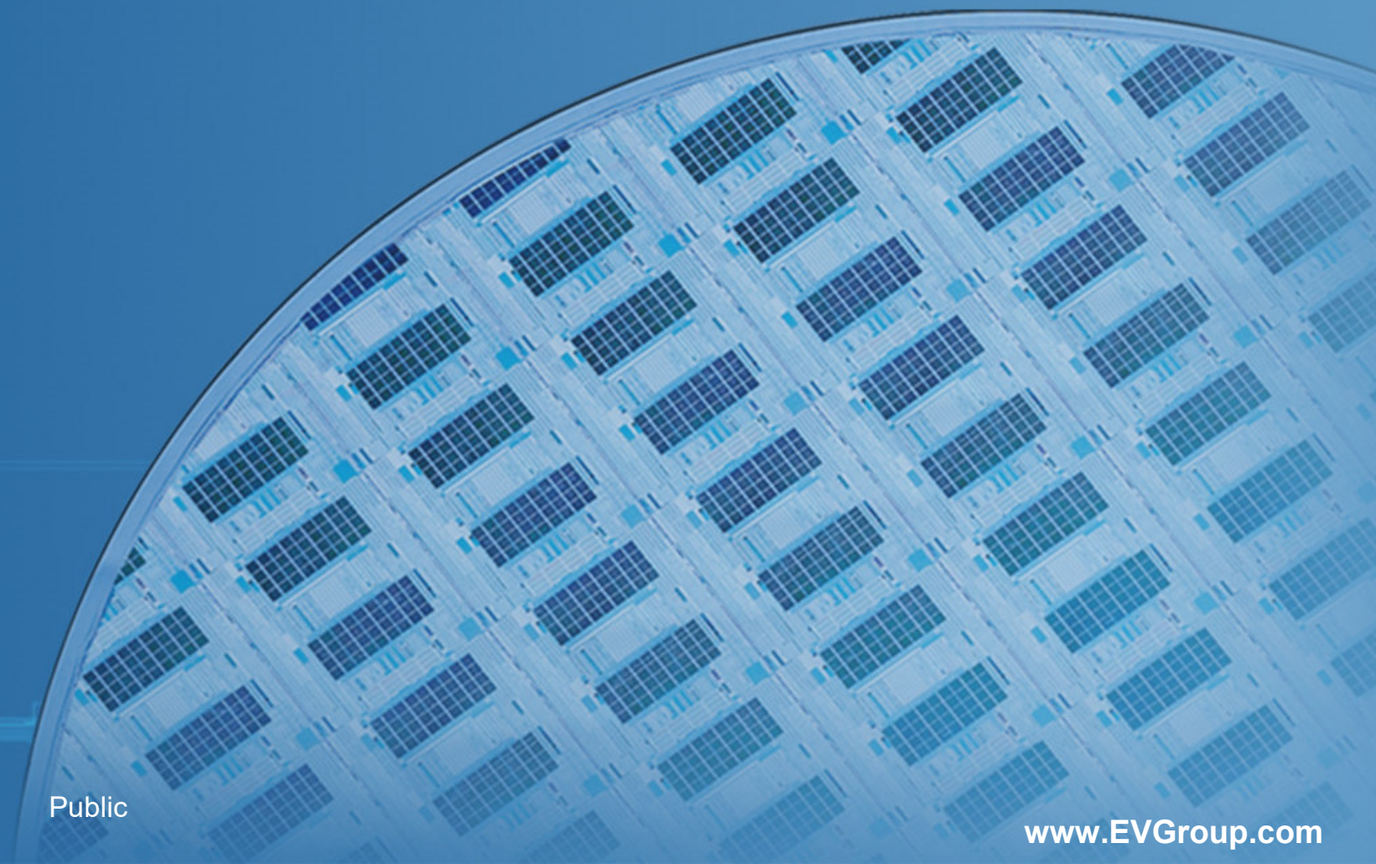
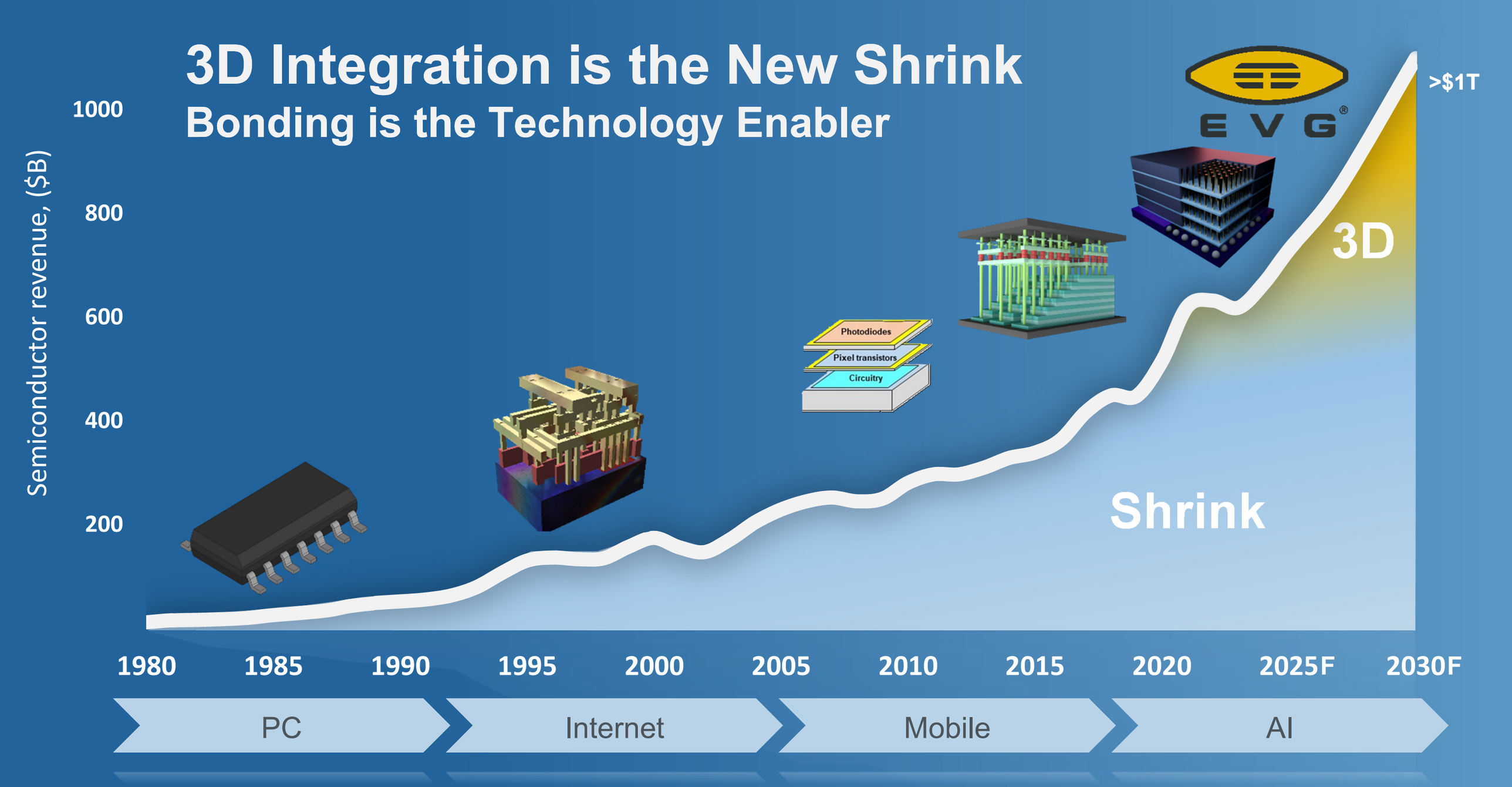
Fusion & Hybrid Bonding: Trends, Challenges and Prospects

Markus Wimplinger
Corporate Technology Development & IP Director



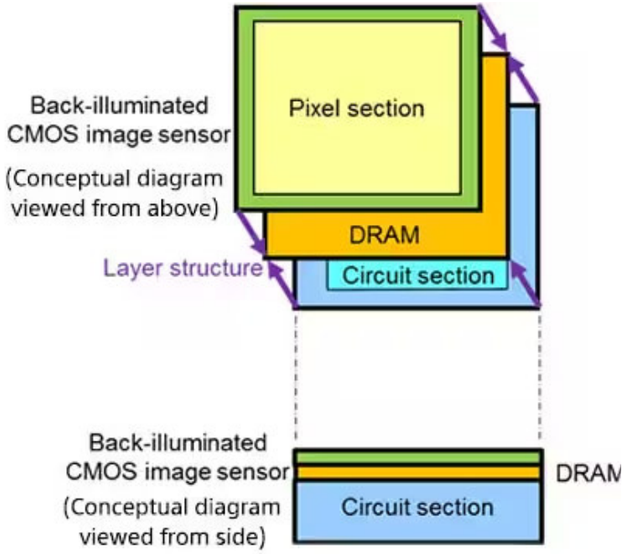
3D Integration is the New Shrink

Bonding is the Technology Enabler

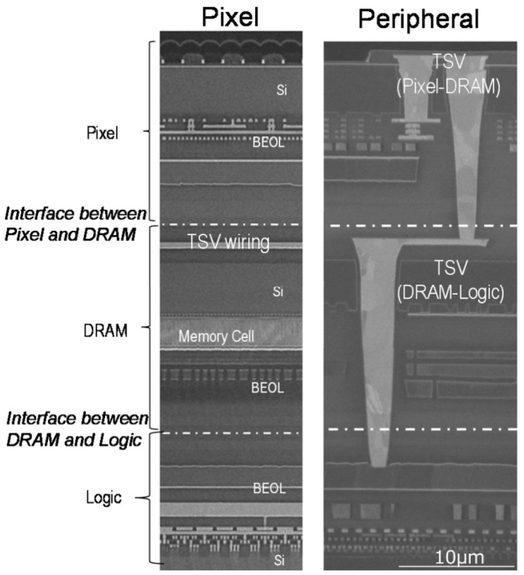


High Volume Manufacturing of Devices using Wafer Bonding for 3D Interconnection

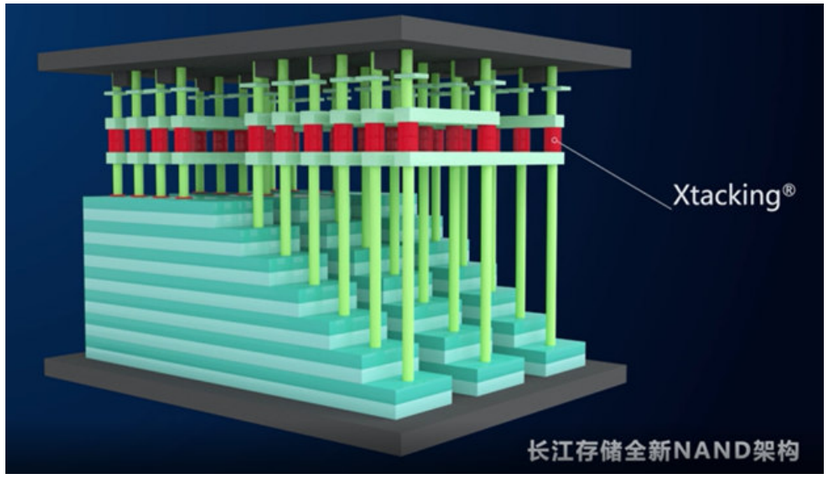
- 2008: Omnivision OV8810 – Backside Illuminated CMOS Image Sensor
- 2012: Sony announced first stacked BSI CIS Sensor
- 2017: Sony announces first 3-layer stacked CIS
- 2018: YMTC announced their Xtacking architecture, which uses hybrid bonding for NAND flash memory manufacturing



Source: SONY



Source: fuse.wikichip.org



Source: TechInsights

3D Integration Addressing Interconnect Challenges

Historical View

- Bandwith
- Latency (R, C)

Today

- Crowding
- Power Consumption
- Clock Delivery
- Voltage Drop
- Thermal Management

Future

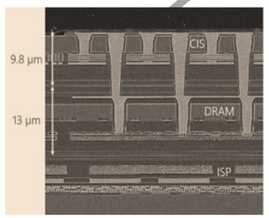
- New Materials
- New Transistor Architectures



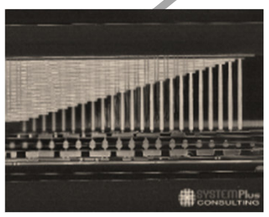
3D Integration is the new „shrink“
Wafer Bonding is the technology enabler

Fusion & Hybrid Bonding I Market Segmentation

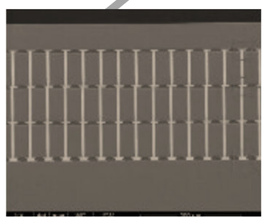
	Backside Illuminated Image Sensor	Memory				Logic			µLED Displays
		3D NAND Flash	HBM Stacks	DDR6+	Next Gen. Memory	SoC Partitioning		Scaling	
Device Stack	Photo Diode + DRAM + Logic	NAND Block + Periphery	12+ layer stacking	Peri under DRAM	Peri on MRAM, FeRAM, PCM	SoIC	SRAM + Logic	Backside PDN (5nm node)	EPI layer + Logic
Bonding Process	W2W	W2W	W2W and/or D2W	W2W	W2W	W2W and/or D2W	W2W	W2W	W2W and/or D2W
	Hybrid	Hybrid	Hybrid	Fusion	Fusion & hybrid	Hybrid	Hybrid	Fusion	Hybrid or fusion
Pitch	2µm → 1µm	2µm → 1µm	5µm → 3µm	2µm → <1µm	2µm → <1µm	9µm → 2µm	2µm	Scanner dependent	2µm → <1µm
Maturity	HVM	HVM	R&D	R&D	R&D	Ramp Up	Ramp Up	Ramp Up	Ramp Up

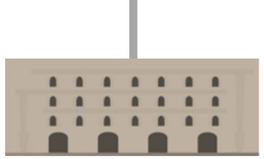


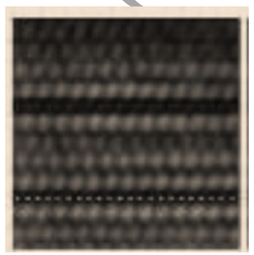
Sony (System+)

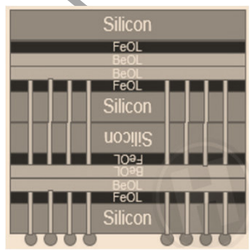


YMTC (System+)


Xperi (ECTC2020)

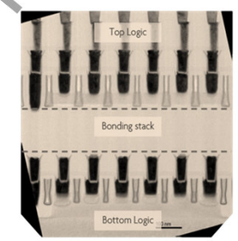

IMEC (PTW21)


IMEC (PTW21)



TSMC WoW SoIC


IMEC Collaboration



IMEC Collaboration

IMEC Logic Roadmap | Potential Bonding Technology Contributions

N7	N5	N3	N2	A14	A10	A7	A5	A3	A2
2018	2020	2022	2024	2026	2028	2030	2032	2034	2036

Continued dimensional scaling

New Backend Materials

Metal Pitch [nm]	40	28	22	21	18	16	16-14	16-12	16-12	16-12

Device and material innovations

Metal Tracks	7	6	6	6	5	5	5	4	<4	<4
	FinFET	FinFET	FinFET	GAA Nanosheet	GAA Nanosheet	GAA Forksheet	GAA Forksheet	CFET	CFET	CFET Atomic

MDI

Bonded CFET

Context-aware interconnect

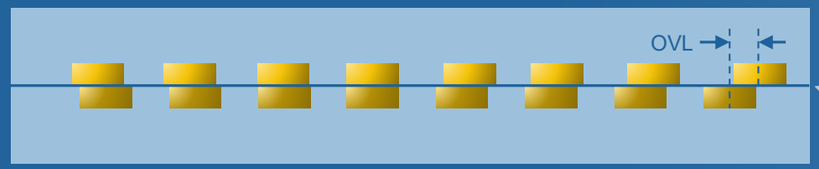




Overlay | Two Independent Metrics

Precision Aligned Bonding (often: Hybrid Bonding)

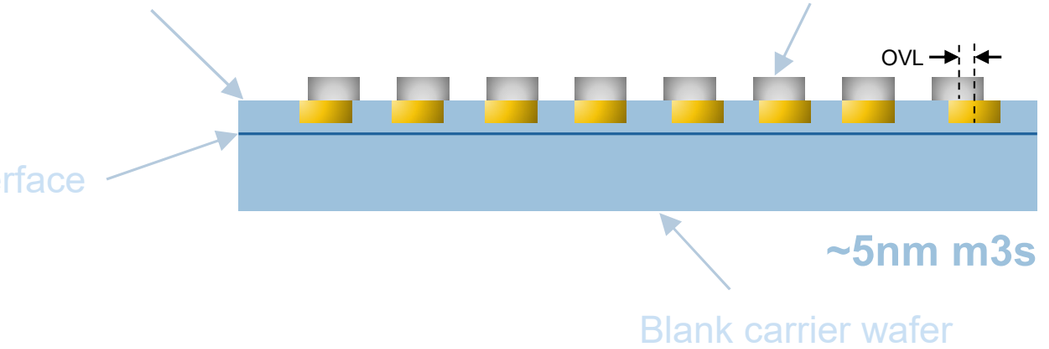
Bonding overlay



~50nm m3s

Edge Aligned Bonding Fusion Bonding

Post bond litho overlay



OVL is “imprinted” during the bonding
Caused by wafer distortion and wafer alignment

Bonding Overlay – Data Analysis

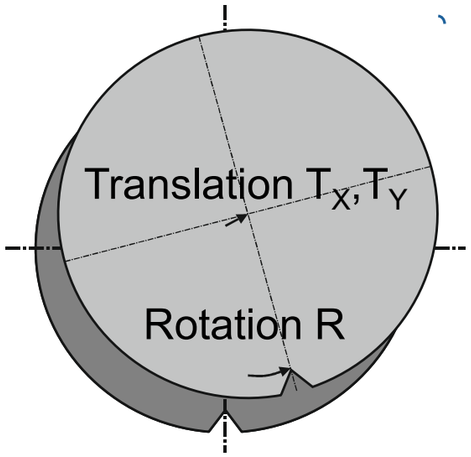
Max Error in fusion bonding

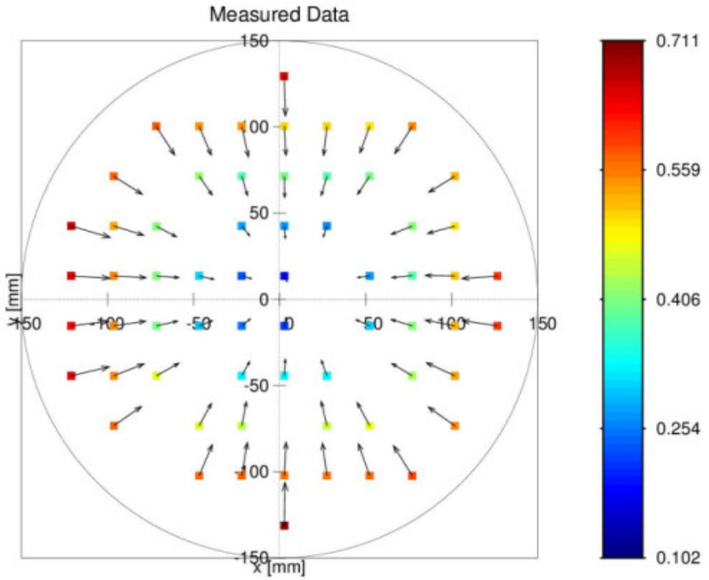
$E_{tot} = E_{alignment} + E_{scaling} + E_{distortion}$

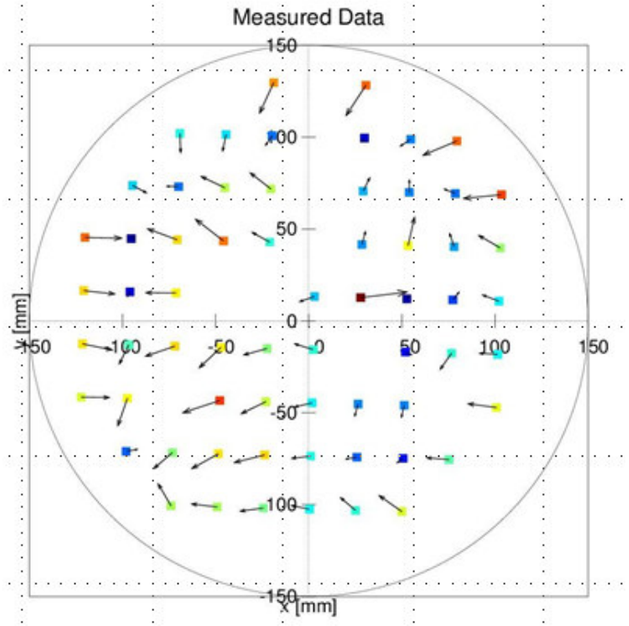
Function of pre-processing, preparation, activation, fusion bonding, etc.
→ ***Function of whole MEOL metallization***

Wafer preparation, tooling and process
→ ***Function of wafer surface and processing***

SmartView alignment capability (W2W)
→ ***Function of the equipment***

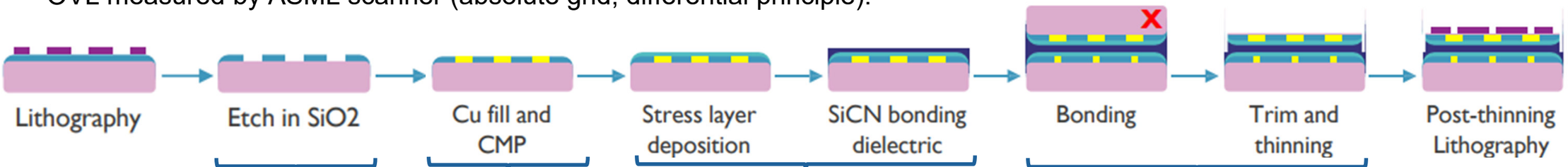




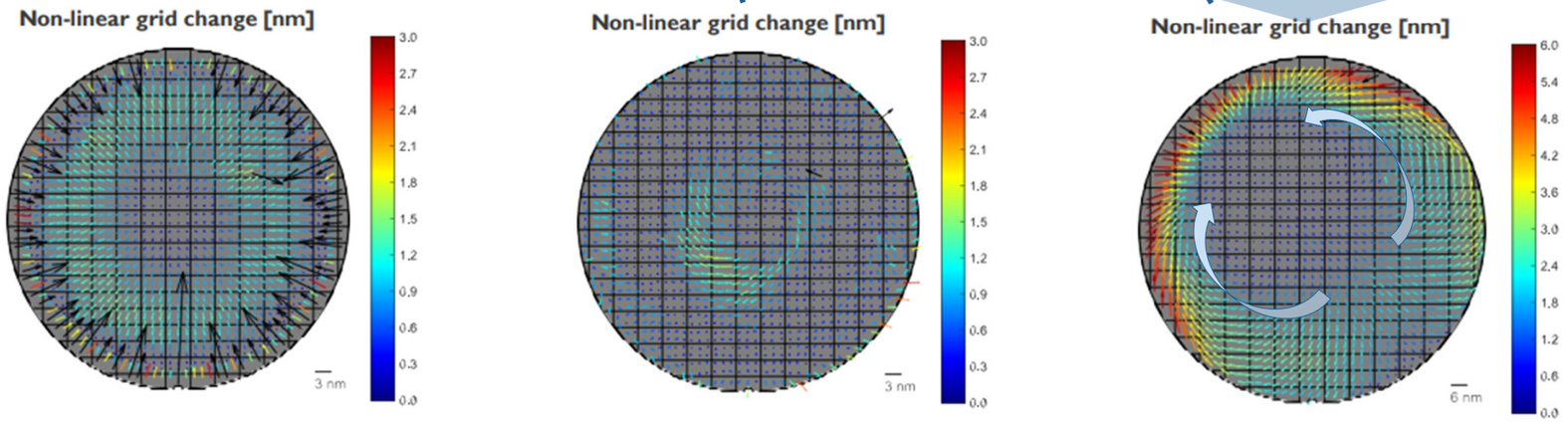


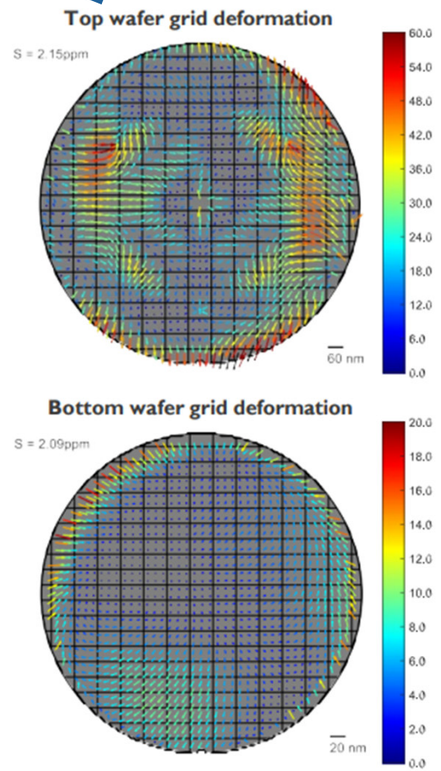
Bonding Overlay Components | Contributors Summary

OVL measured by ASML scanner (absolute grid, differential principle).



Major variation mode





Koen Dhave “Impact of warped wafer-to-wafer bonding on wafer grid and overlay”, PTW 2023 H2

Incoming wafer quality and deposition processes affect clamping and play a significant role in the bonding OVL stability.

Process Optimization | 59nm OVL residuals

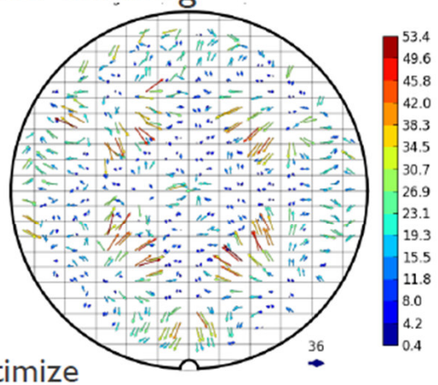
STCE hybrid bonding

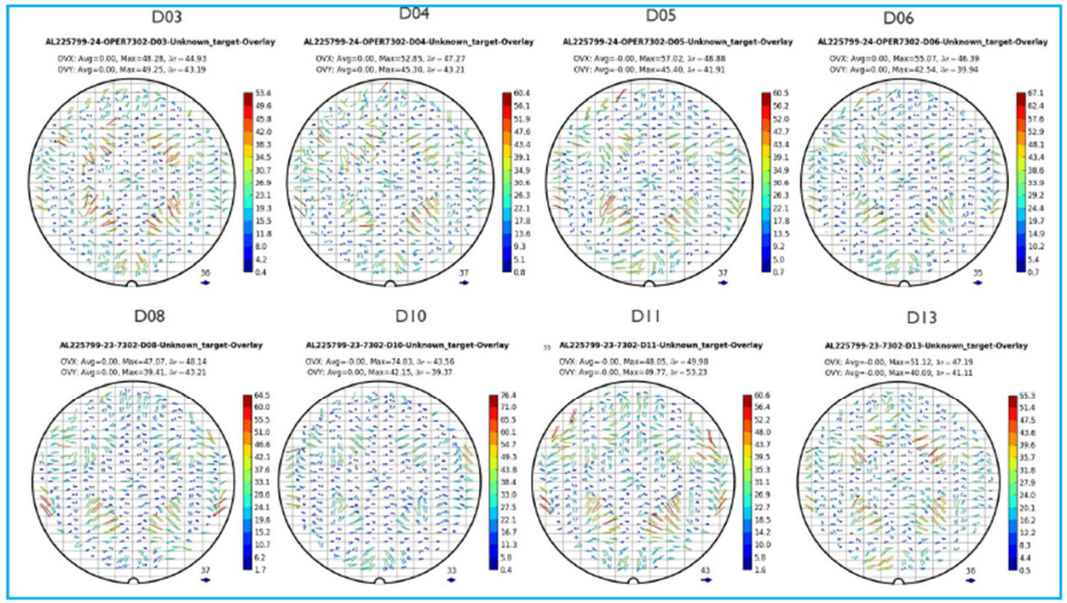
Reproducibility of residual vector length

Overlay measurements after thinning

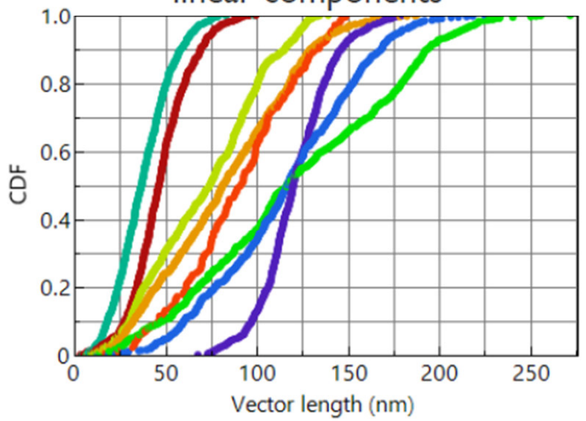
8 STCE wafer pairs

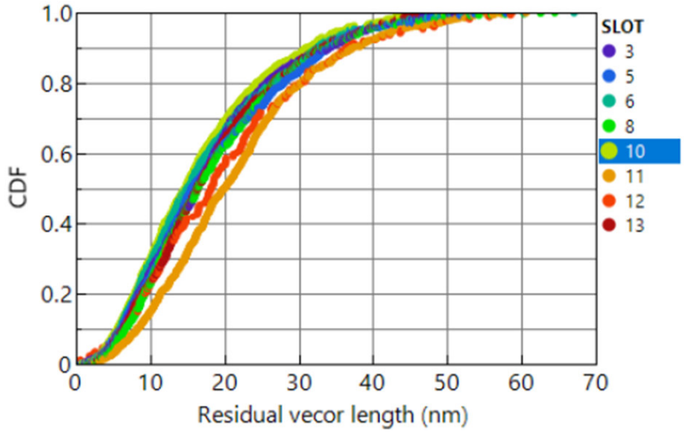
~680 points per wafer measured





Some wafers used to optimize linear components

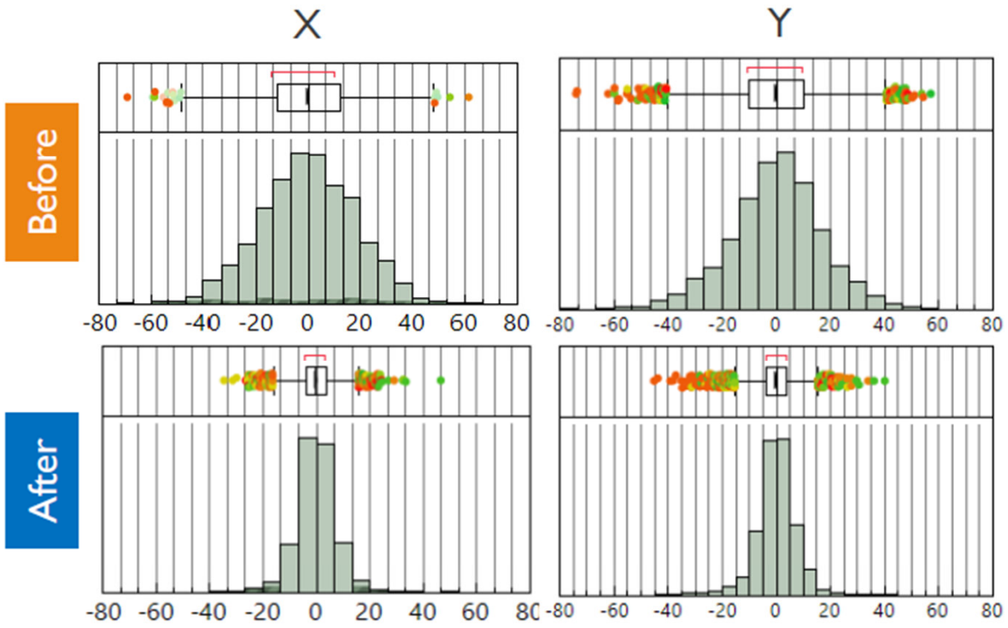




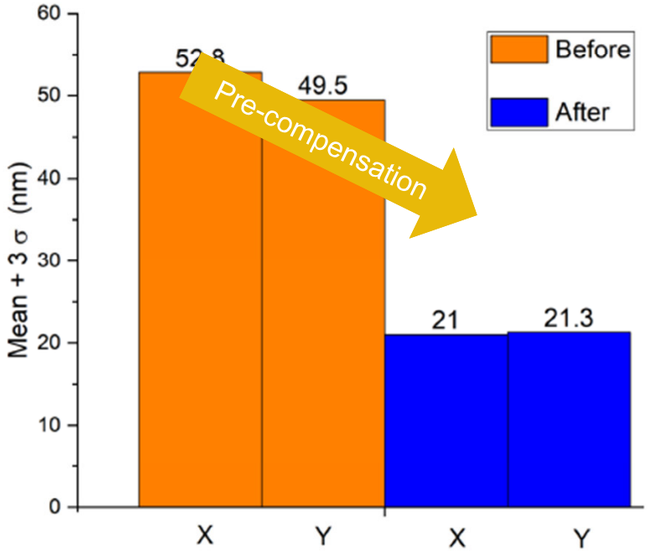
- Residual Pattern is comparable across the different wafer pairs.
- Max residual vector length for 99.5 % of data < 59 nm.

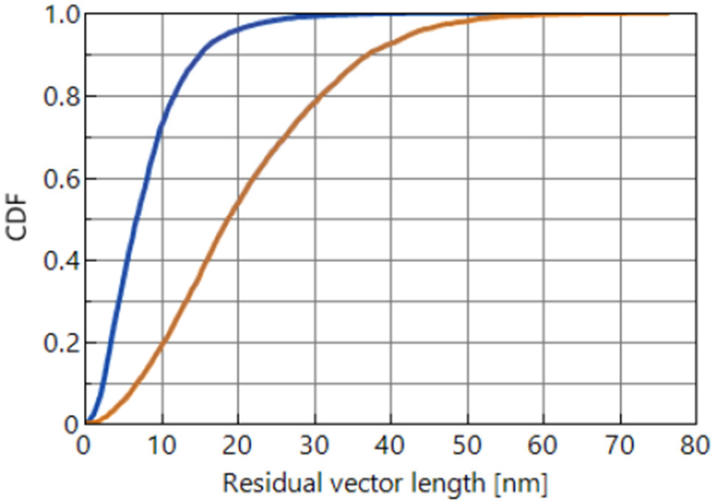
Source: IMEC

Litho Pre-compensation | 20nm OVL residuals



$$Value_{after} = Value_{before} - \frac{\sum_1^8 Value_{before}}{8}$$





- 680 overlay measurements for each wafer pair.
- Note: actual litho corrections require a more detailed overlay map (more measurement points).

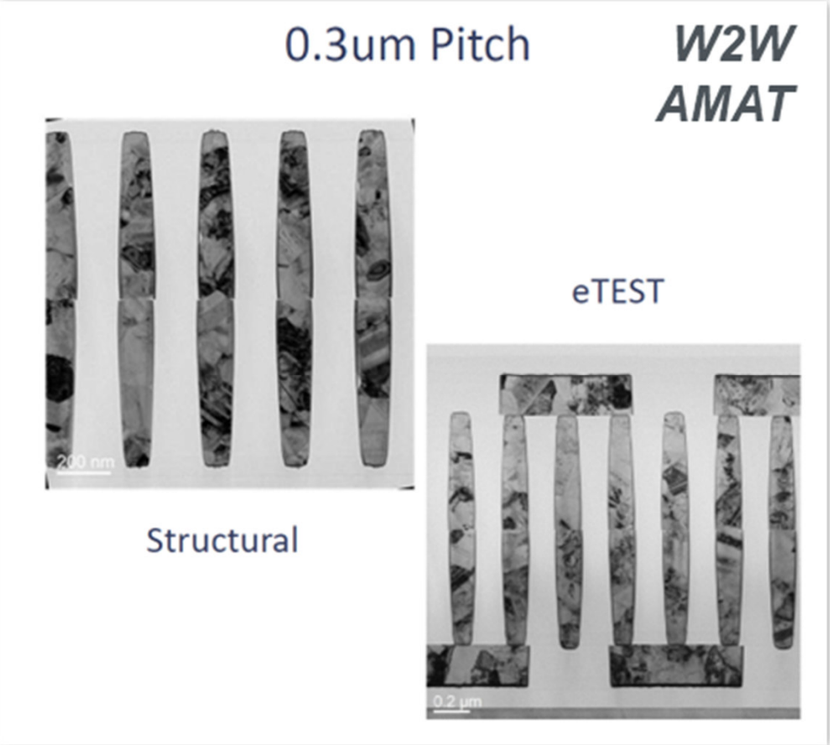
  - Using accurate measurements of a sufficient set of identical wafer pairs does allow to define an RPN litho correction on the hybrid bond pad layer. This could improve the overlay accuracy in the current case with the current tool to some 50 nm (1/2 of the total overlay error).

Source: IMEC

Scalability of Fusion & Hybrid Bonding – Challenges

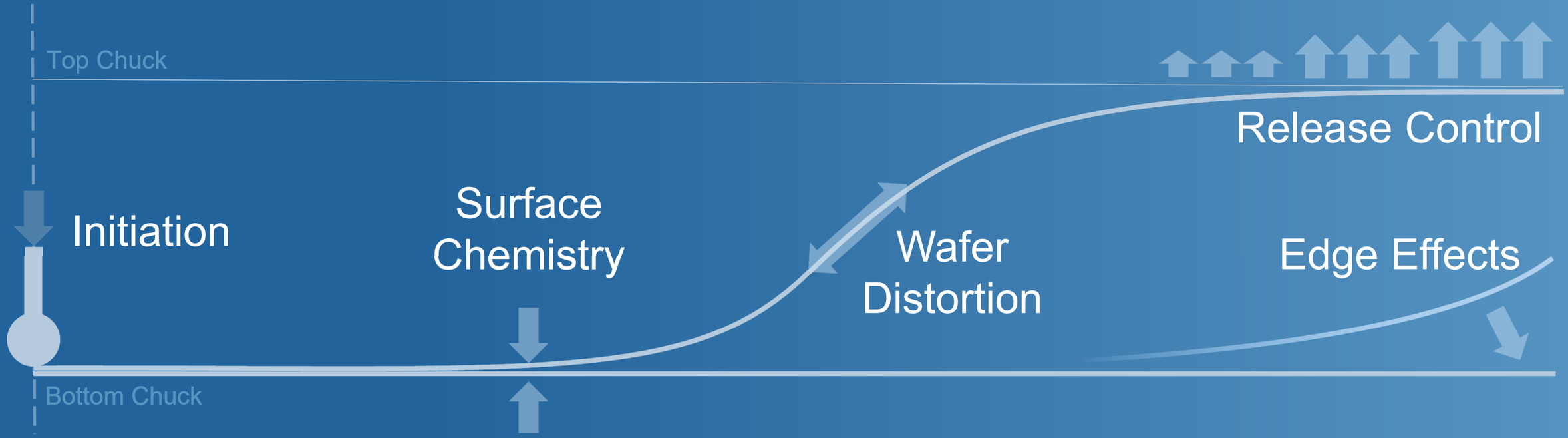
- **Scalability of Cu pads** – How small can Cu pads be made and still bond?
  → Smaller pads and smaller Cu volume reduce the process window
  - Tighter specs on pad recess
  - Oxide management
  - Erosion has to be avoided
- **Alternative dielectrics**
  → Stability against Cu diffusion, low temperature bonding capability, dielectrics with better thermal conductivity
  - SiO2 well understood (incl. bonding mechanism)
  - SiCN works well – mechanism somewhat understood
  - AlN on the horizon

  Bondwave speed management will be very important for the future. – Requires engineering of surface chemistry (mainly hydrophilicity)



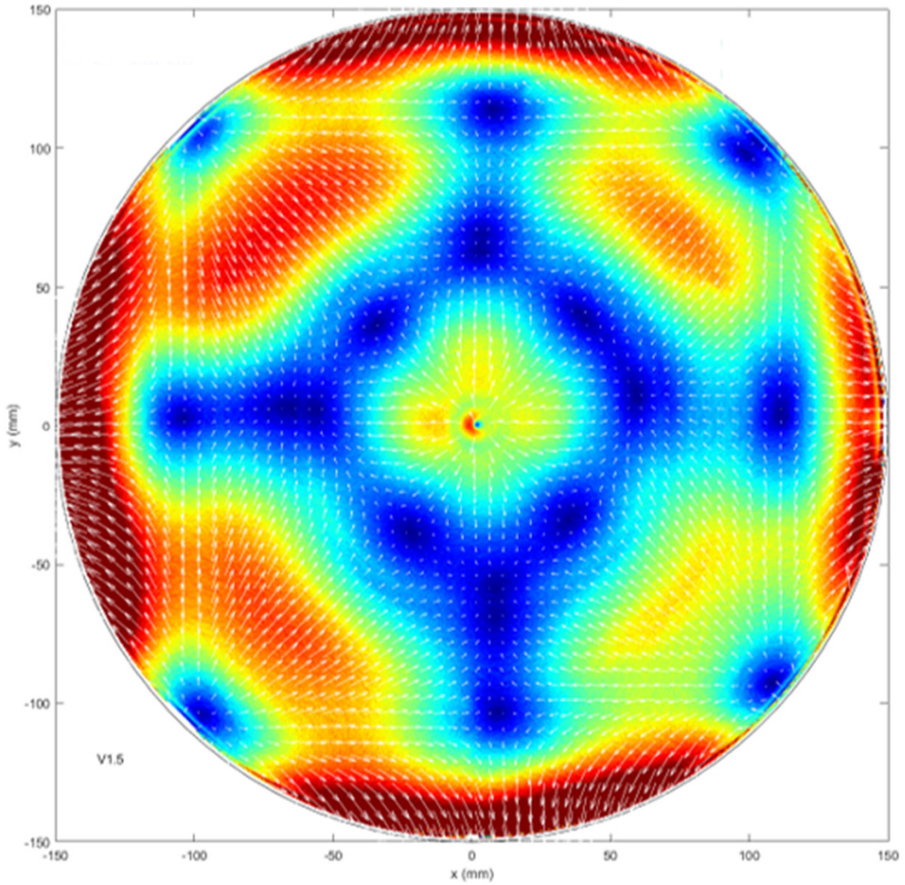
ECTC2024: Tyler Sherwood et al. „300nm Pitch W2W HBI for CFET and 3D DRAM Through Module Co-optimization"

Physics Zoom-in

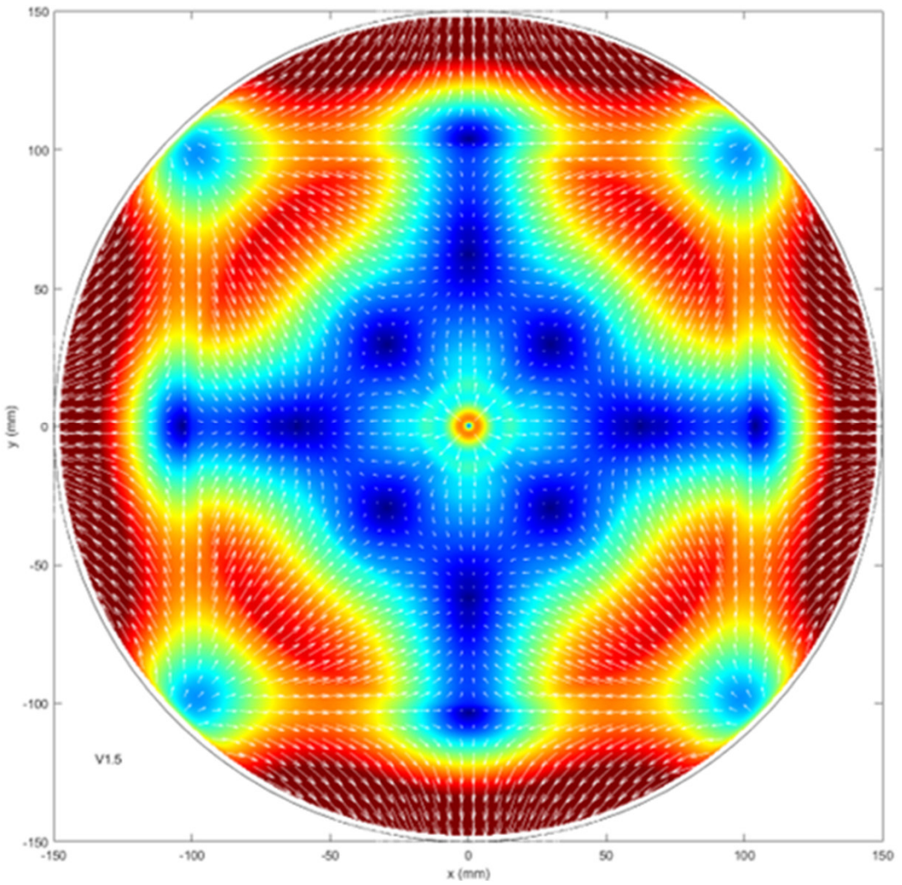


Model Description

Measurement



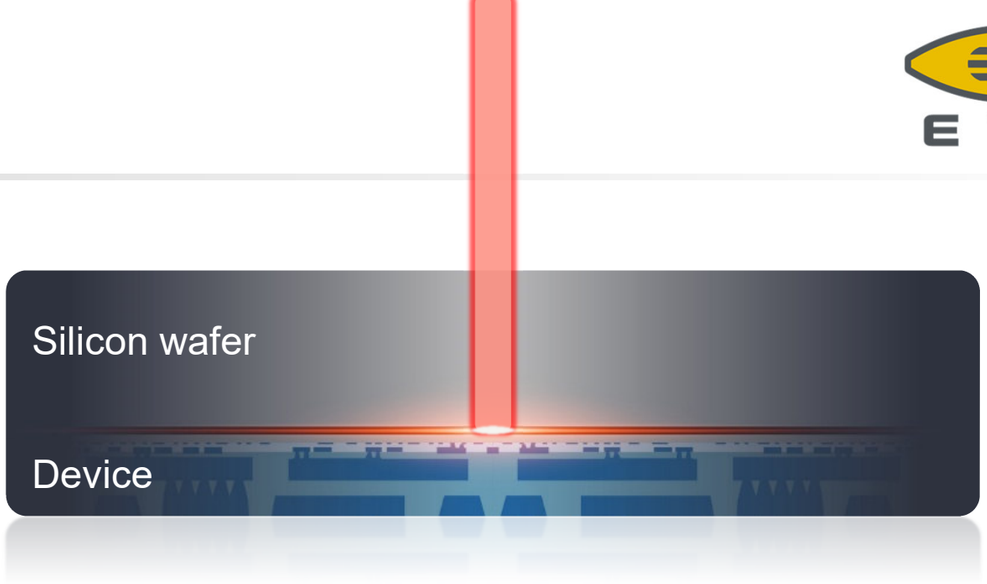
Simulation Results



EVG LayerRelease™ | Introduction

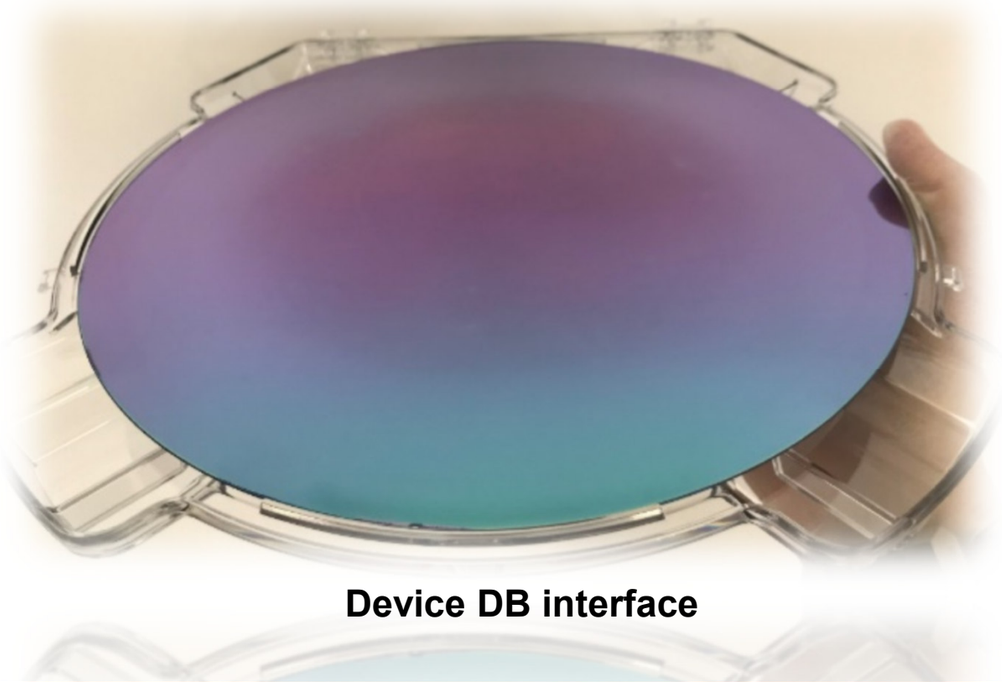
Technology

- Silicon wafers as carriers
- Nanometer precisely defined separation planes
- Ultrathin (<10 µm) die and wafer processing
- Fusion bonding compatible
- Room Temperature release
- Inorganic and front-end processing-friendly
- Withstands high processing temperatures
  > 750°C for hours; >1000°C short term



Applications

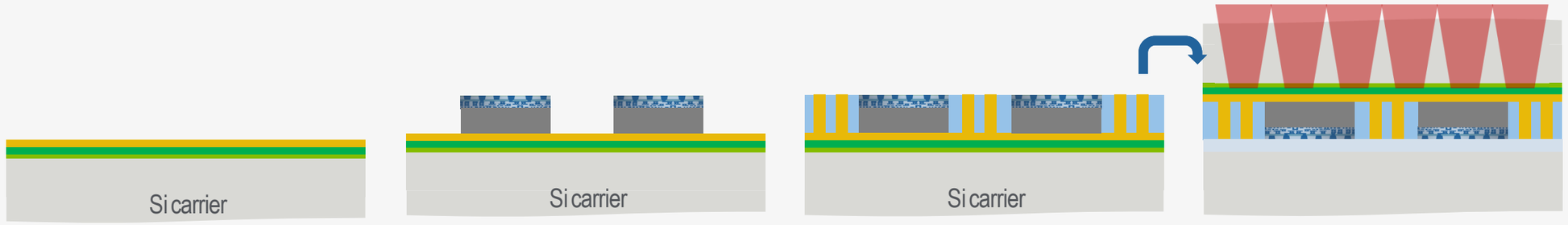
Ranging from advanced packaging to 3D integration to future scaling FEOL integration



Device DB interface

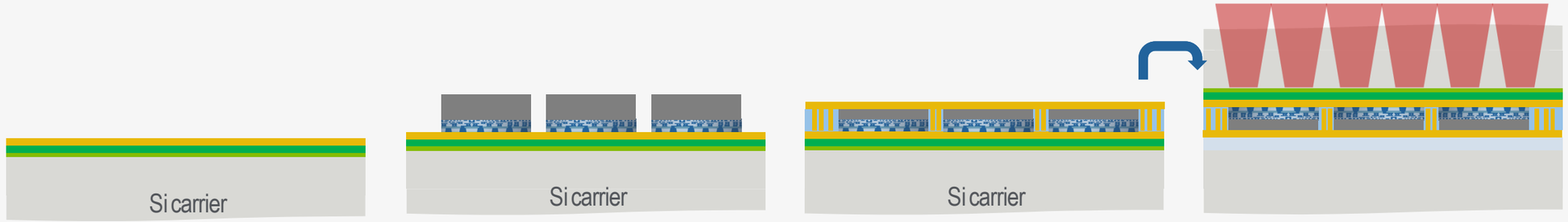
LayerRelease™ | Reconstructed W2W Bonding

Flow 1
Face up
die placement



Limited to die thickness	Silicon Release Carrier deposition (including plating layers, bonding layers and alignment marks)	Face Up die D2W Bonding	Interlevel dielectric fill and interconnect patterning	Reconstructed W2W Bonding and subsequent IR Laser Release (EVG Gemini FB & EVG LayerRelease)

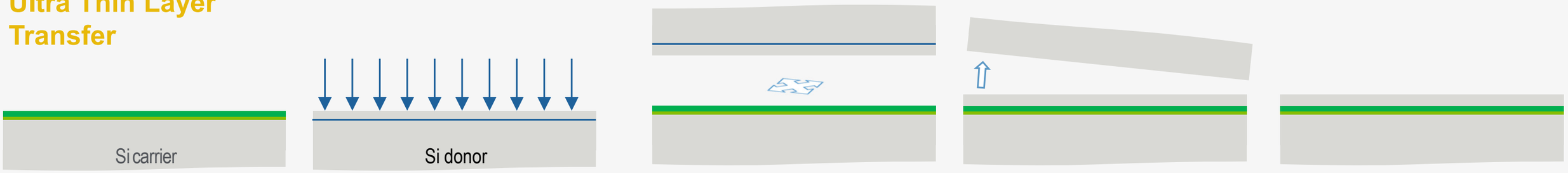
Flow 2
Face down
die placement



Enables down to single digit µm die thickness generating know good wafers for fusion and hybrid bonding	Silicon Release Carrier deposition (including plating layers, bonding layers and alignment marks)	Face Down D2W Bonding	Interlevel dielectric fill, wafer level thinning, and interconnect patterning	Reconstructed W2W Bonding and subsequent IR Laser Release (EVG Gemini FB & EVG LayerRelease)

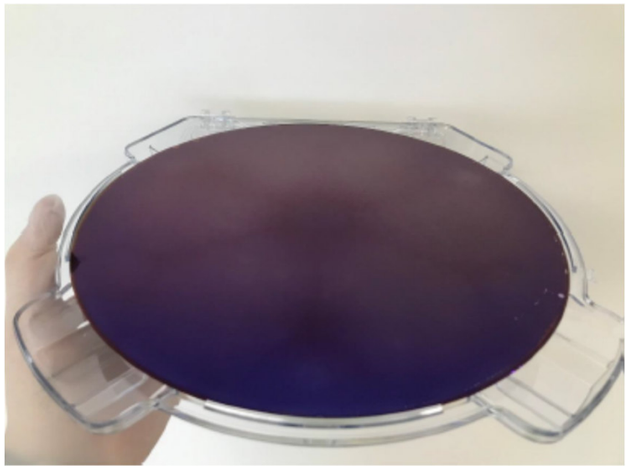
IR Laser Release | Ultra Thin Layer Transfer / IR-SOI Release

Ultra Thin Layer Transfer

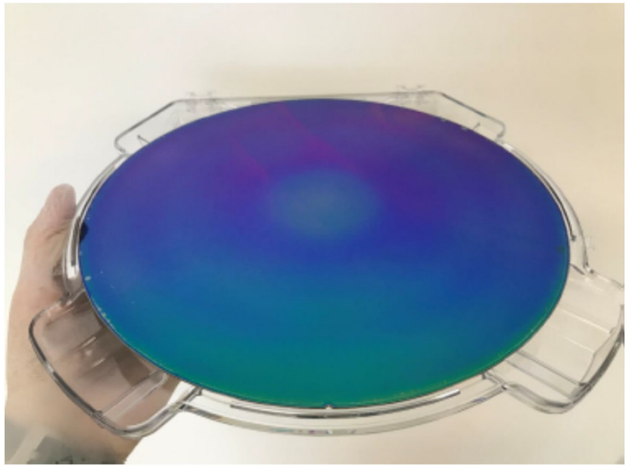


Silicon Release Carrier deposition	Ion implantation of donor substrate	Fusion Bonding of implanted donor to IR carrier substrate	Annealing, mechanical initiated separation and wafer surface finishing (CMP & Oxide growth)	IR-SOI substrate ready for Epitaxy Sequential integration Sequential / Hybrid CFET

- Wafers are easily separated after IR laser release with minimum lift-force
- DB interfaces are free from peeling or any other laser initiated defects
- inspection showed release showed exact separation in deposited release layers



Carrier wafer interface after debonding



Device wafer after thin layer transfer

Thank you for your attention!