Agency for Science, Technology and Research
SINGAPORE

Accelerating Innovation with Industry-Grade Platforms

Carlos Mazure & Navab Singh
Institute of Microelectronics
Agency for Science, Technology and Research (A*STAR)
Singapore

CREATING GROWTH, ENHANCING LIVES

A*STAR encompasses

Research & Technology

- *Science & Engineering Research Council (SERC)*
  - *8 Research Institutes*
- *Biomedical Research Council (BMRC)*
  - *9 Research Institutes*
- *National Platforms*

Industry Development & Commercialisation

- *Innovation & Enterprise (I&E)*
- *Venturing, Startups*

Talent Development

- *A*STAR Graduate Academy*

>6,000 Staff

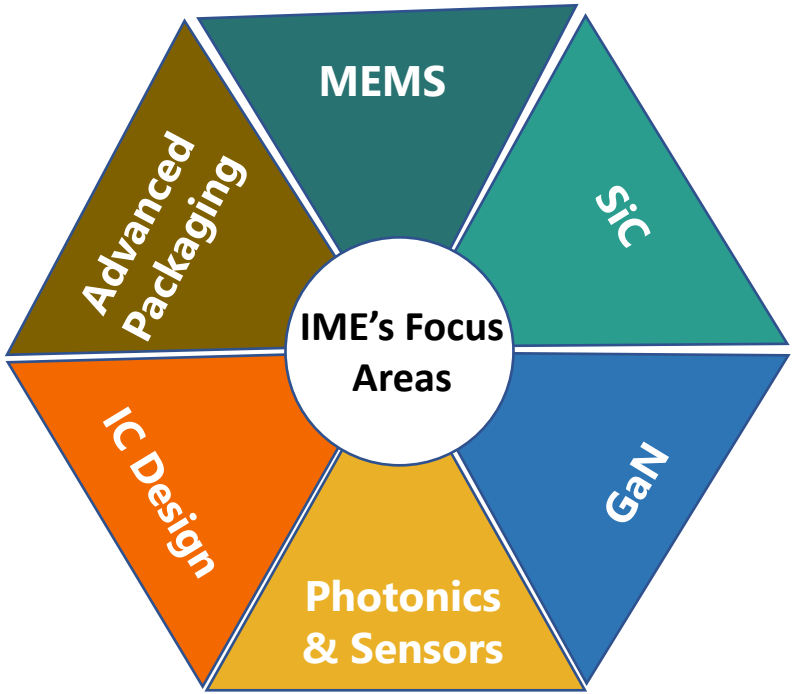
>4,700 Researchers, Engineers, and Technical Support Staff

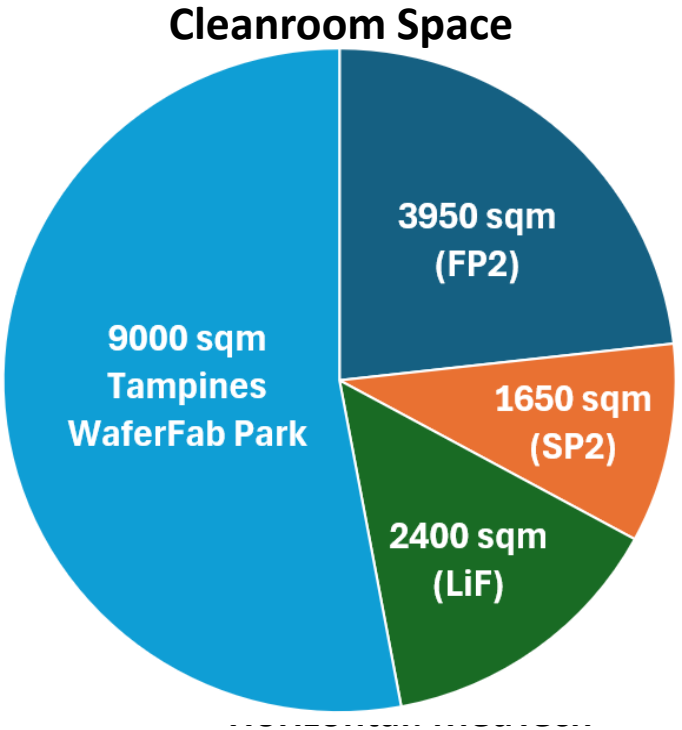
~37% from **>60** countries

Numbers accurate as of March 2023

CREATING GROWTH, ENHANCING LIVES

Institute of Microelectronics: R&D & Prototyping in Industry-grade Facilities





Advanced Packaging

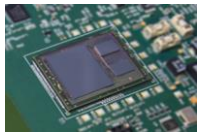
State-of-the-art 300mm R&D and prototyping line
Broad spectrum platform: W2W, C2W, chiplets, COP, SoW

IME has a rich experience in Advanced Packaging

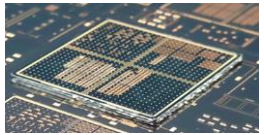
Our R&D is mostly driven by the needs of AI / high performance computing

2.5D/3D IC Packaging

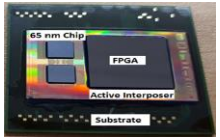
2.5D Passive Interposer



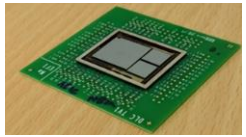
15 die stacking with TSV & µ-bump



Active Interposer



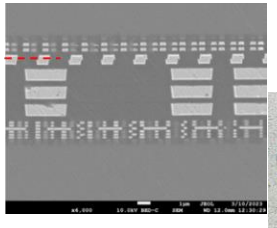
Embedded Fine Pitch Interconnect (bridge chip) Interposer



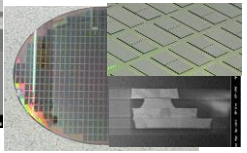
Quantum Ion Trap

Bonding interface

Wafer-to-Wafer Hybrid Bonding

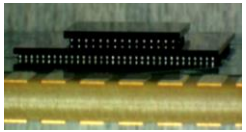


Chip-to-Wafer Hybrid Bonding

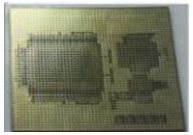


2013 | 2015 | 2017 | 2019 | 2021 | 2023

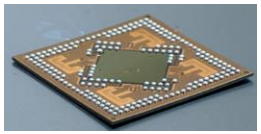
Fan-out Packaging



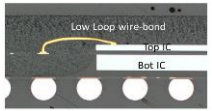
Fan-out Package-on-Package



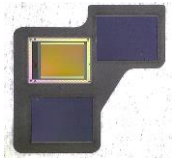
Multi-chip Fan-out Package



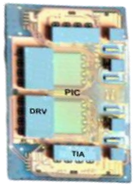
3D Antenna-in-Package



Ultra-thin Package-on-Package



Via-Last Through Silicon Via on multi-chip fan-out



Electronic Photonic Heterogenous Integration

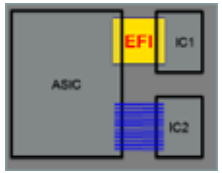
Large (~3x reticle size) fan-out package for chiplet integration

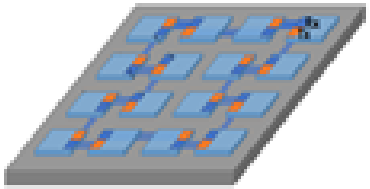
Advanced Packaging Capabilities

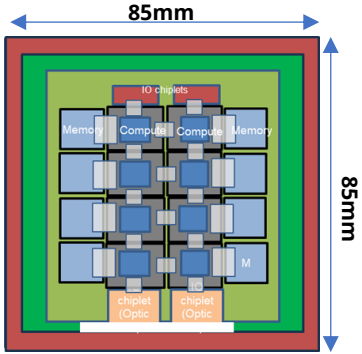
Application/System Requirements	Package Architecture	Models, PDK	Adv. Pkg Modules	Process Integration, Materials Selection	Packaging Platforms
Data Centre/ HPC	Electronic & Photonics Integration	Mechanical	TSV		FOWLP
AI	High Density 2.5D Pkg for AI SiP	Electrical	Micro-bumps		
IoT, 5G	Fan-out based RF module for 5G		Fine Pitch RDL		2.5D
AR/VR	AR/VR Display Module	Thermal	Multi Layer RDL		
Automotive	Si/SiC interposer for Radar module	Package Design (PDK)	Flip Chip Bonding		3D Stacking
	mmWave Antenna in FOWLP		Cu-Cu Bonding		

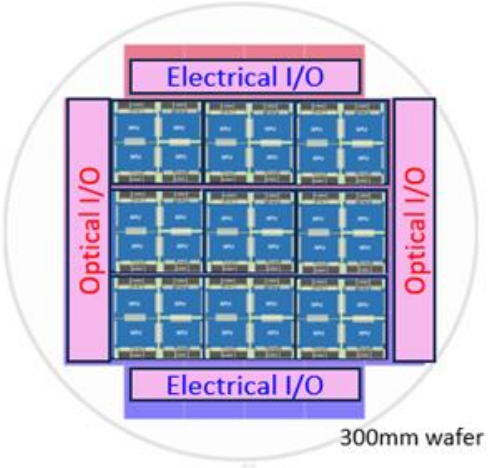
Development, prototyping & low volume mfg.

IME's Chiplet Integration Roadmap









2018	2020	2022	2024	2026	2028	2030	2032
Embedded Fine-pitch Interconnect (EFI) bridge interposer: ASIC-HBM integration		HD-FOWLP SiP: NetFlex Chiplet CNN accelerator		Large RDL Interposer Package with embedded bridges and Optical I/O for AI training systems. TDP>2kW		System on Wafer (SoW): High Performance Compute Accelerated Processing Unit with over 40 xPU and 80 HBM Stacks. TDP: 25-50kW	

Power Delivery and Thermal Cooling are Major Challenges for Ultra Large Systems

Piezo MEMS

Non-captive Lab-in-Fab
R&D and volume manufacturing in the same facility
Fastest time-to-prototype for piezo-MEMS

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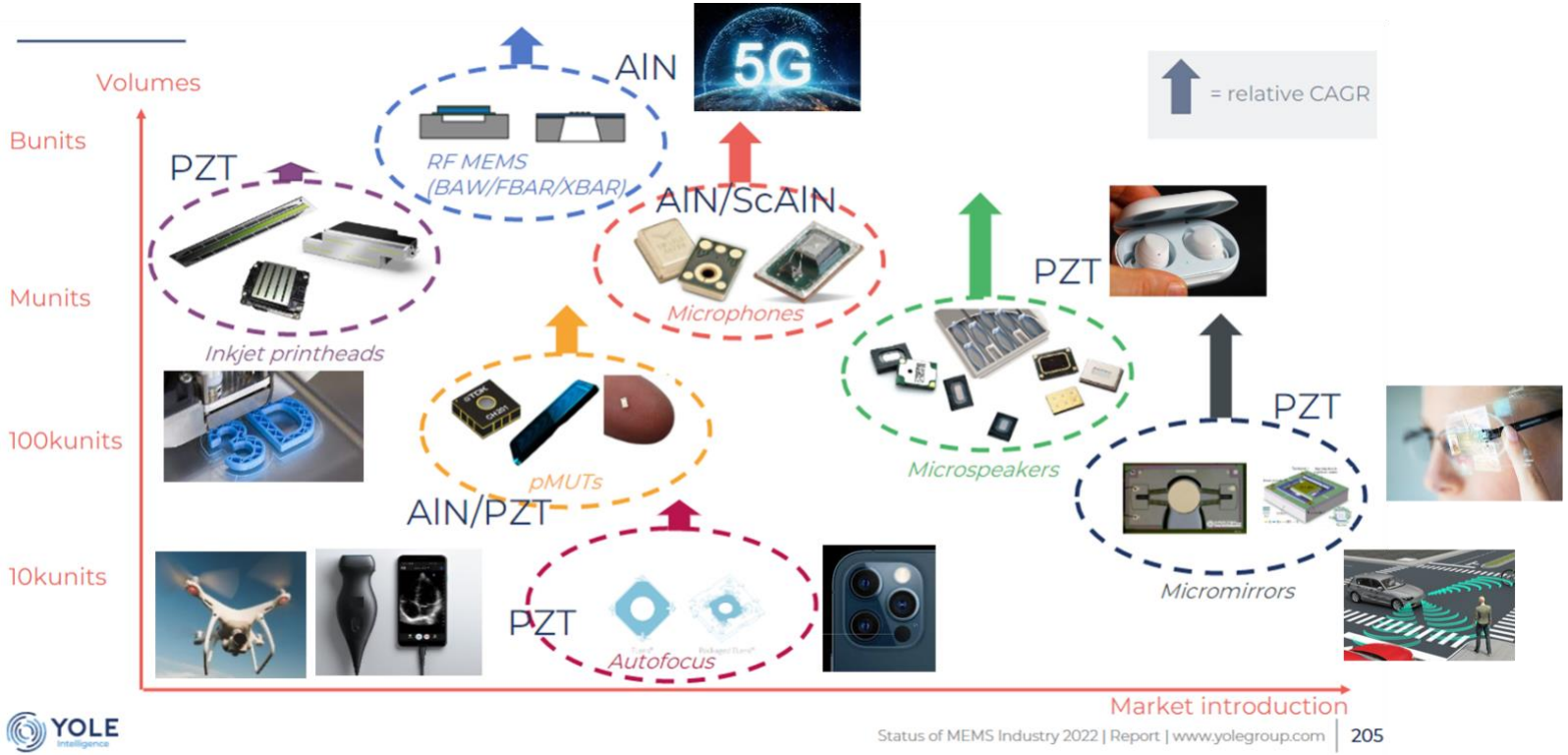
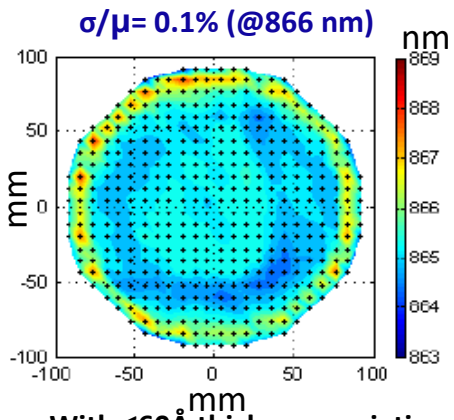
Piezo-MEMS Platform addresses all Growth Areas

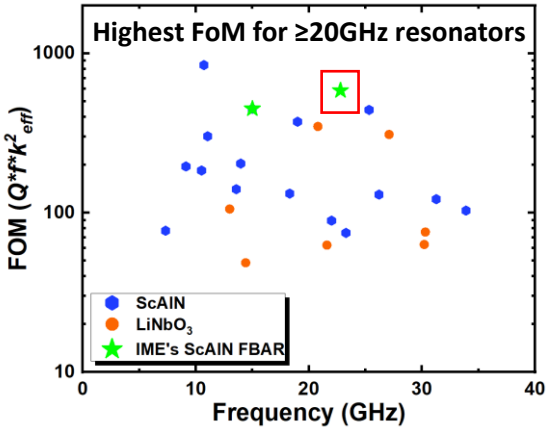


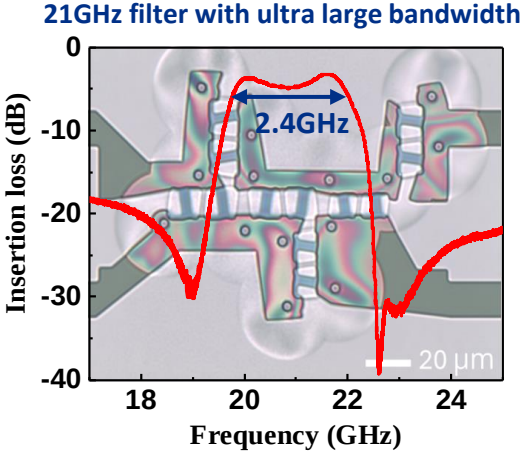
Its small size, low power consumption, and compatibility with semiconductor manufacturing processes make Piezo-MEMS an ideal solution for numerous applications.

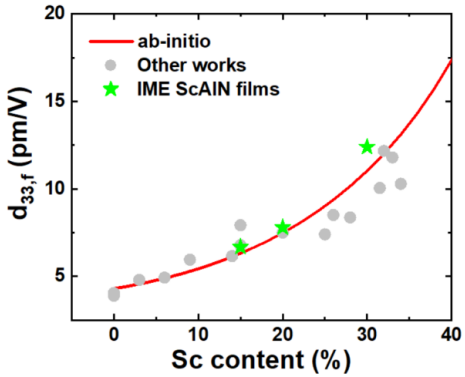
Best-in-class piezo materials and platform technologies



With ≤60Å thickness variation across 200 mm wafer.







Best-in-class ScAlN on Si wafer, characterized by highest Piezo coeff. d_{33}

Thin-film ScAlN platform

RF MEMS (GHz resonator & filter) and resonator-based sensors

ScAlN/PZT on Si platform

for sensing and actuating

ScAlN on Si-on-nothing platform

for microfluidics and high density PMUT arrays

PMUT using best of PZT & ScAlN

- TX sensitivity: 4x higher for PZT
- RX sensitivity: 10x higher for ScAlN
- Best combination: TX-PZT & RX-ScAlN.

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SiC

Most advanced 200mm R&D and prototyping line
Non captive process and device development
Complete ecosystem from epitaxy thru power module

Silicon Carbide Technology Platform

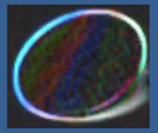
SiC Substrate Integration

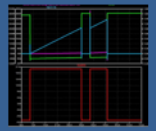
- SiC crystal
- SmartSiC™
- via procuring substrates

SiC Epitaxy

- Si-/C-face SiC
- Trench-filled SiC Epitaxy

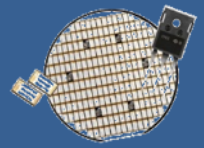
SiC Device Design, Process Integration, Fabrication, and Testing (1.2-20kV)



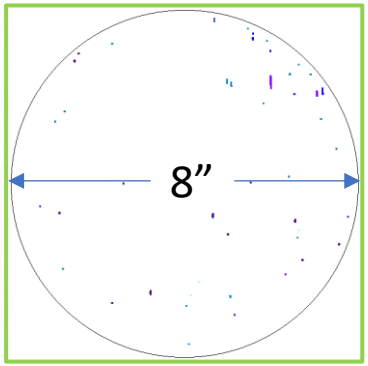


- Si-/C-face Trench Gate MOSFET w/wo SJs
- Si-/C face Junction Barrier Schottky Diode
- SiC CMOS (Planar Gate/FINFET) Drivers
- IGBT with modified SmartSiC™

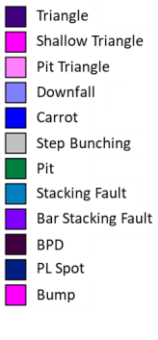
SiC Power Module Packaging

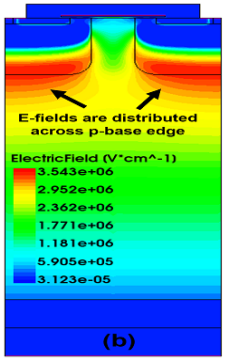


- Double-Sided Cooling, DBC-free package, 3-Phase solutions
- Co-Optimized Device to Package
- Module with integrated gate drivers

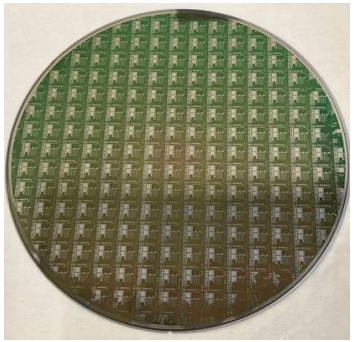


Post epitaxy Candela 8520 scan,
Total Killer defect density ≤ 0.5/cm^2

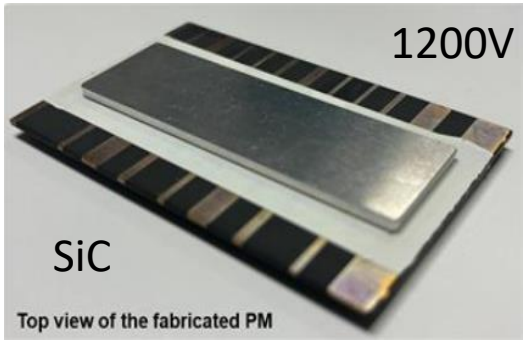




Device TCAD



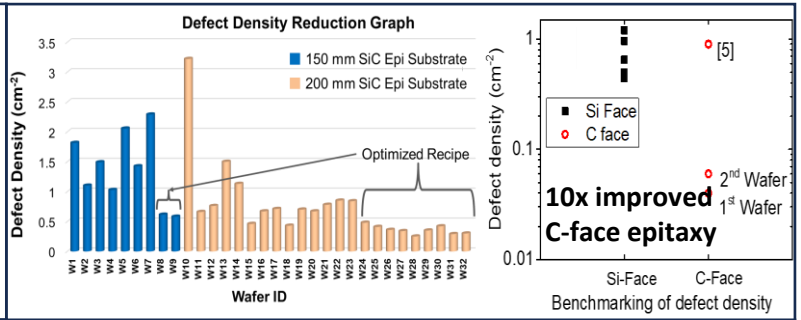
Fully fabricated 8” wafer



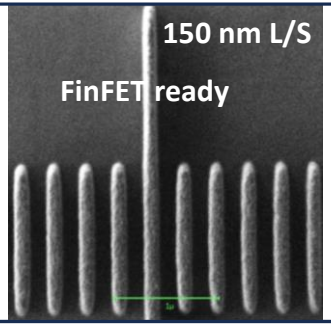
6-in-1, 3-phase SiC power module

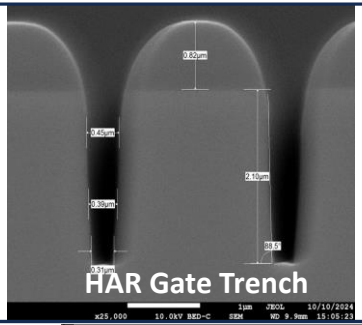
Speciality of Our 200 mm Open Innovation SiC Pilot

ASM LPE 1O8 with Candela 8520.
"Extremely low killer defects & Excellent Thickness and Doping uniformity"

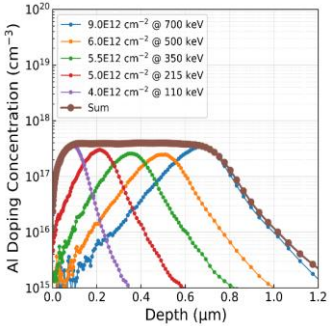


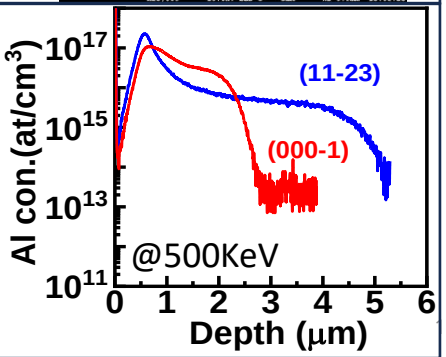
ASML PAS5500/850C with TEL Act-8.
"110nm resolution in a SiC line with transparent wafer handling capability"





Nissin IMPHEAT-II with integrated XRD.
"Channeling implant for device innovations reducing manufacturing cost"





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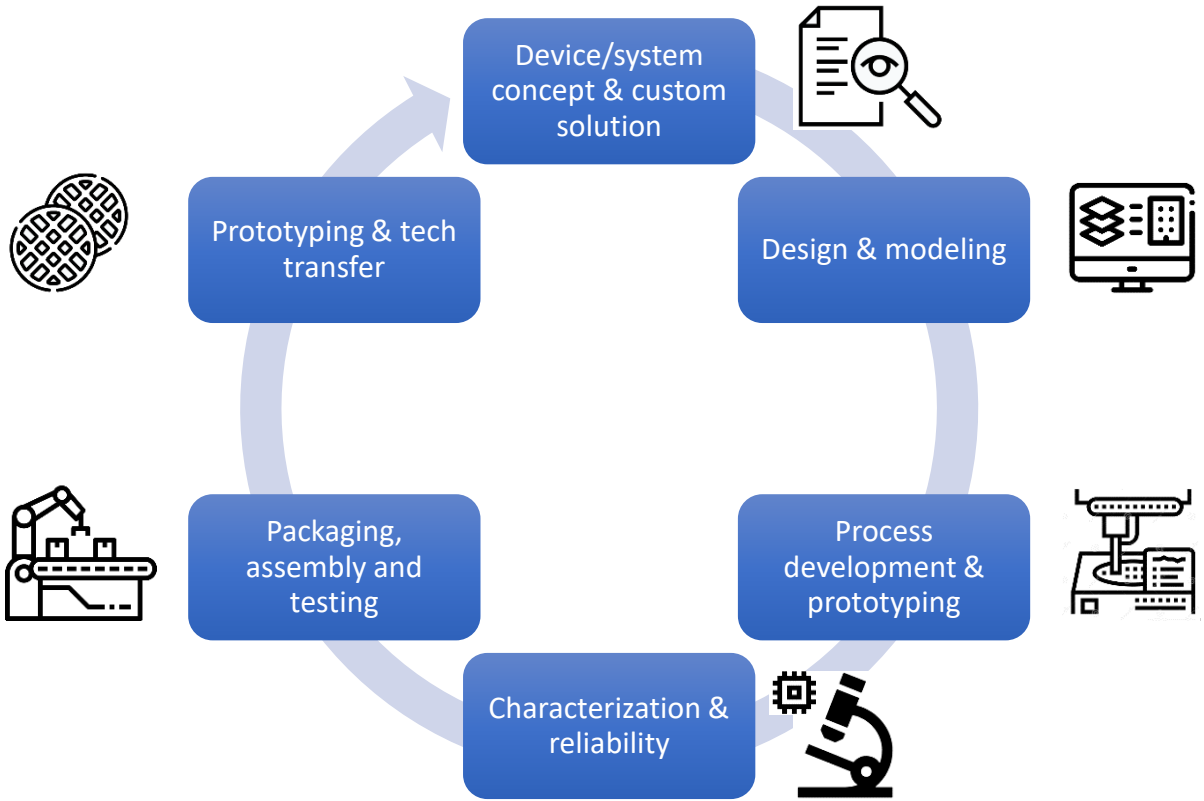
Summary: Value Proposition



Institute of Microelectronics
IME

THANK YOU

For more information, visit www.a-star.edu.sg

Email contact: Navab@ime.a-star.edu.sg