

Achieving Zero Defect Manufacturing

APRIL 18, 2024



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Fabs Today

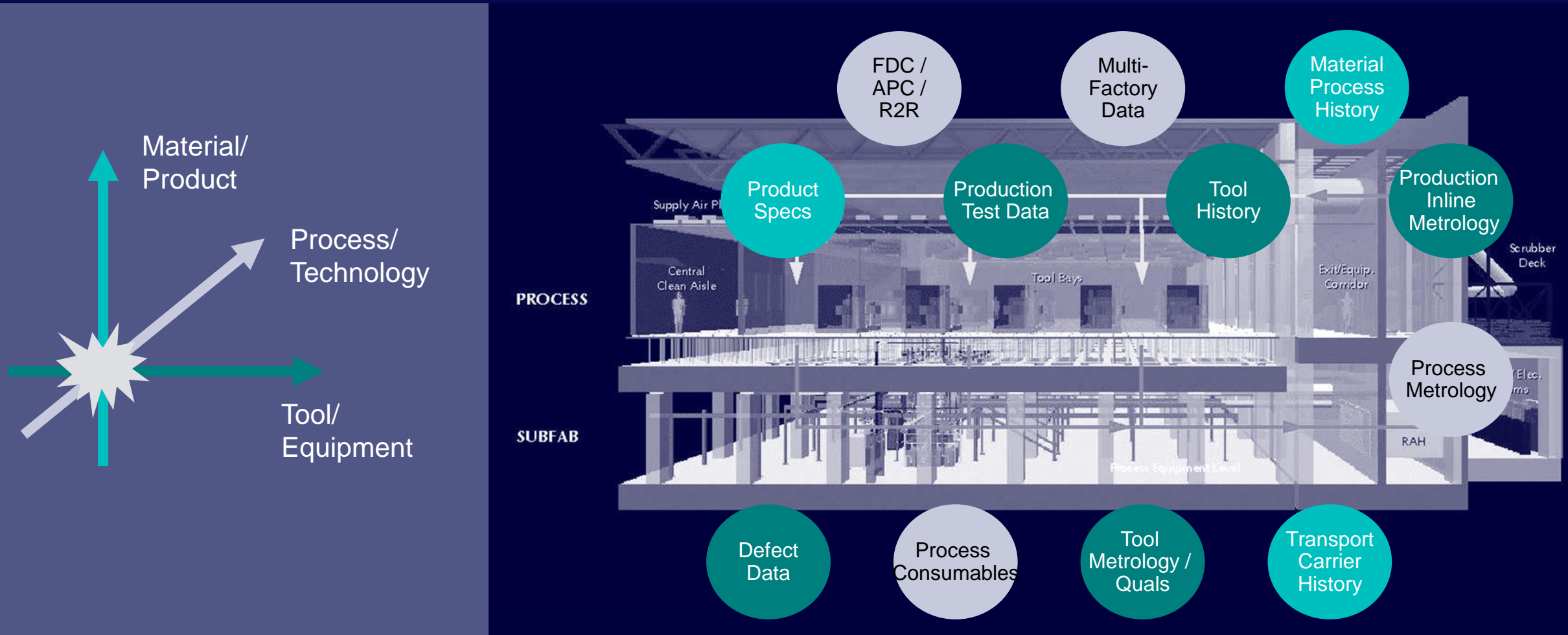
Modern processes have become unimaginably **complex**

Managing your controls are critical to ensuring **performance**

—
All types of chip providers require **zero defectivity**, reliability & traceability to meet customer requirements

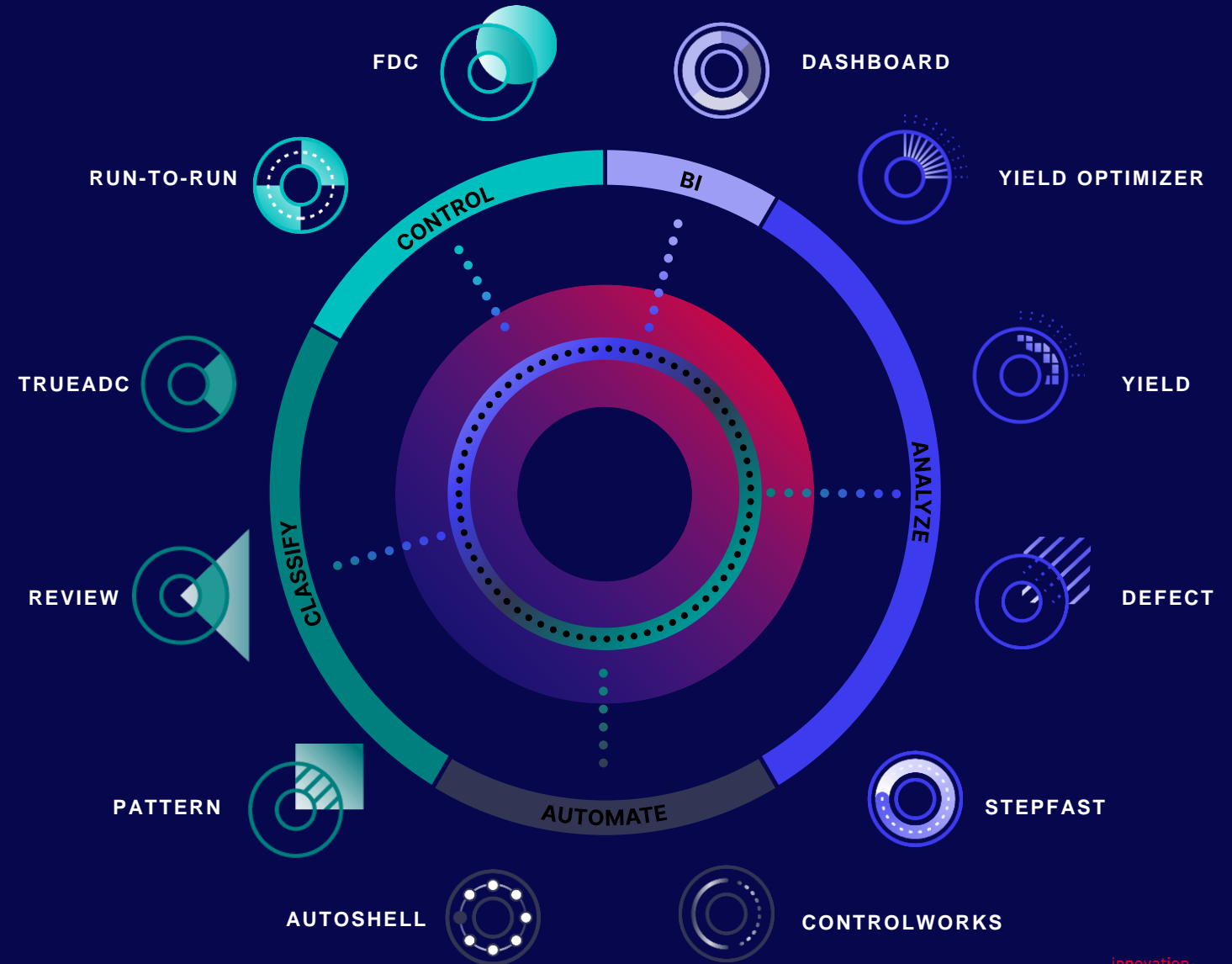
Big Data

Data Integration Is The Starting Point For Any Digital Transformation



Enterprise Software Ecosystem

Onto Software is the
Connective Tissue for
Power Manufacturing
Process



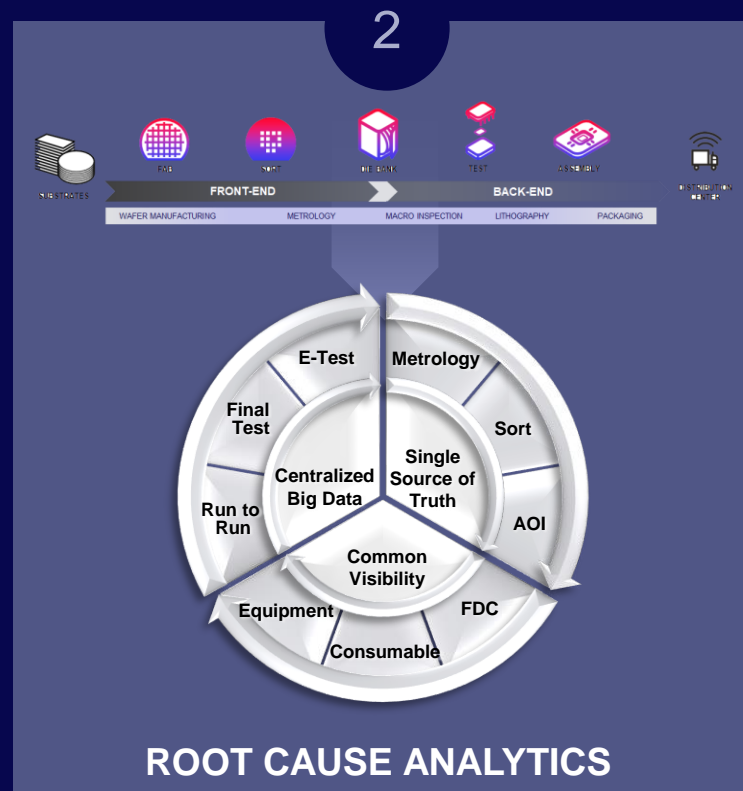
Achieving Zero Defects in Semiconductor Device Manufacturing

Three Step Initiatives

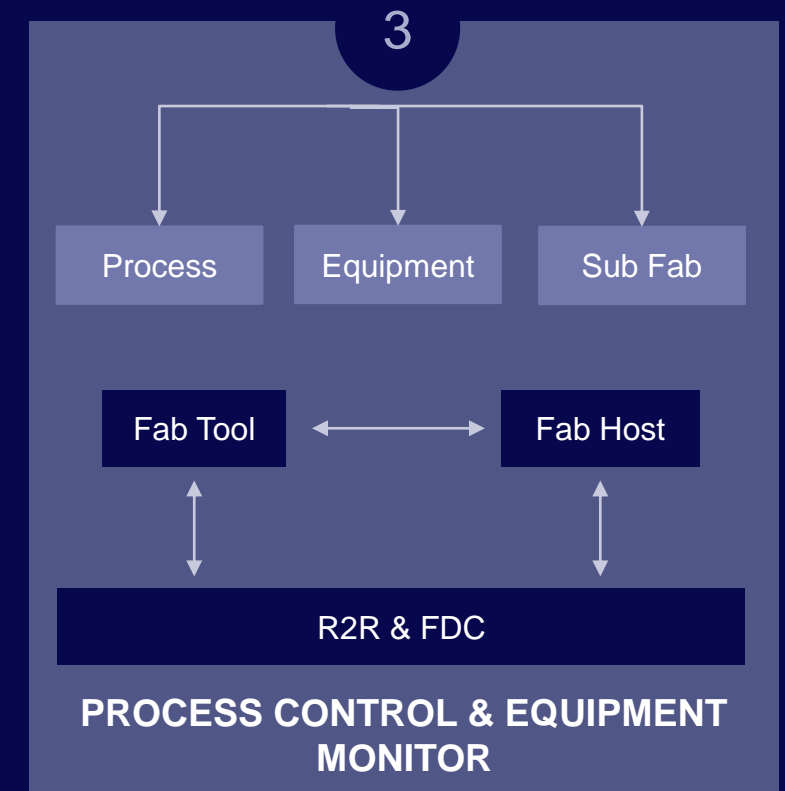
Detect & Classify Defects



Find Defect Sources



Prevention of Defects










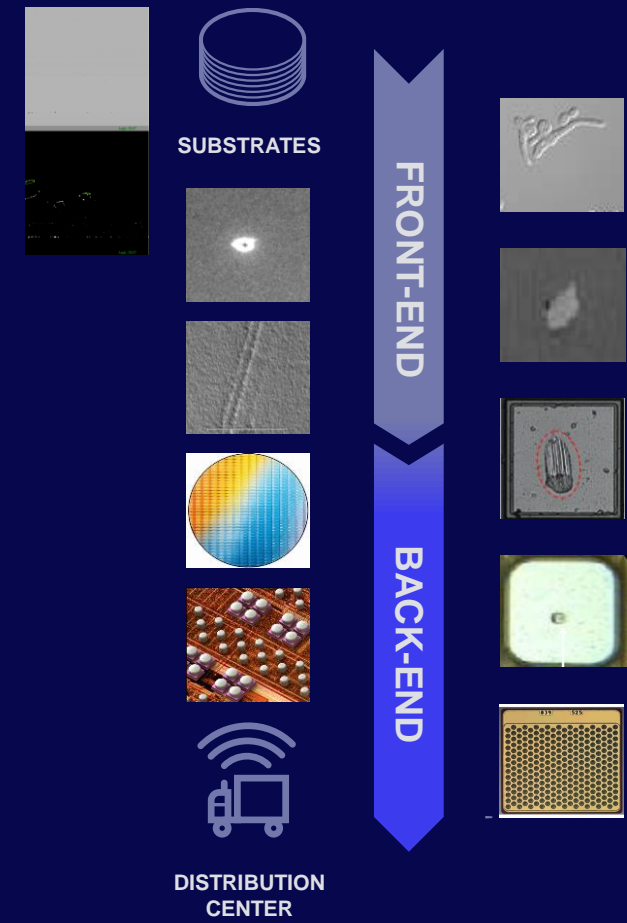
Total Solution for Inspection & Metrology

Detect & Classify – Defect Level



TRUEADC®

-  One ADC for Entire Fab – AOI, SEM, OM/Camera
-  On Tool Real Time ADC
-  Defect, Die, Shot, Wafer Edge
-  Whole Wafer Image Front & Backside
-  Multi Engine Approach
-  Closed Loop Feedback
-  Real Time Binning & Die Disposition with Discover



Total Solution for Inspection & Metrology

Detect & Classify – Defect Level



 One ADC for Entire Fab – AOI, SEM, OM/Camera

 On Tool Real Time ADC

 Defect, Die, Shot, Wafer Edge

 Whole Wafer Image Front & Backside

 Multi Engine Approach

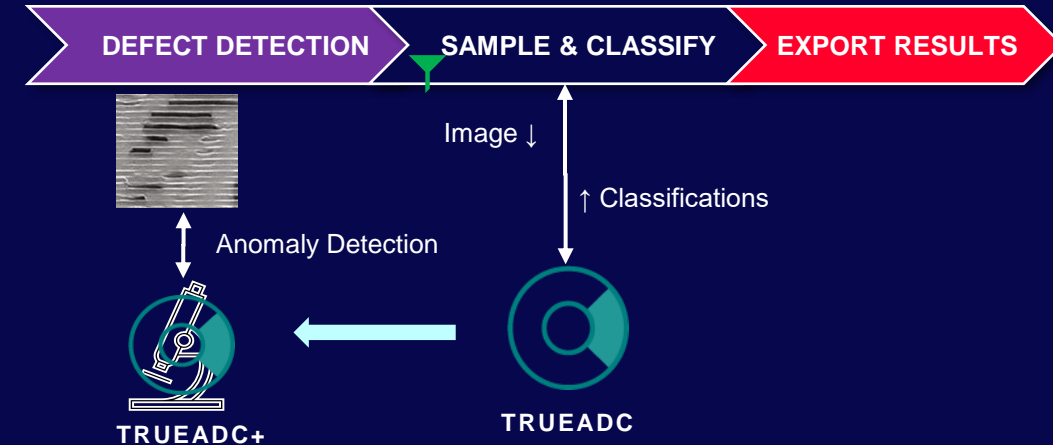
 Closed Loop Feedback

 Real Time Binning & Die Disposition with Discover



TRUEADC®

AOI tools running at higher sensitivities result in excessive rates of nuisance and non-visual defects










TRUEADC+ Removes 60% of the noise that impacts throughput & yield loss

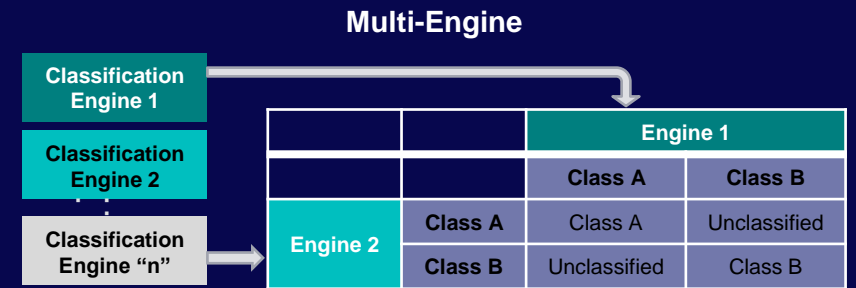
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LABELLING TOOL

Total Solution for Inspection & Metrology

Detect & Classify – Die Level

REVIEW



DEFECT



Rules Based Auto Die Binning

Auto Bin Potential Reliability Failures (GDBN)

Trend Hit Rate / Kill Ratios

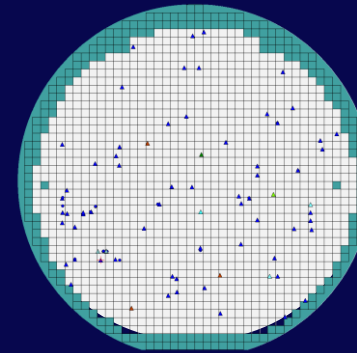
Predict Die Bin & Failures

Integrate, Feedback & Feed Forward

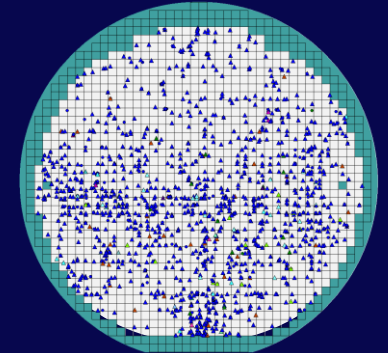
Enable Industry 4.0 towards Fab Efficiency

Tools to Monitor Performance both ADC & Manual

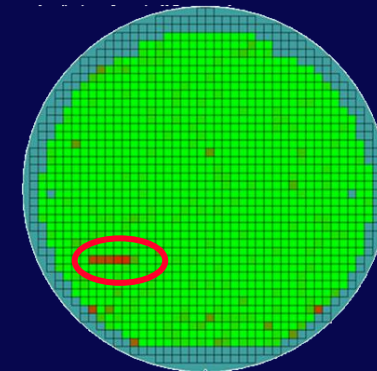
DEFECT MAP



STACKED MAP



STACKED PROBE
MAP – MICRO CRACK



Total Solution for Inspection & Metrology

Detect & Classify – Wafer Level



PATTERN

Auto Discovery for Library Setup

Detect & Classify Wafer Signatures

Inline Wafer Monitoring

Learn from UNKNOWNNS

Search/Link Patterns Across Data Types

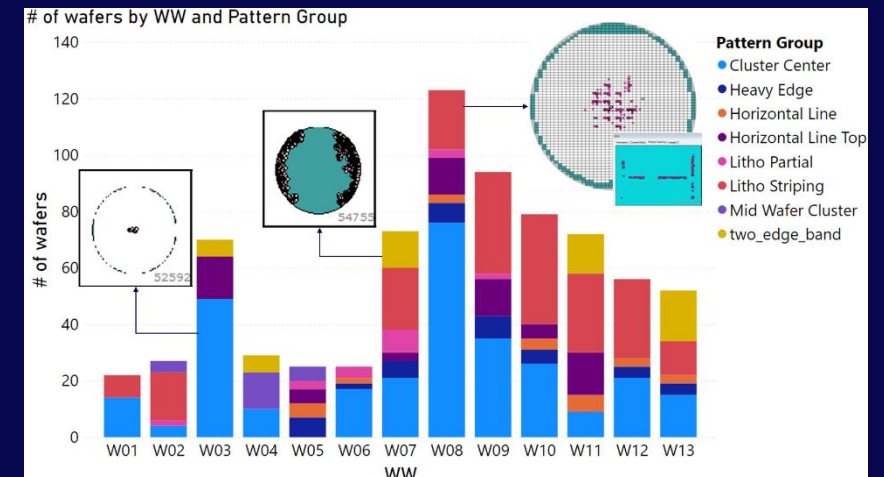
Advanced Scratch Detection

Integrate, Feedback & Feed Forward

REACTIVE TO PROACTIVE

21% of wafer starts have some form of spatial pattern

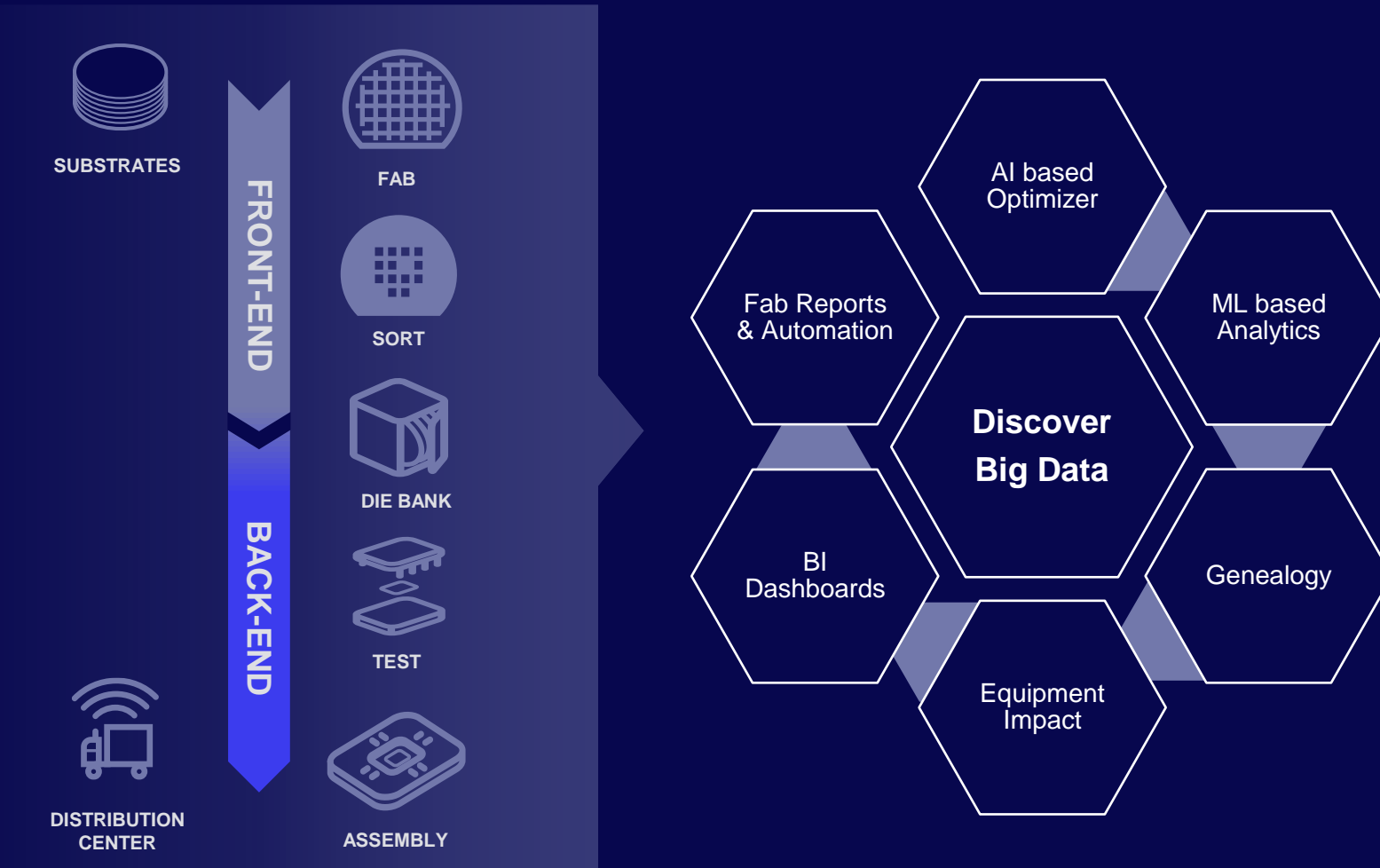
↳ 4% of wafers exhibit new UNKNOWN spatial pattern



Results of learning from “UNKNOWN” spatial yield limiting events over 3 months

Root Cause Analytics (RCA)

Faster Understanding of Visual, Non-Visual & Latent Defect Sources



Supply Chain Analytics

- Multi-site Integration
- Enable Feedback – FT to EPI
- On-site & In Cloud Ready

Introducing

- Web Based AI Yield Optimizer
- Test Quality Center

To Improve Quality & Reliability of Automotive Device Manufacturing!

RCA Value Case 1

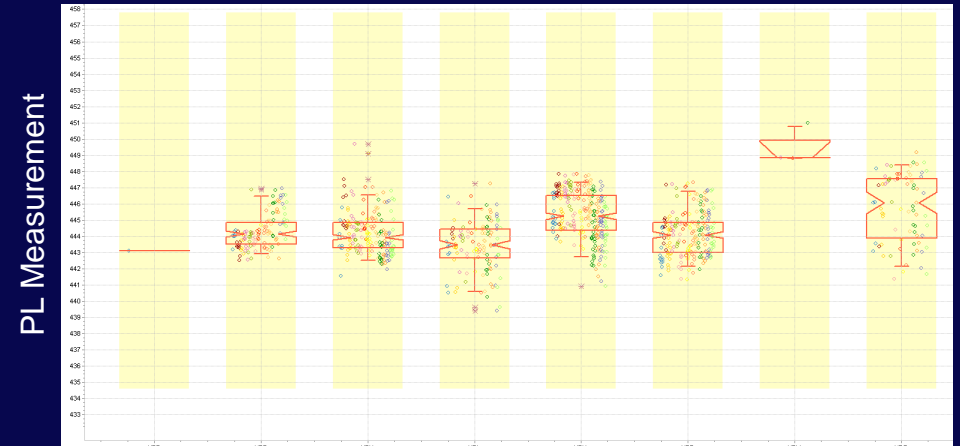
Integrating Wafer Probe, EPI and PL data

Challenges addressed

- Linking wafers pre & post EPI
- Depending on wafer die count, dealing with large volumes of electrical test data
- Normalize and interpolate size level data into die level

Value

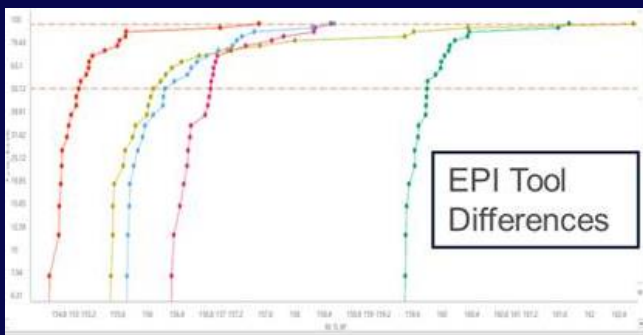
- Reduced time to root cause from days to < 3mins
- Enabled zero defect manufacturing & improved yield by saving 100s of wafers getting processed from problem EPI Tool/Pocket



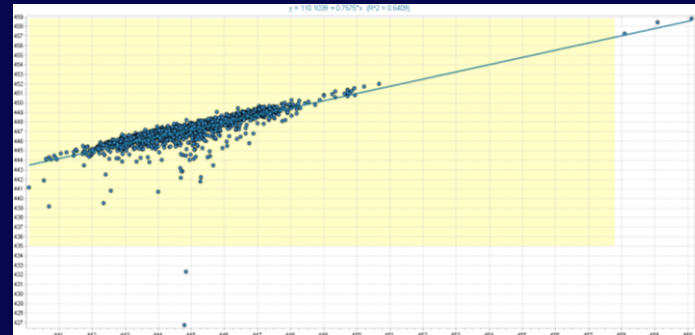
EPI Tools

NOTE: Wafer position within EPI reactor also can be used to understand trends

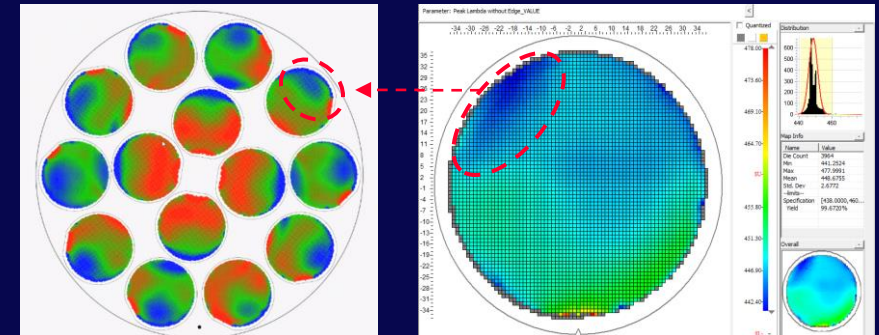
Electrical Test Performance by EPI Tool



WP Parameter vs. PL Statistical Mean

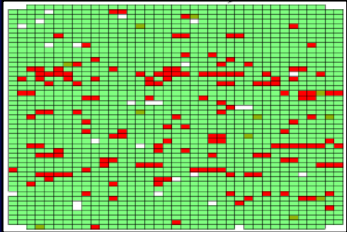


PL Parameter Map



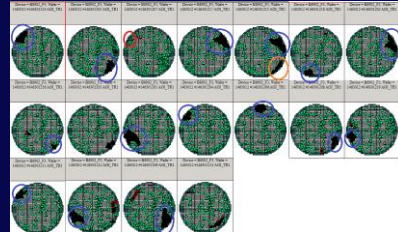
RCA Value Case 2

Problem Solving within the Supply Chain



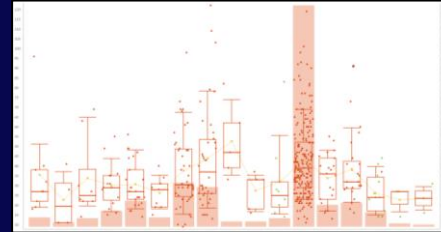
\$375K

Potential loss* due to Final Test on Panel

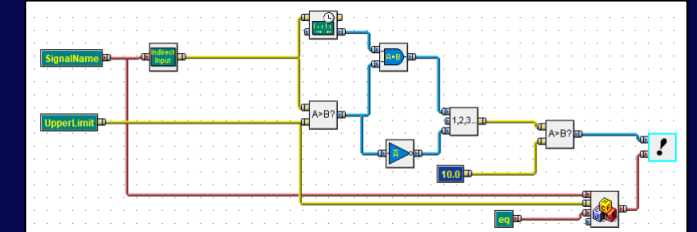


1,700 wafers

Failed dies come from wafers with edge cluster that are signaled by Spatial Pattern Recognition



Issue found to Spinning Step & specific Spin Coater by integrating MES into YMS, Identified the "bad" tool



A proper exhaust flow is crucial for Quality & Yield

Setup monitoring for exhaust flow sensor to notify and clean exhaust when more than 10 consecutive samples are above 95 Pascal

Panel Test

Wafer AOI

MES

FDC

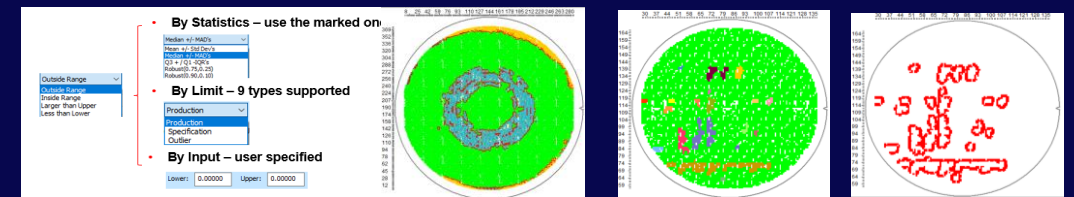
Reactive to Proactive Zero Defect Manufacturing

Avoiding Potential Dormant Defects

Test Quality Management

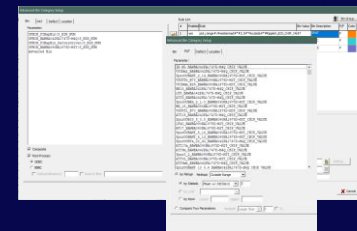
Best practices followed by fabs today

- Dynamic Part Average Testing (DPAT)
- Statistical & engineering rules-based binning per AOI results, WP test values & bin codes
- Good die in bad neighborhood
- Lot level guard banding / die kill
- Reticle field based die kill
- Edge exclusion
- Die score based on different events and data types



PAT & DPAT Map

Cluster-based BBBC



Custom Rule definitions



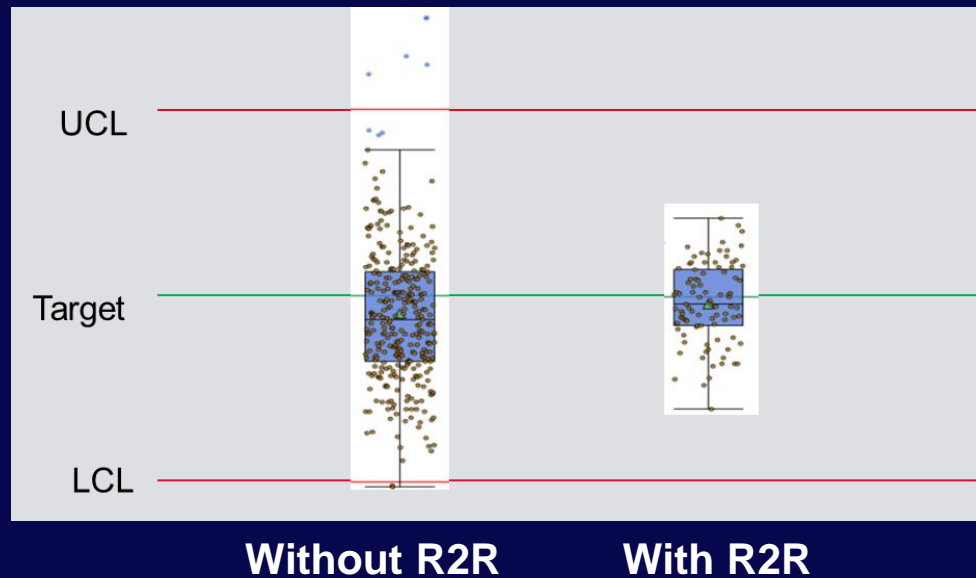
Prevention of Defects by Process Feedback and Feedforward

Applies to Entire Manufacturing Process Steps

Customer Example: Enabling Dynamic Deposition Rate Control Throughout the Lifetime of the Process Chamber

Zero Defect Initiative

- Implement feedback from Yield Analytics & FDC to empower R2R Controller Design



Process	Equipment
Increased Process Centering	Chamber Lifetime Increased 15%
Dispersion Decreased 32%	Enabled Automated Maintenance Detection
OOB Decreased 40%	Reduced Maintenance Costs

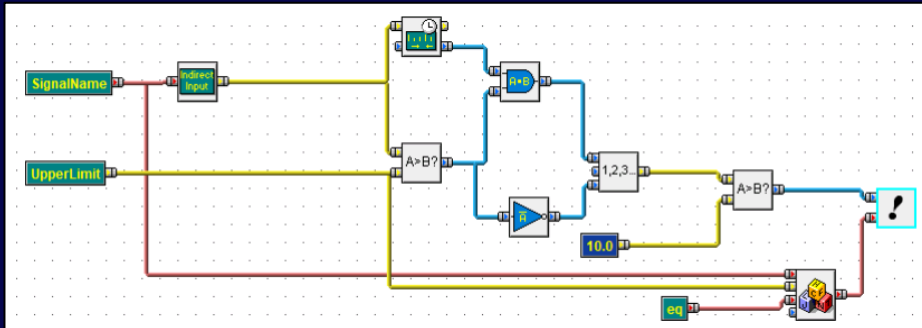
Prevention of Defects by Monitoring Equipment Health

Applies to Entire Manufacturing Process Steps

Monitoring of Tool Sensors prevents defects.
Customer Example: Proactive Monitoring exhaust flow sensor in a spin coater resulted in higher **Quality** & Yield.

Zero Defect Initiatives using FDC data

- Utilize FDC Trace and Summary data in Machine Learning based Analytics
- Fleet Management

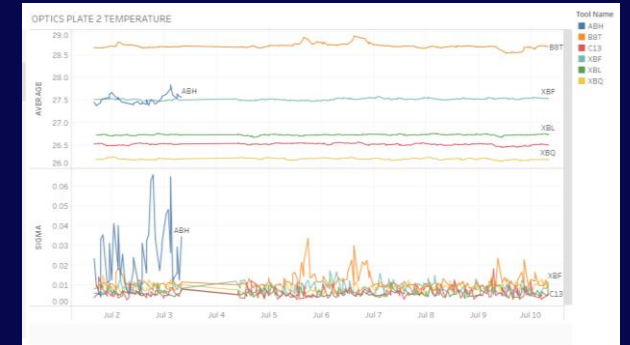


FDC Model

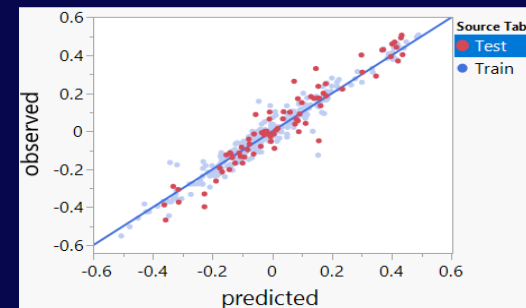
Health Monitor



Analysis Toolkit



Predictive Models



Q&A

Thank You

谢谢 | 謝謝

Danke

ありがとう

감사합니다

Obrigado

Merci

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