SEMI Europe 2023

BUSINESS BENEFITS OF **SmartSiC™** FOR SIC IN AUTOMOTIVE

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Munich - November 15th , 2023

01

SIC MATERIAL

An essential material for the success of the EV revolution

AUTOMOTIVE MARKET UPDATE

Positive trends

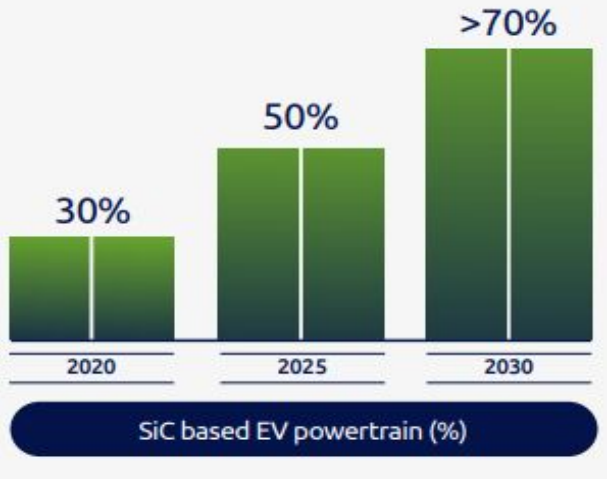
- Growing Light Vehicles worldwide market of +4.8% CAGR
- +22% CAGR for BEV's (more with Hybrid)
- +32% CAGR for SiC (Silicon Carbide) modules

- Multiple Chinese BEV's (BYD, SAIC,..) are mostly on SUV/Urban segment with IGBT inside
- Sedan/Berline segment dominated by Tesla challenged by Hyundai/ BMW/VW(Audi/Porsche) with SiC inside

BYD China
First vehicle with SiC

Tesla Europe
Best-selling vehicle of any kind in Q1

Hyundai Worldwide
>7 new models in 2023



POWERTRAIN – THE CORE OF THE ELECTRICAL VEHICLE (EV)

SiC ADDS VALUE AT SYSTEM/MODULE/DEVICE LEVEL AND ENABLES COST REDUCTION

POWERTRAIN COST: ~10,000$

Electric motor

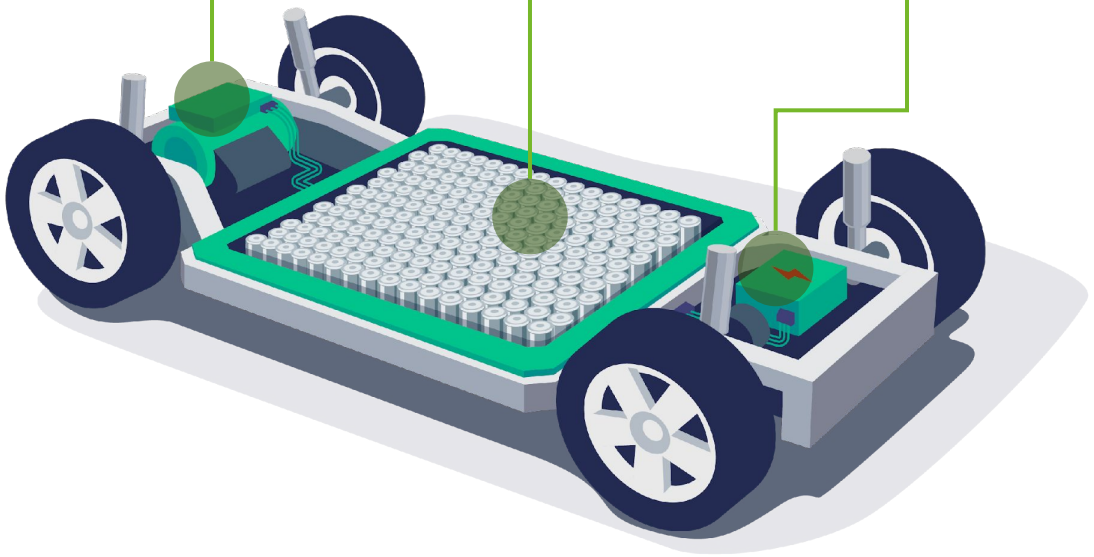
~1,100$

Battery pack & modules

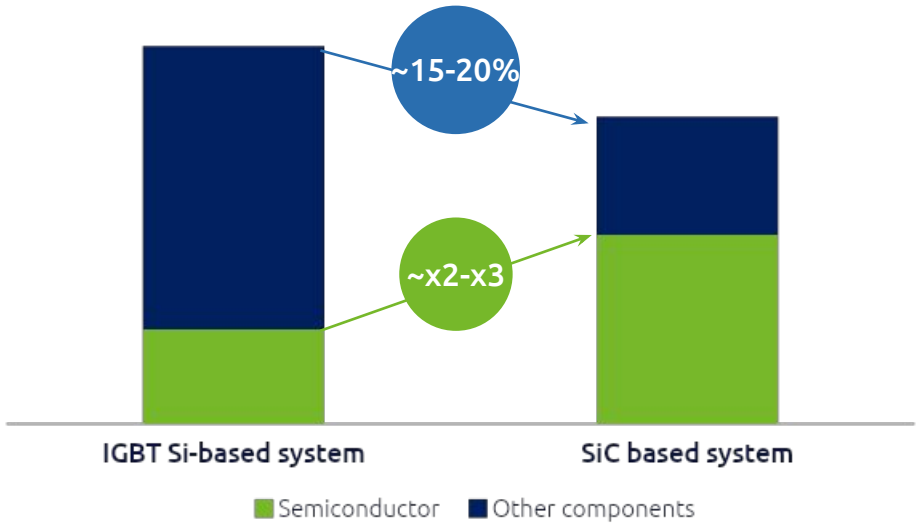
~8,000$

Power electronics

~1,500$



TOTAL SYSTEM COST: 15-20% REDUCTION



STANDARDIZATION OF 800V IN BATTERY ACCELERATES SiC ADOPTION

Source: AlixPartners, Bernstein, Infineon, Soitec estimates

SINGLE CRYSTAL SiC IS COSTLY AND ENERGY INTENSIVE BY NATURE

2500°C IS HALF OF THE TEMPERATURE AT THE SURFACE OF THE SUN

From Boule…

Slice

Edge Grind

Shape

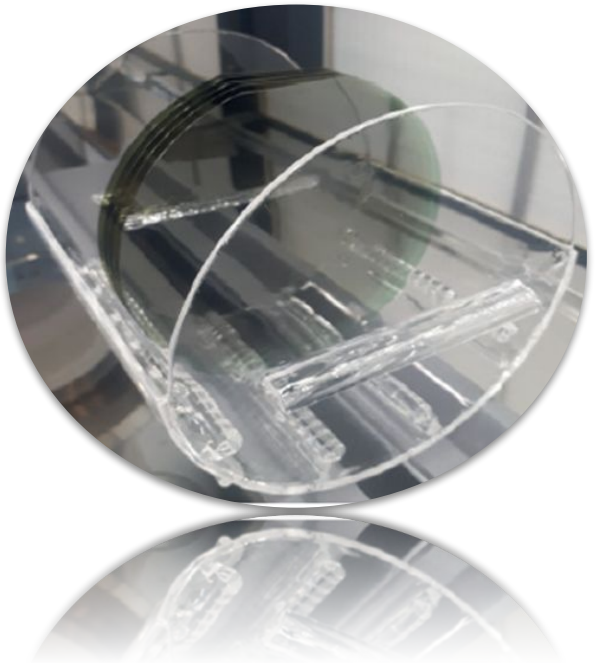
Polish

Clean

Epitaxy (optional)

… to Single Crystal SiC wafers

Device ready (SiC Wafers)

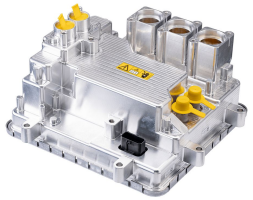


SiC Boule - 2 weeks at 2500°C
1 boule – 40/50 wafers
10/12 EVs per wafer

INNOVATIONS EVERYWHERE – MULTIPLE INITIATIVES TO REDUCE COST

SiC WAFER COST REDUCTION IS THE NAME OF THE GAME

OeM / Tier 1	IDM / Foundry	Crystal / Wafer
Highly integrated X-in-1 systems	**Cell pitch shrinking**	**Optimum boule usage:** ++ Good wafers within the same boule
Inverter optimization	**Epitaxy**	**Wafer productivity:** 150mm → 200mm
Inverter efficiency	**Chip optimization**	**Wafer optimization:** ++ crystal quality (BPD, TSD,..), ++ usable area



All these innovations are expected to increase Power Density AND reduce $/Amp of Devices/Modules

02

SOITEC

High-Tech leader in engineered substrates for 30 years

SOITEC HAS BUILT A UNIQUE POSITION IN THE SEMICONDUCTOR INDUSTRY

STRATEGIC PARTNERSHIPS IN THE ENTIRE SEMICONDUCTOR ECOSYSTEM

STRATEGIC SUPPLY AGREEMENTS

BULK MATERIALS

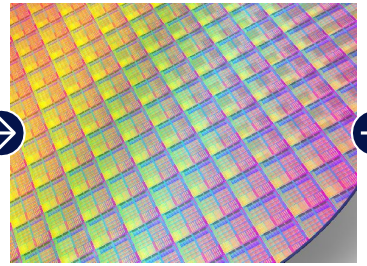
soitec

LEADING HIGH TECH SUPPLIER

ENGINEERED SUBSTRATES

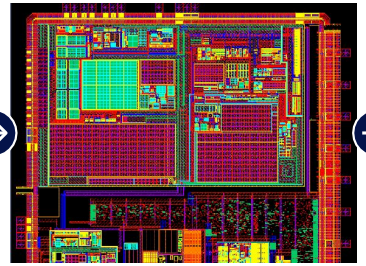
>3 Mwpy

JOINT DEVELOPMENT ROADMAPS



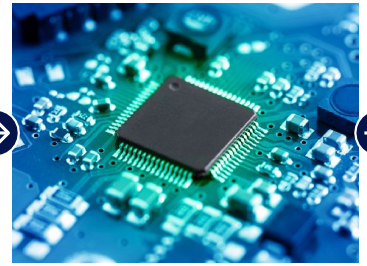
FOUNDRIES

DESIGN CAPABILITIES TO SUPPORT DEVICE DEVELOPMENTS



DESIGN/IDMs

TECHNOLOGY ENGAGEMENT



FABLESS

END MARKETS

MOBILE COMMUNICATIONS

AUTOMOTIVE & INDUSTRIAL

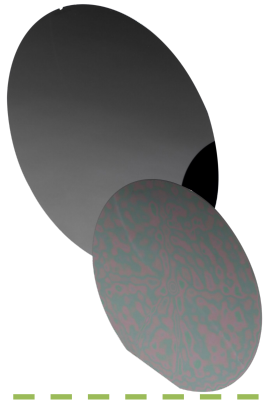
SMART DEVICES

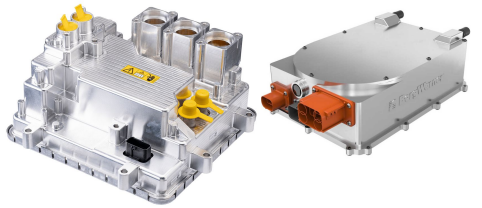
SmartSiC™, BECOMING KEY FOR NEW SiC-BASED POWER ELECTRONICS

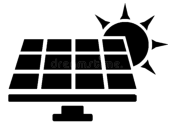
SOITEC IS A PURE-PLAYER ENGINEERED SUBSTRATE SUPPLIER

SiC Material → Engineered SmartSiC™ Substrates → SiC Foundries & IDM → Tier1 → OEM

soitec



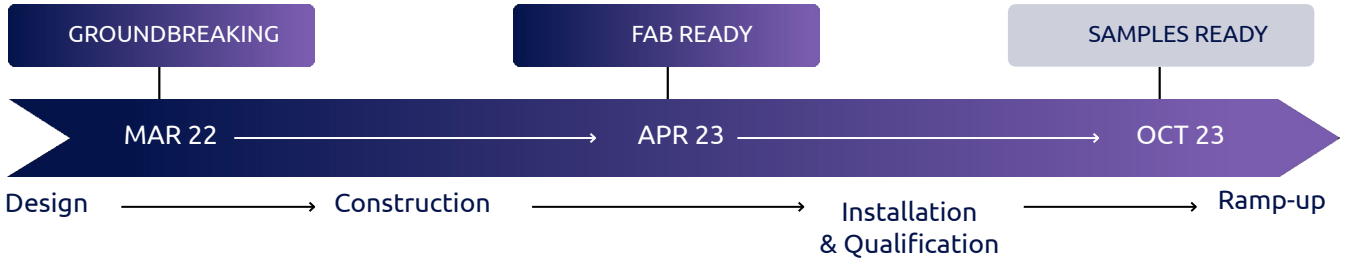




soitec

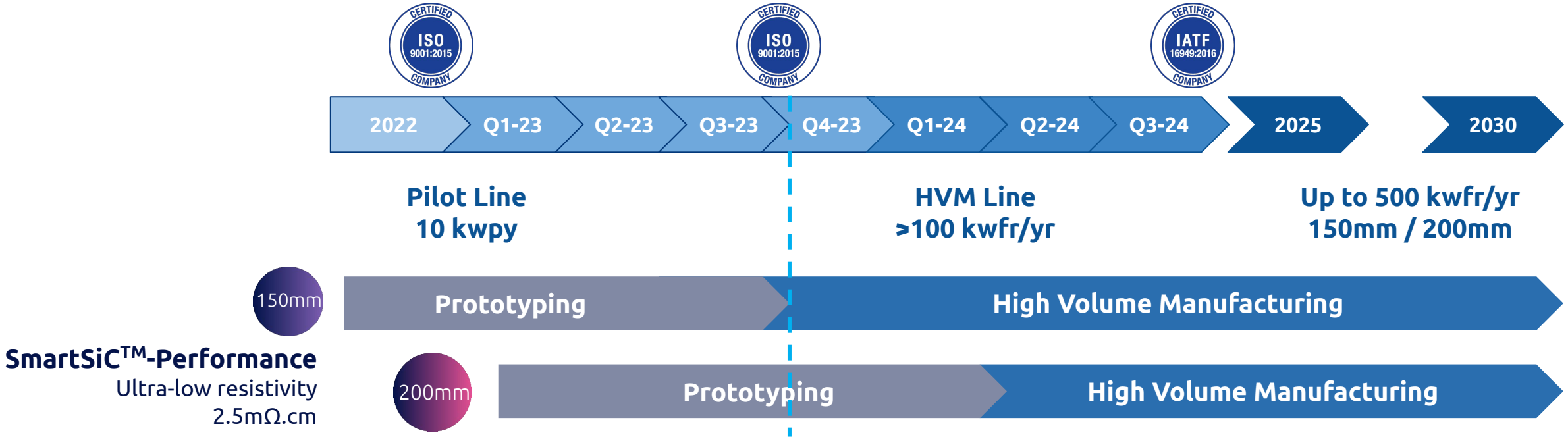
SmartSiC™ HVM FACTORY

NEW CLEANROOM FOR SmartSiC™ 500kwpy 150/200mm CAPACITY



SmartSiC™ RAMPING-UP TO HVM

FROM 10 KWPY PILOT LINE TO 500 KWPY-CAPABLE



HVM Capacity
150mm from Sep 2023

200mm from Apr 2024

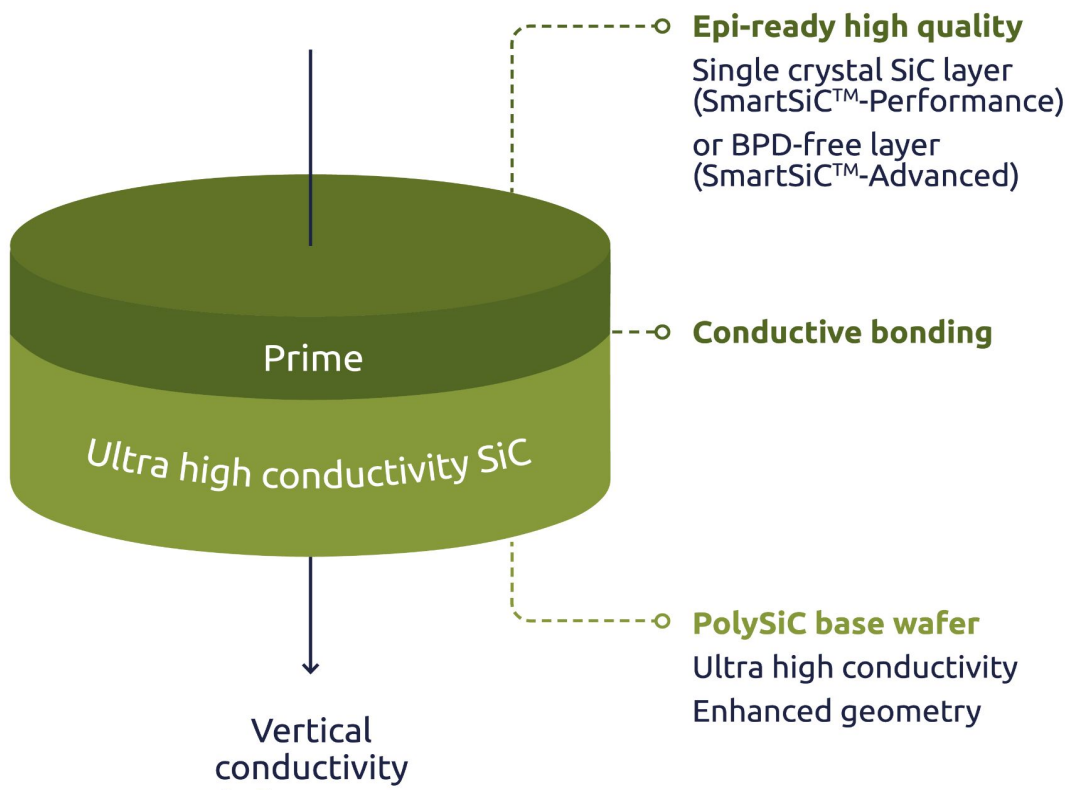
03

SmartSiC™

Unrivaled performance enabler for power devices

SmartSiC™ ENGINEERED SUBSTRATE

UNRIVALED VALUE PROPOSITION TO ENABLE SiC ACCELERATION



UNRIVALED VALUE PROPOSITION

>10x

Single crystal SiC wafer re-usability

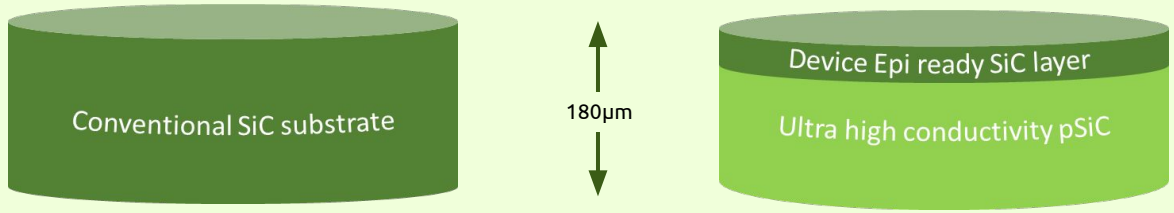
~8x

Poly Crystal SiC wafer higher conductivity

SmartSiC™, THE ENABLER FOR BETTER DEVICE PERFORMANCE

REDUCED RESISTIVITY BRINGS IMPROVED CURRENT DENSITY

LOWER SUBSTRATE R_{ON}.A



Standard SiC substrate | **SmartSiC™ substrate**

mSiC 20mΩ.cm	Substrate →	pSiC **2.5mΩ.cm**	Interface **10µΩ.cm²**
100 µΩ.cm²	BS metal contact →		**5µΩ.cm²**
460µΩ.cm²	Total R_{Subs}.A →		**60µΩ.cm²**

SmartSiC™ reduces the substrate contribution by 8x

A NEW PARADIGM FOR DEVICE PERFORMANCE

Customer Results on 1200V SiC MOSFET Devices

Parameter	A	B	C
Ron.A (mΩ.cm²)	2.7	2.5	2.5
Die thickness (µm)	180	150	110
Ron.A gain vs mSiC	**16%**	**15%**	**12%**

Customer Results on SiC Schottky Diodes Devices

Parameter	A	B	C
Rated Voltage (V)	650	1200	1200
Die thickness (µm)	180	180	180
R_{dyn} gain vs mSiC	**40%**	**30%**	**30%**

Diodes from ST

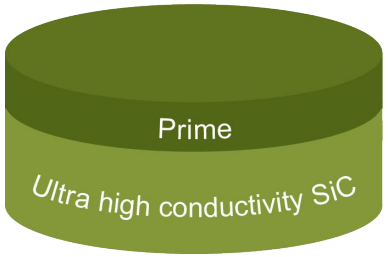
life.augmented

VALUE PROPOSITION

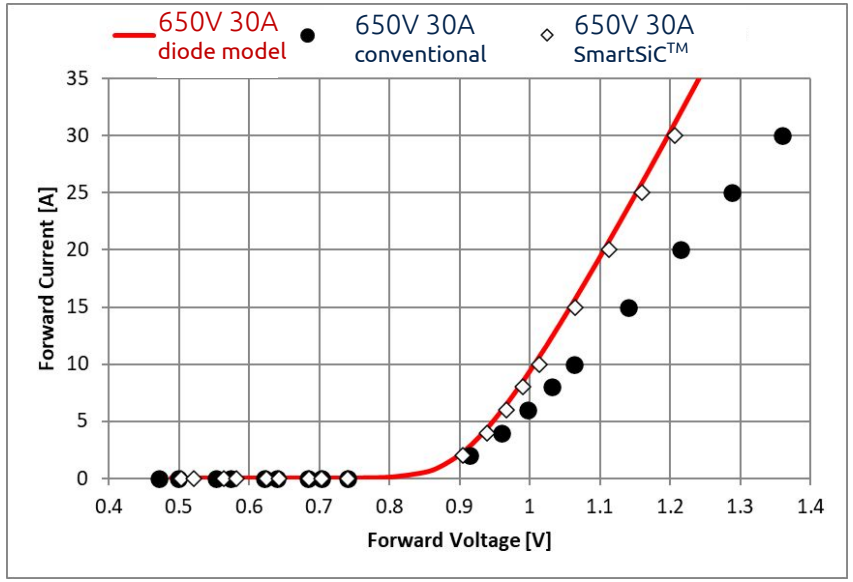
- High increase of number of producible wafers
- Maximize substrate value
- Higher manufacturing yield
- Device feature size reduction / RDSon improvement
- Copy & paste of MOSFET process flow
- Acceleration of the path to 200mm transition

Current industry solution (monocrystalline bulk)

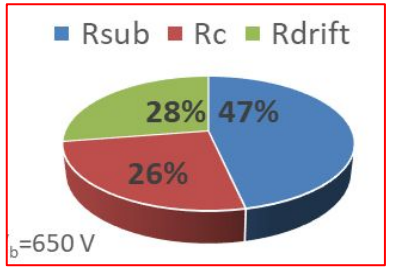
SmartCut™ 's engineered Epi-ready substrate solution



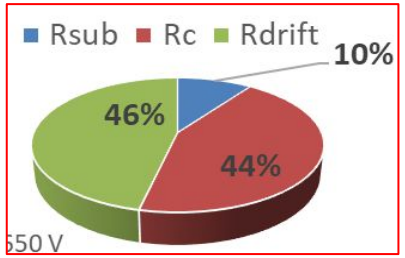
Experimental data on 650V SiC diode



mSiC



SmartSiC



Vf gain at rated current (30A): 150mV over 1.35 => 11% gain

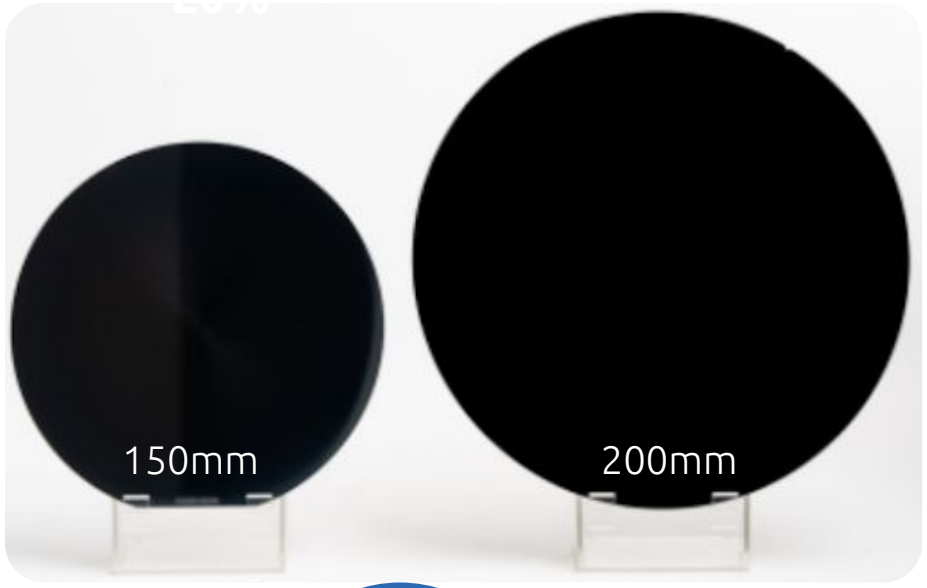
*ΔR @ RT = 30mOhm*mm²*

Courtesy of STMicroelectronics

soitec

SmartSiC™ IS READY FOR 200MM
DISRUPTIVE ACCELERATION FACTOR

SMARTSiC™ ENABLES 200MM

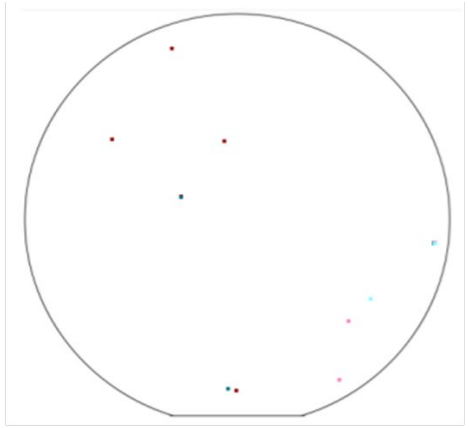


x1.82

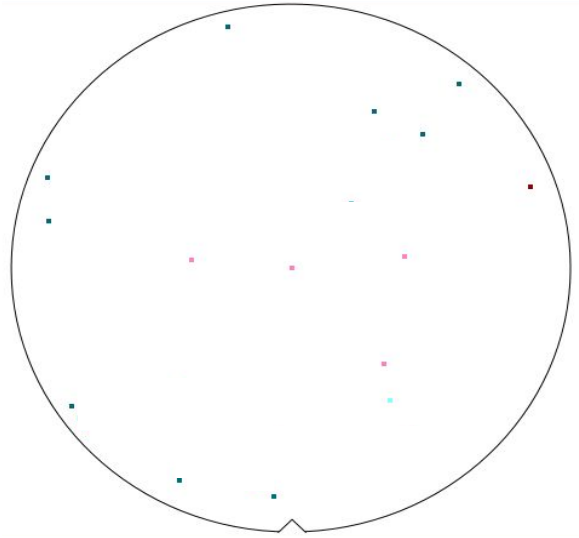
Higher usable area

SMARTSiC™ DEFECTIVITY MAKES YIELD IMPROVEMENT

150mm
Def 0.1/cm²



200mm
Def 0.1/cm²

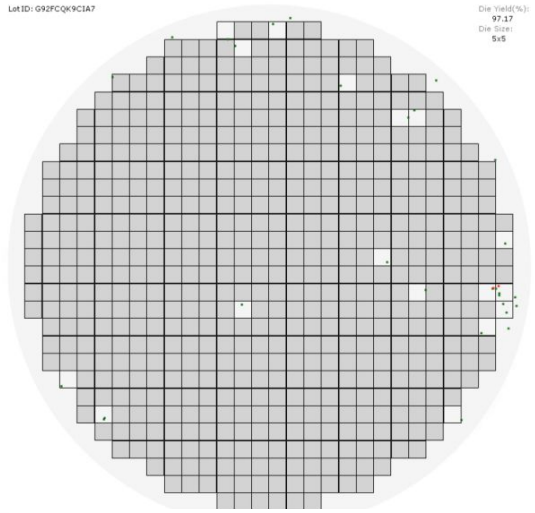


200mm defectivity performance matches 150mm

SmartSiC™ ENABLES MORE GOOD DIE/WAFER

(For 200mm wafer)	Constant Ron redesign MOSFET 1200V		
	Single Crystal SiC	**SmartSiC™**	**Gain**
Initial die size	25mm²	**21.3mm²**	**+15%**
Gross Die / Wafer	1108*	**1313***	**+18%***
Yield	**70%** by 2024	**74%** by 2024	**+4 %** by 2024
Good Die / Wafer	**776** by 2024	**969** by 2024	**+25%** by 2024

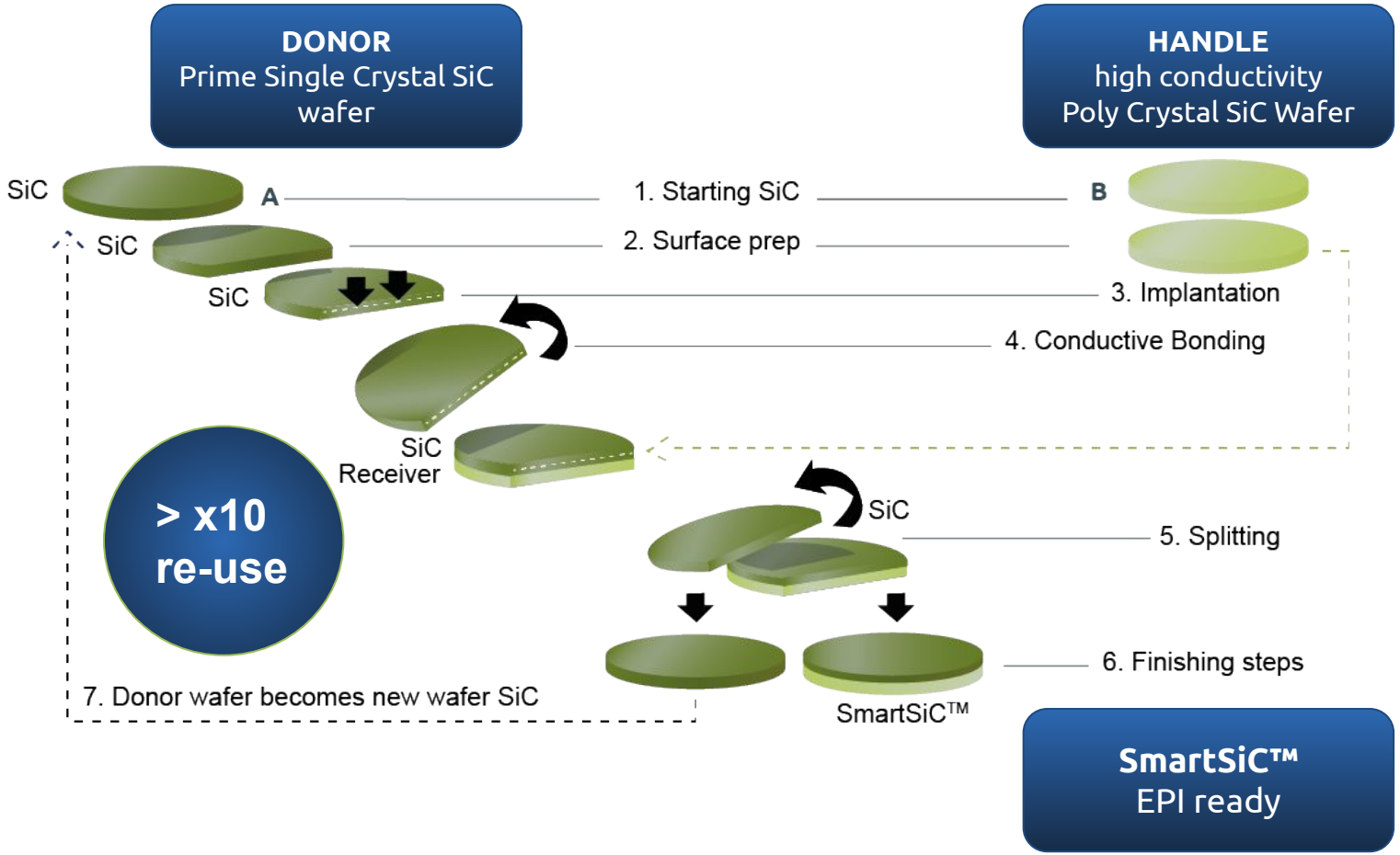
* 3mm EE and 80µm scribe lanes



IMPROVED Ron.A AT THE ORIGIN OF IMPROVED PRODUCTIVITY by 25%

SmartSiC™, A UNIQUE x10 REUSE CAPABILITY

LEVERAGING SOITEC HIGH VOLUME MANUFACTURING EXPERIENCE

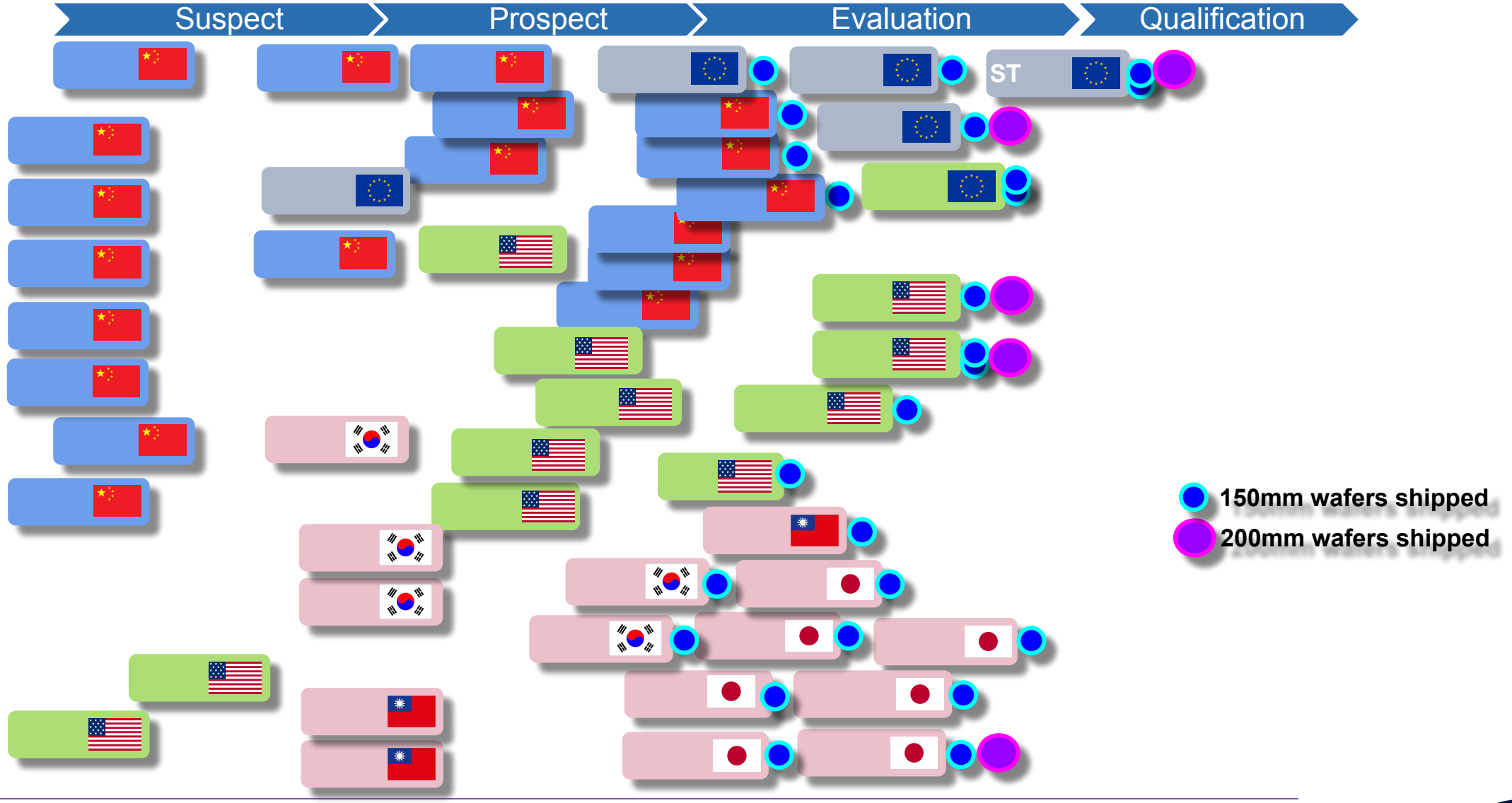


04

SmartSiC™

What can it do for you ?

SmartSiC™, WORLD-WIDE DEPLOYMENT ON-GOING



Thank you!

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SmartSiC™
Greener Faster Better

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SEMICON® EUROPA