



Epitaxial Growth of SiGe/Si Multi-Layers for Advanced Logic Devices

Rami Khazaka and Wonjong Kim

November 16, 2023



Agenda

1

Overview and challenges

2

1x1 NS on undoped Si wafer

3

2x2 and 3x3 NS on undoped Si wafer

4

Conclusion



Overview

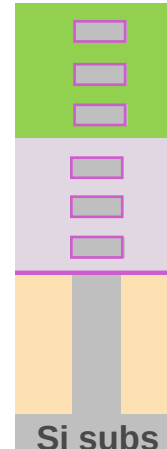
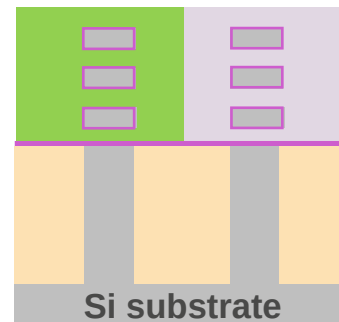
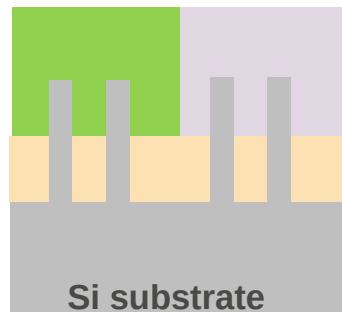
IMEC ITF WORLD



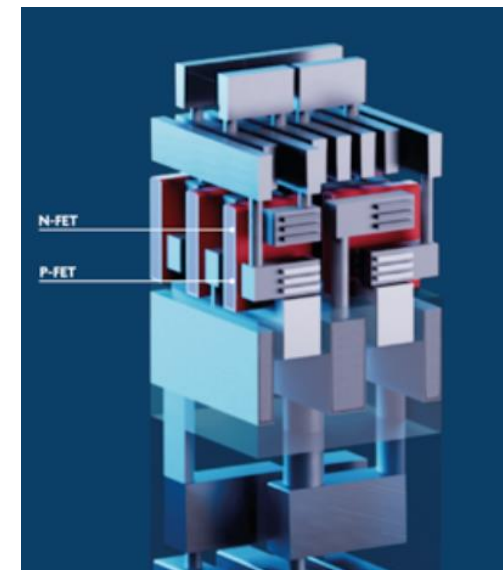
FinFET

GAA

CFET



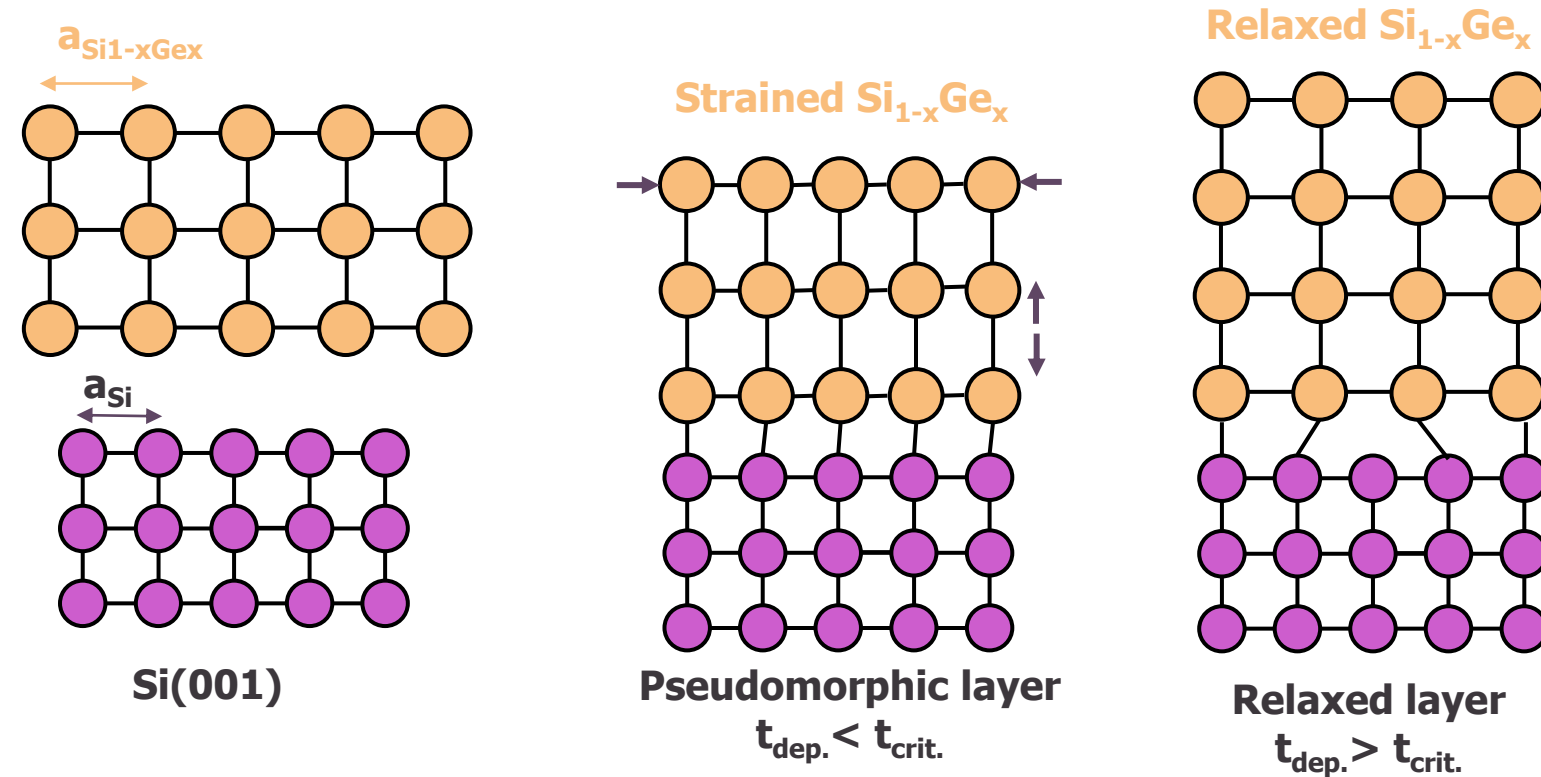
- GAA and CFET require epitaxial layer as first building block of the final device
- Strict requirements on epi quality:
- **Fully strained stack without defects**
- **Smooth surface morphology**
- **Sharp interface transitions from SiGe $\leftrightarrow$ Si**
- **High throughput**



Source: IMEC



Layer relaxation



$$a_{\text{SiGe}}(x) = 5.43105 + 0.1988x + 0.028x^2 \text{ (\AA)}$$

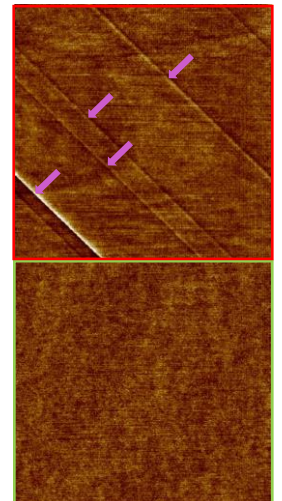
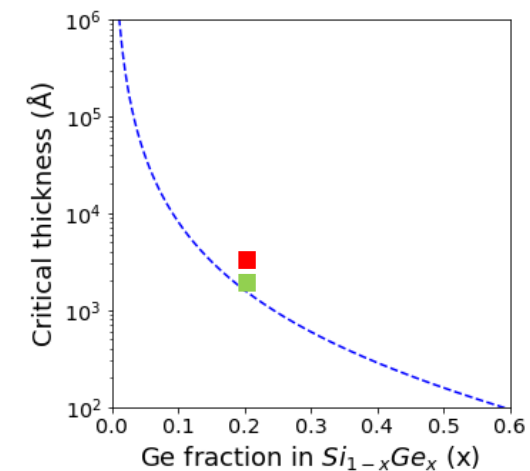
$$f = \frac{a_{\text{SiGe}} - a_{\text{Si}}}{a_{\text{Si}}} \approx 0.042x$$

Where x is the Ge content in the layer $\rightarrow$ higher Ge content leads to higher mismatch

$$h_c = \frac{1.9 \times 10^{-2}}{f^2} \ln \frac{h_c}{4} \text{ (\AA)} \quad [1]$$

Where h_c is the critical thickness $\rightarrow$ higher Ge content leads to lower critical thickness

Higher Ge content would induce earlier relaxation leading thereby to high density of misfit dislocation

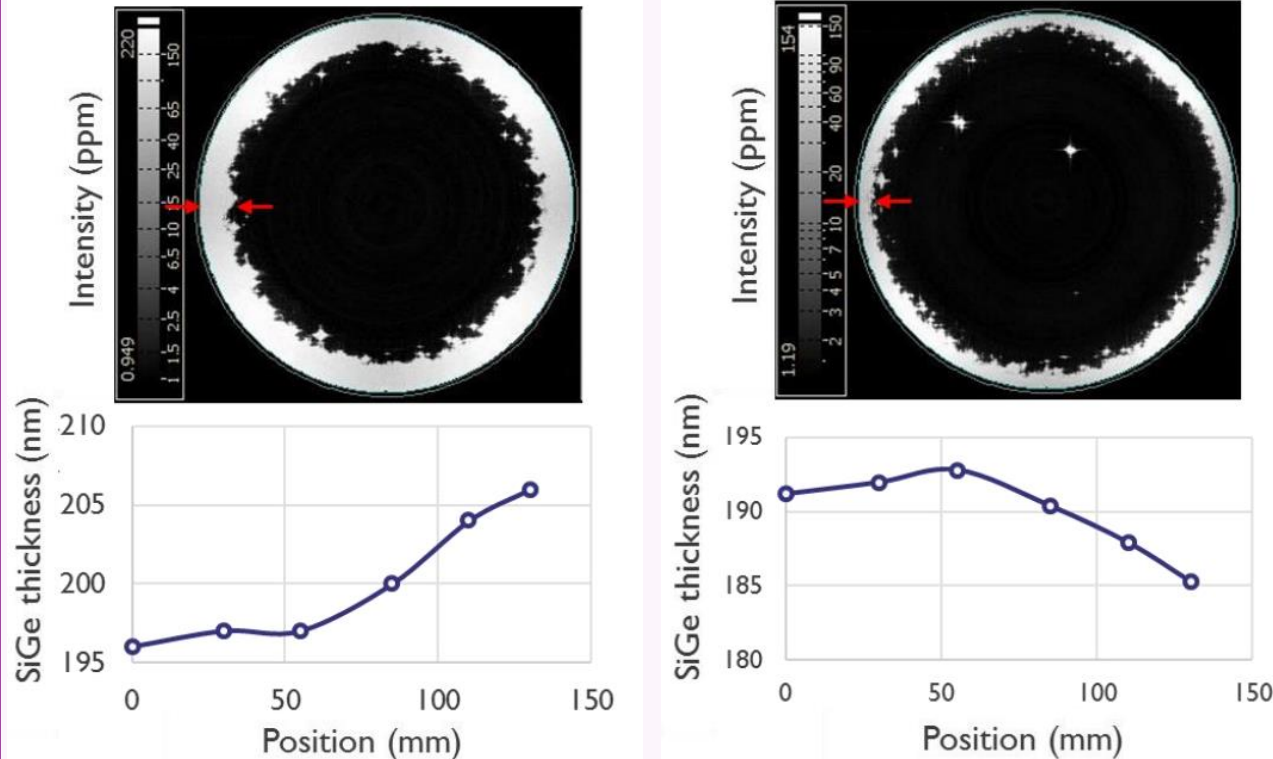




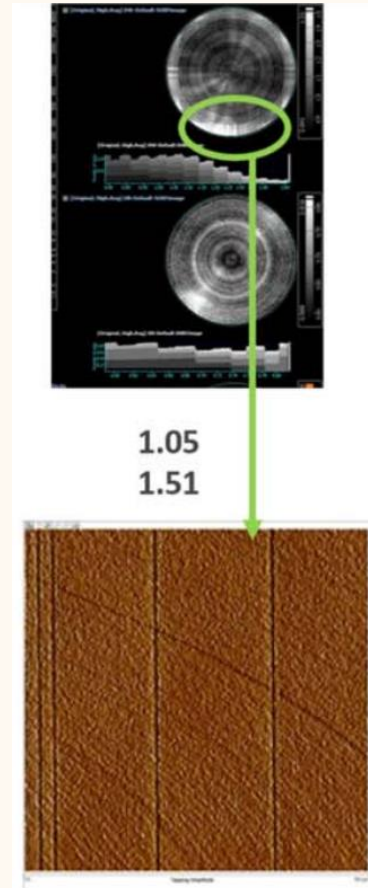
Relaxation at wafer edge

C. Porret et al ECS J. Solid State Sci. Technol. **8** P392 **2019**

R. Loo et al CS J. Solid State Sci. Technol. 10 014001 **2021**



Relaxation at the edge appears prior to center relaxation, despite thinner thickness



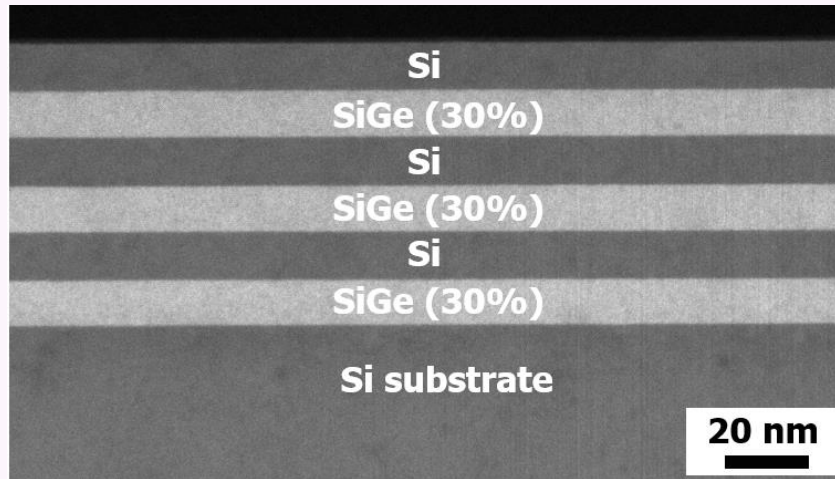
460 nm Si on top of **89nm SiGe (25%)** shows relaxation at wafer edge

- ❑ Once close to critical thickness, relaxation is initiated at wafer edge leading to significant area loss



CFET stack challenges compared to GAA

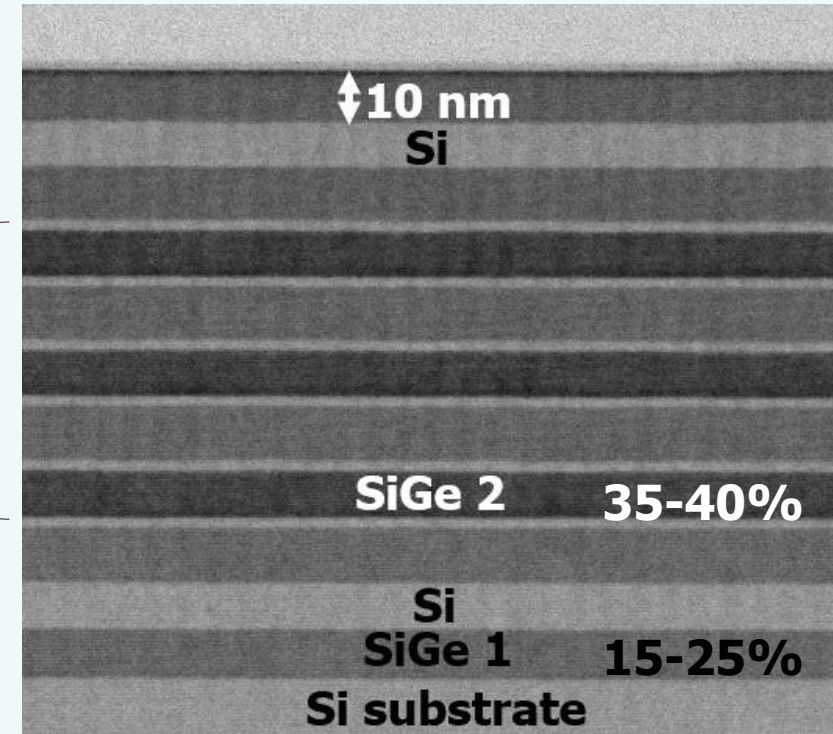
GAA



- 60 nm in total for 3 bilayers
- 3 SiGe layers
- Max Ge 30%

CFET

MDI



- 108 nm in total for 1x PFET and 1x NFET
- 9 SiGe layers, including 3 SiGe layers with high Ge content (38%)
- 24 nm of SiGe 38% and 54 nm of SiGe 22%

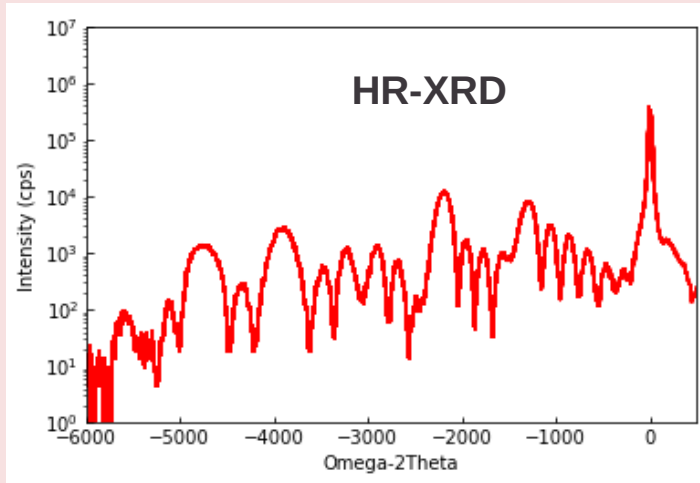
CFET stack is more challenging compared to GAA stack:

- ☐ Thicker overall stack
- ☐ Higher Ge content is needed

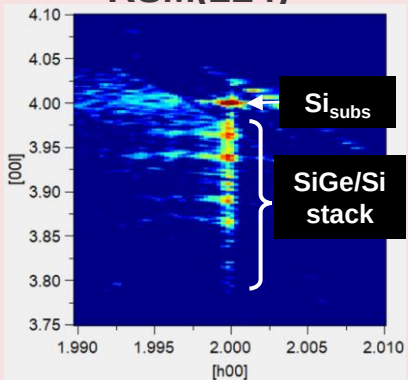


CFET stack characterization @ wafer center

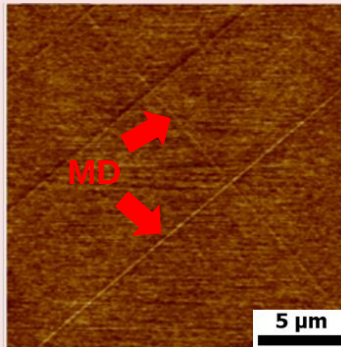
Partially relaxed stack



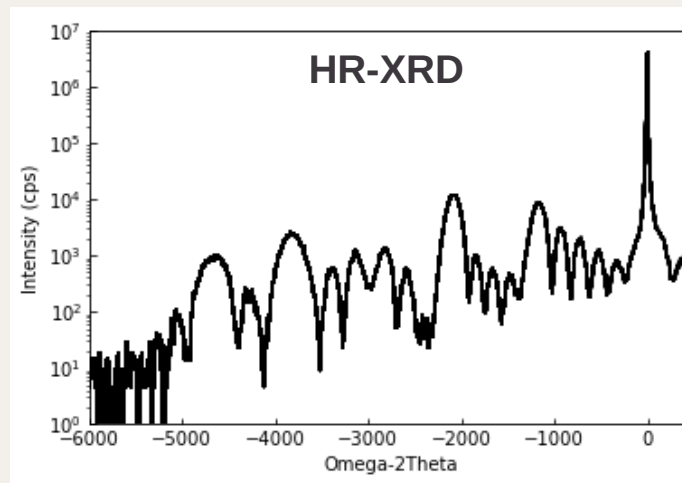
RSM(224)



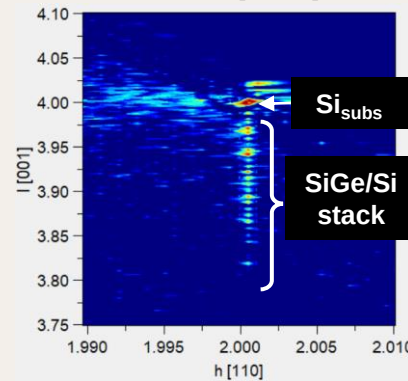
AFM



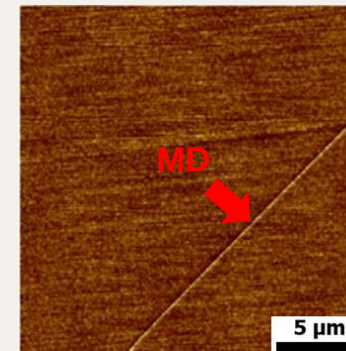
Strained with few defects



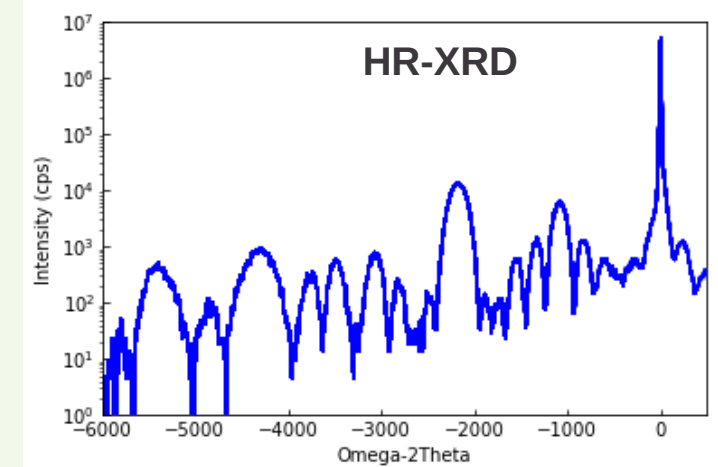
RSM(224)



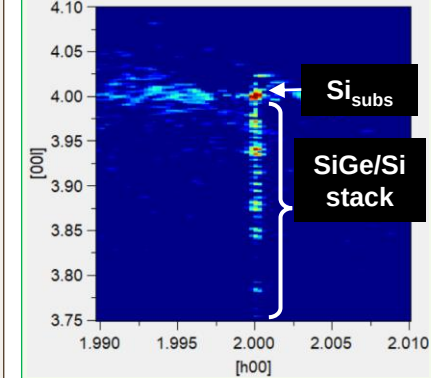
AFM



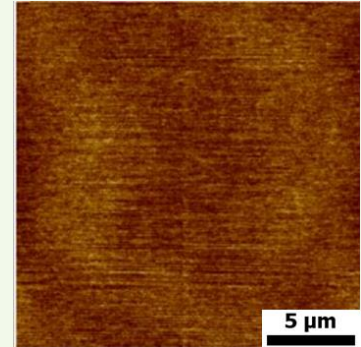
Defect-free stack



RSM(224)



AFM

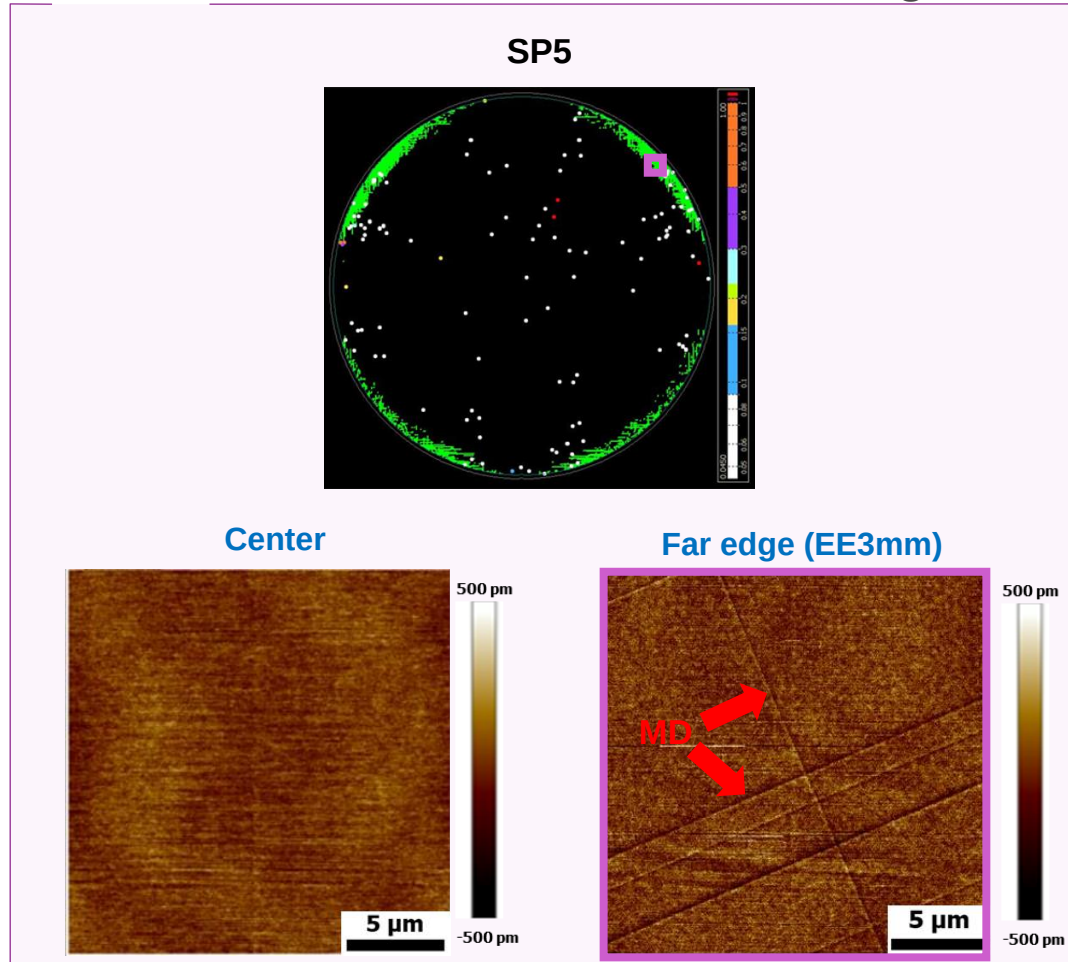


- ❑ Low density of defects could be only detected by surface sensitive techniques
- ❑ Defect-free at wafer center could be achieved by proper tuning of growth conditions

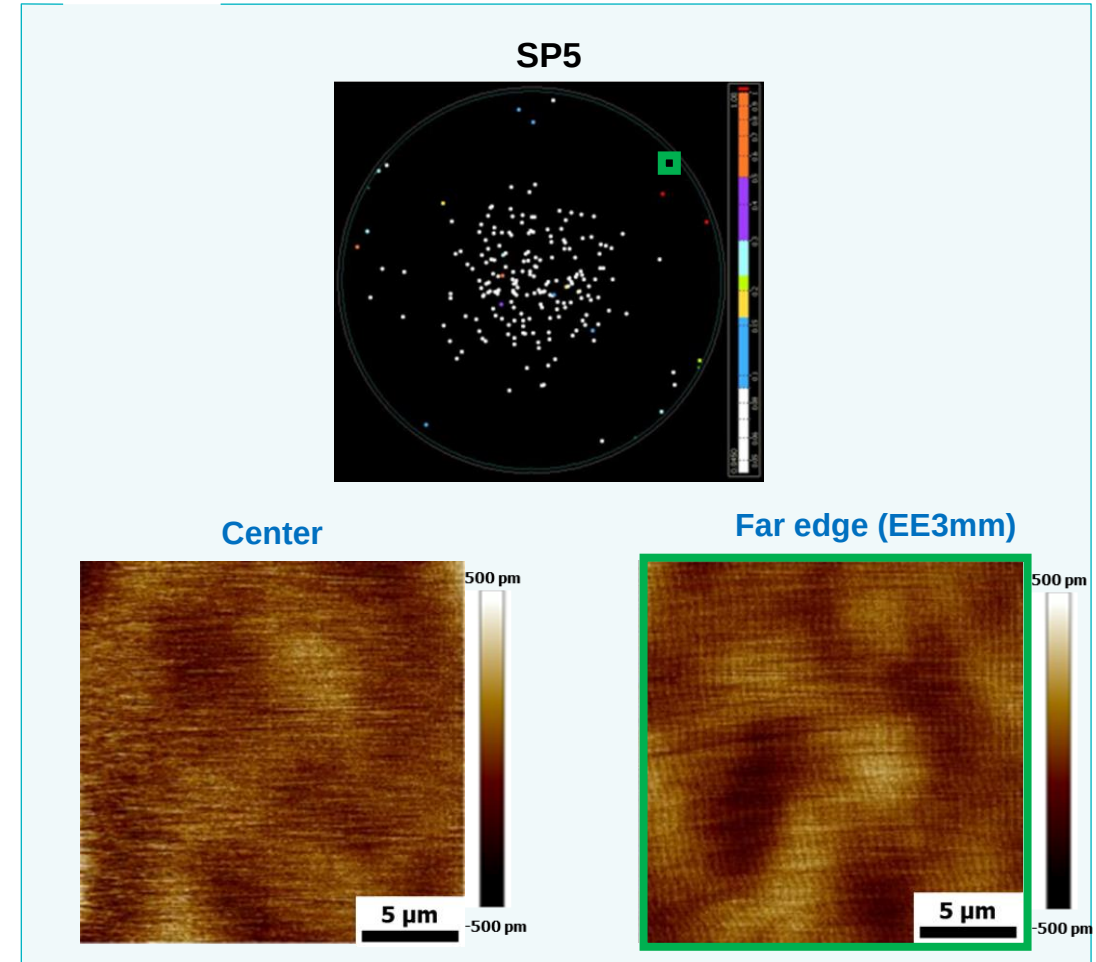


CFET stack characterization @ wafer edge

Partial relaxation at wafer edge



Defect-free wafer

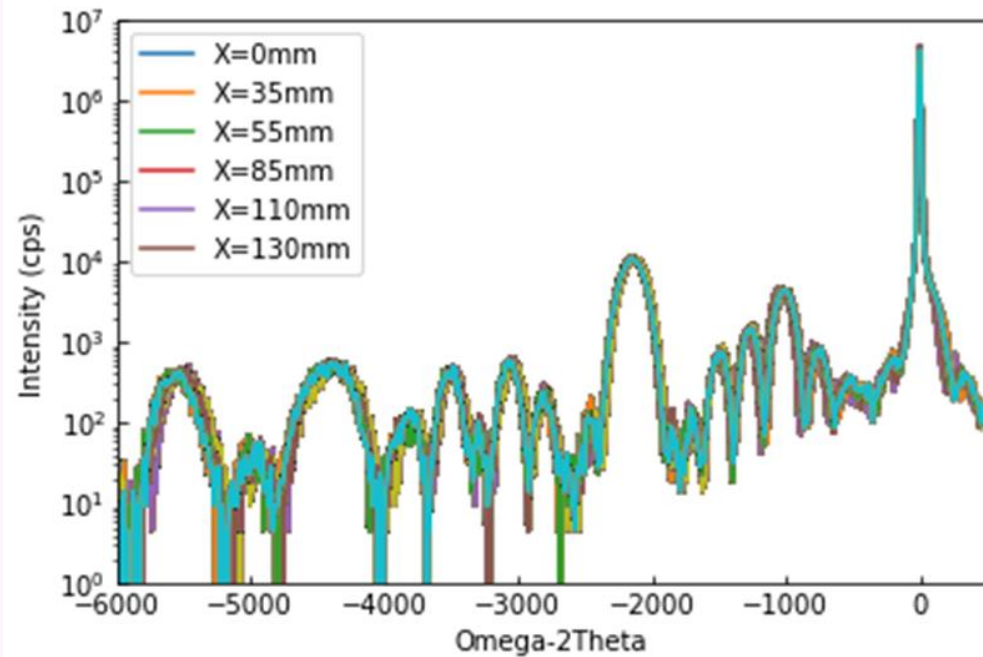


- ❑ Defects at wafer edge could be eliminated by optimizing process conditions
- ❑ **Defect-free stack at full wafer could be achieved**

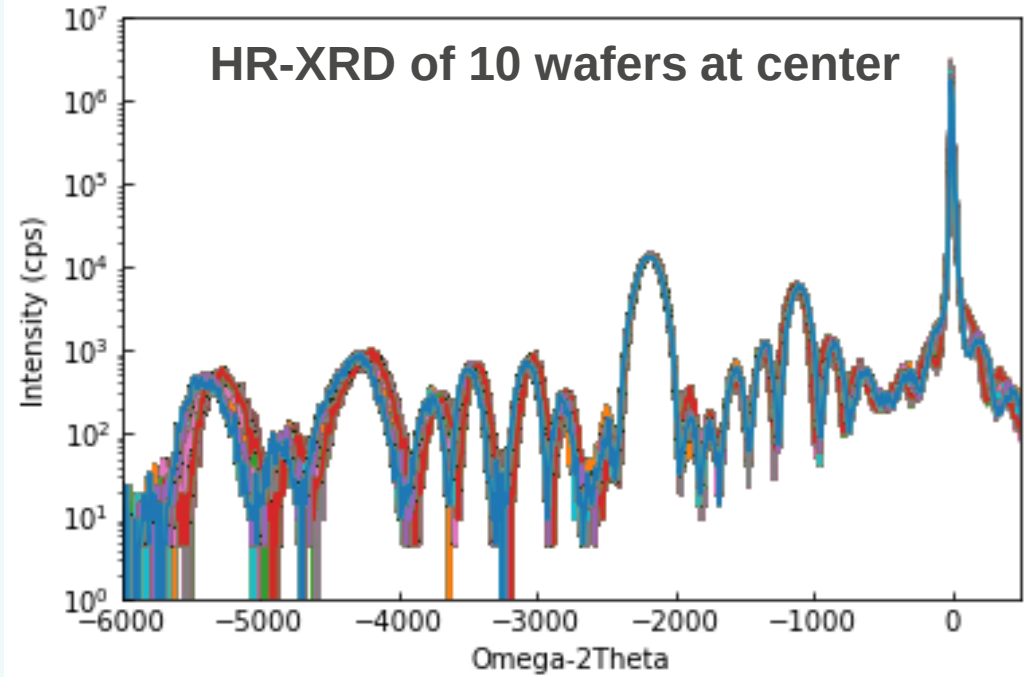


CFET stack uniformity and repeatability

WiW uniformity



WtW uniformity

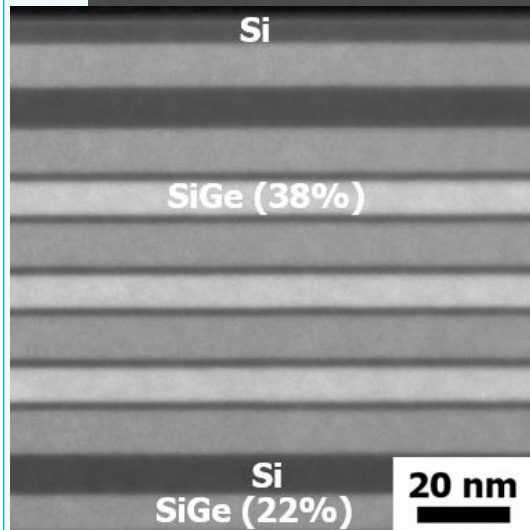
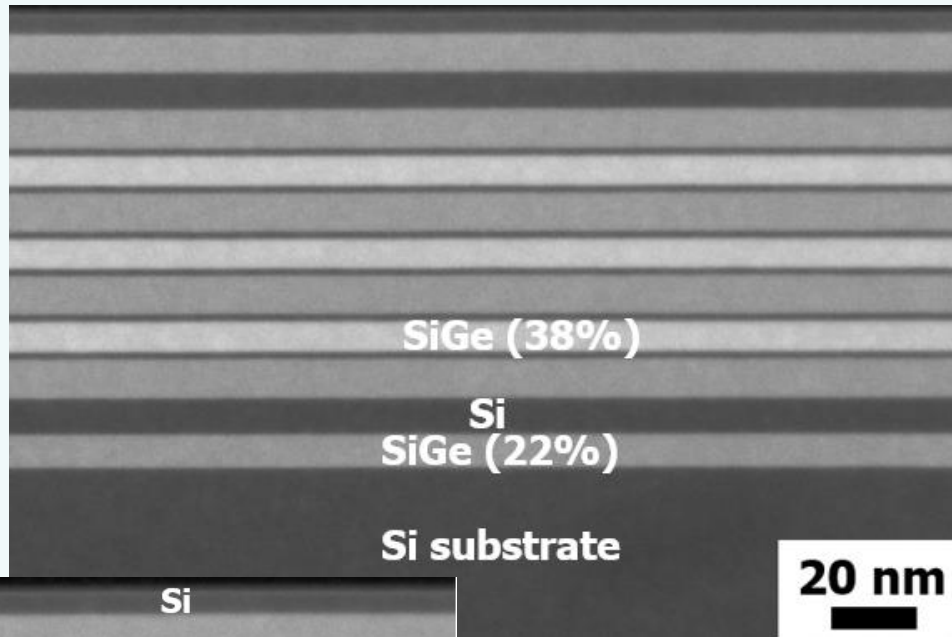


☐ Good with in wafer and wafer to wafer uniformity



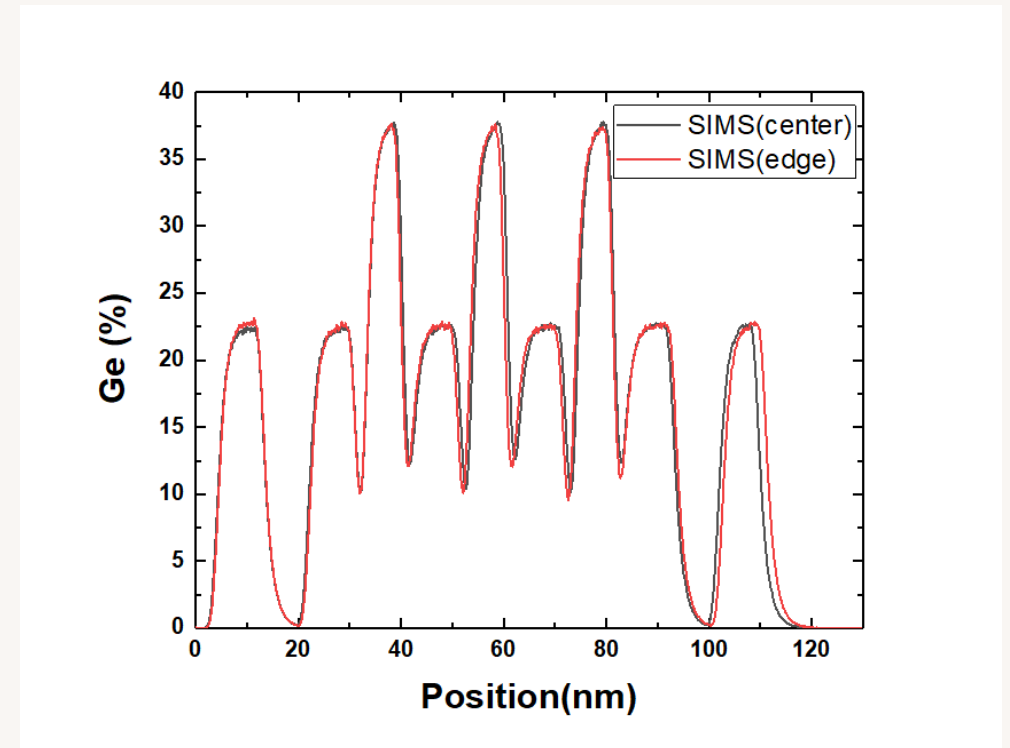
CFET stack advanced characterization

TEM



Smooth surface morphology,
no defect and sharp interfaces
as attested by TEM

SIMS

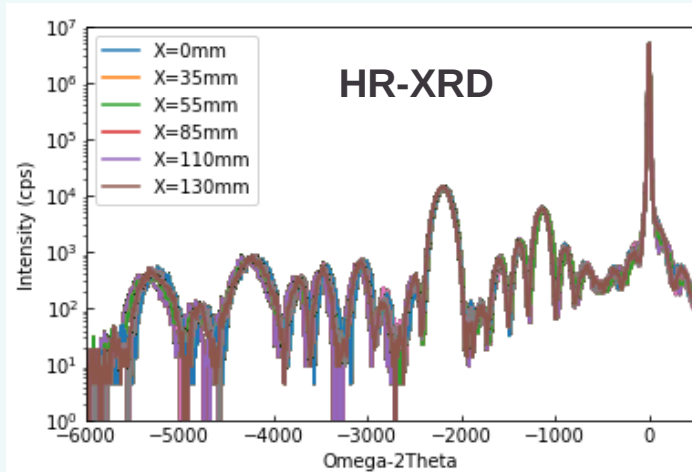


SIMS shows uniform Ge and thickness
uniformity across wafer

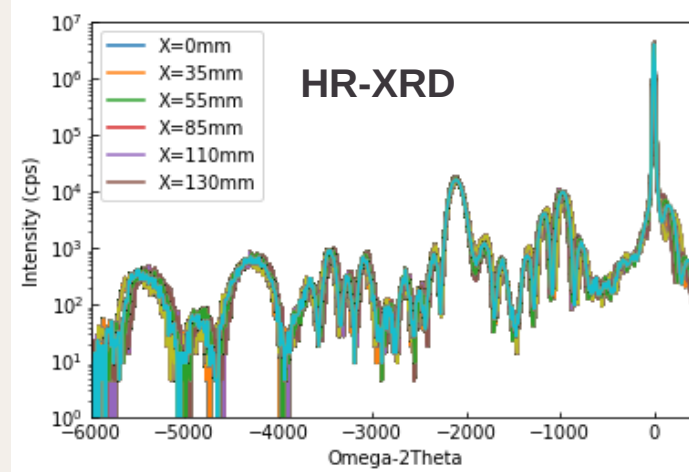


CFET stack with different multiple NS

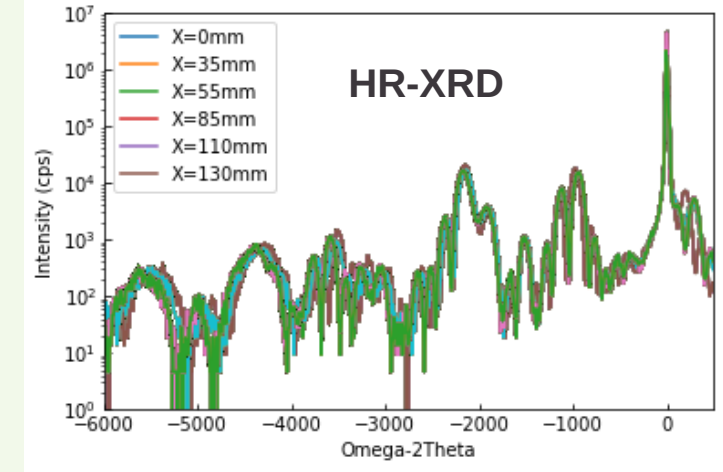
1x1



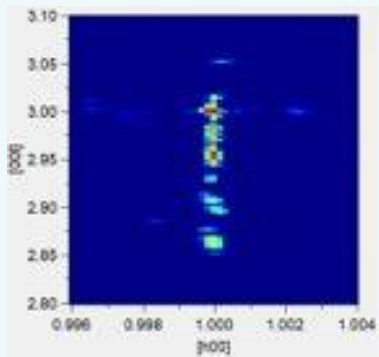
2x2



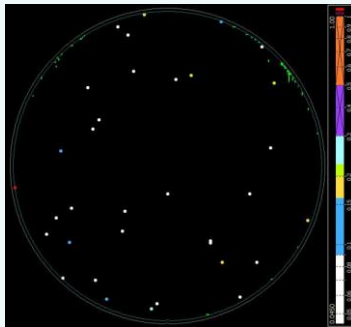
3x3



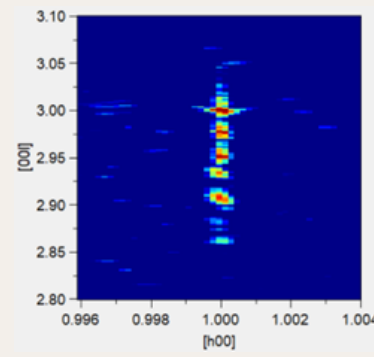
RSM(113)



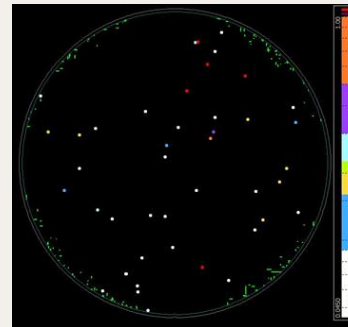
SP5



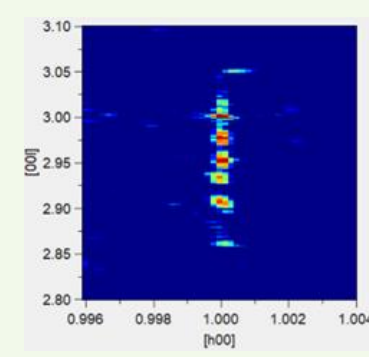
RSM(113)



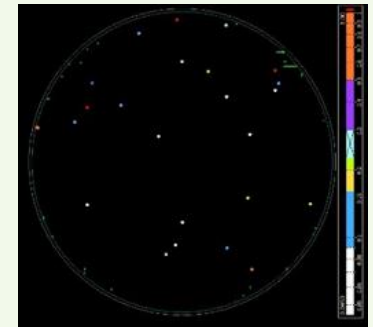
SP5



RSM(113)



SP5

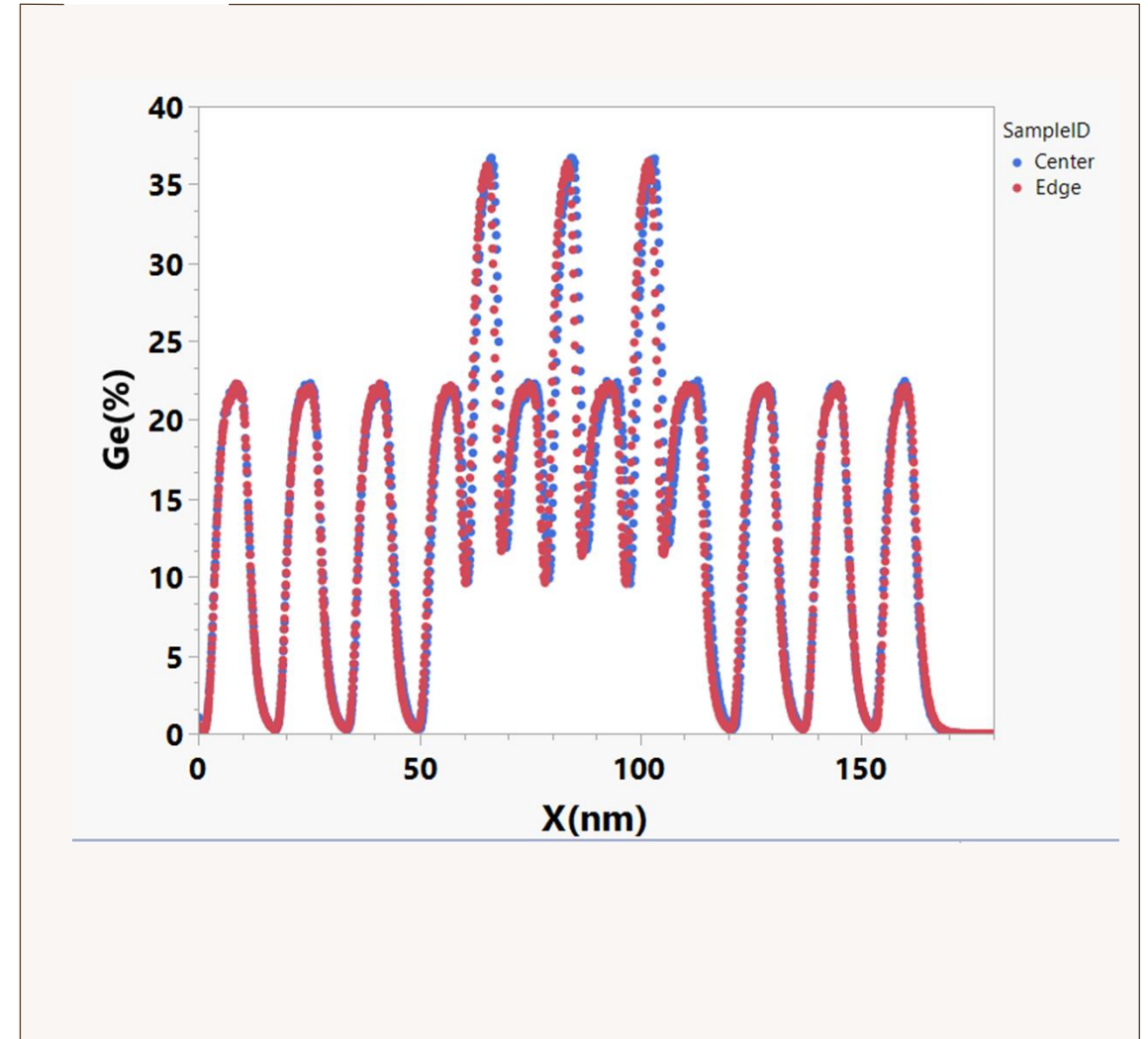
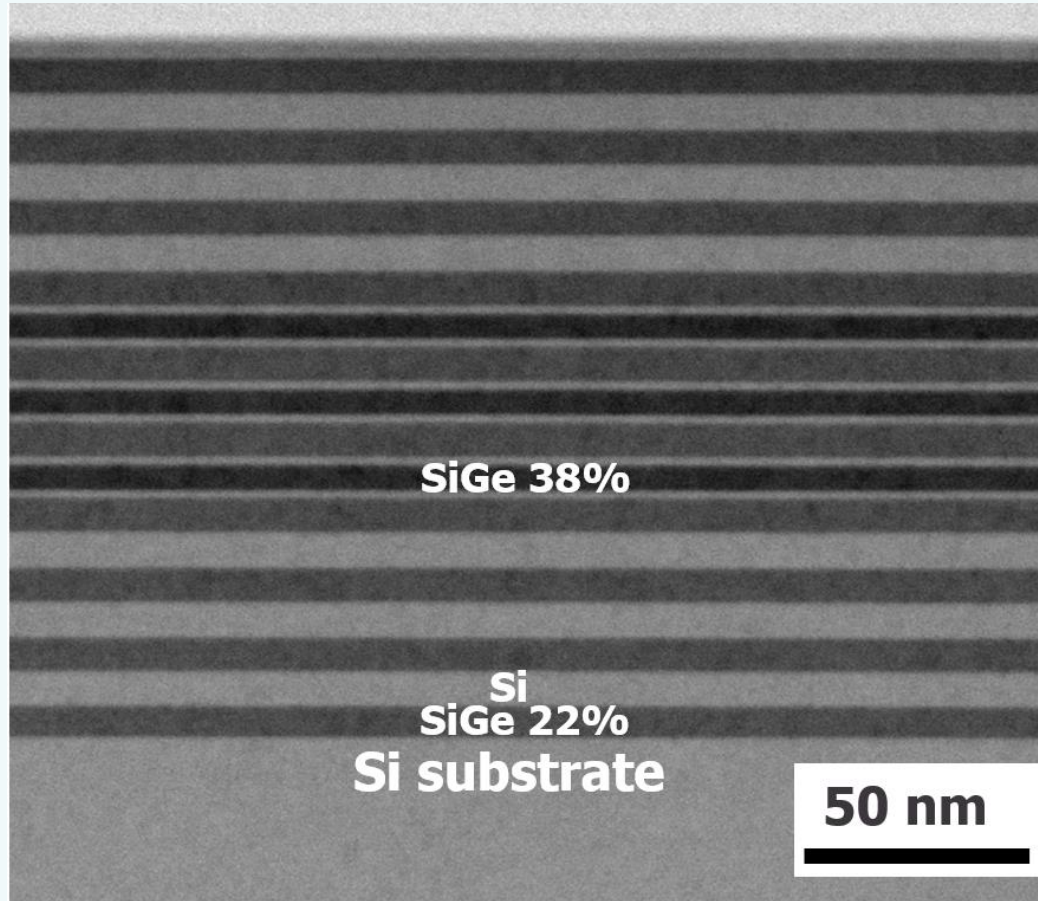


❑ Good crystal quality maintained on full wafer for 2x2 and 3x3 NS



3x3 CFET stack advanced characterization

TEM



- ❑ Smooth surface morphology, no defect and sharp interfaces as attested by TEM
- ❑ SIMS shows uniform Ge and thickness uniformity across wafer



Conclusion

MDs density reduction/elimination both from wfr center & edge confirmed via different techniques

Sharp SiGe to Si interface transitions could be achieved

Good layer to layer, Within wafer and wafer-to-wafer uniformity is obtained

Feasibility of multiple NS options while maintaining excellent crystal quality was demonstrated

Thank you