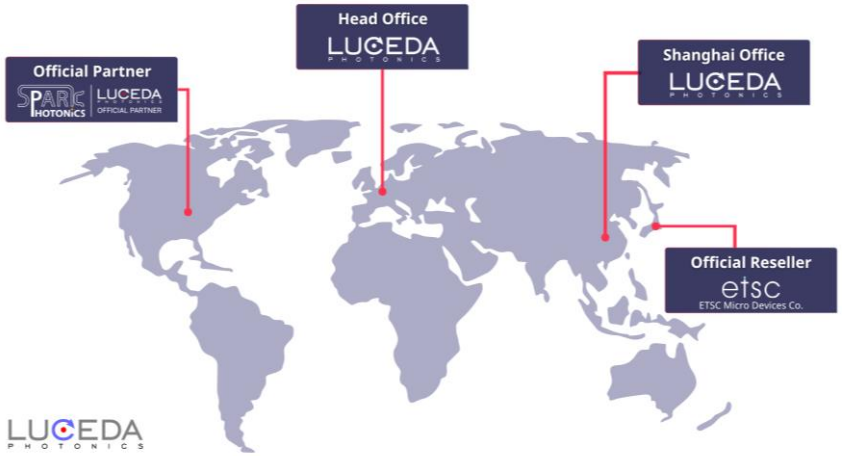
LUCEDA PHOTONICS

Photonic IC Design
Innovation and scalability

Pieter Dumon

November 14th, 2023 – SEMICON Europa TechArena

Luceda Photonics

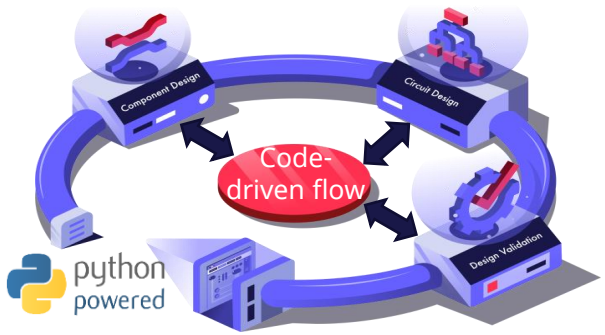


Design kits – foundry & OSAT

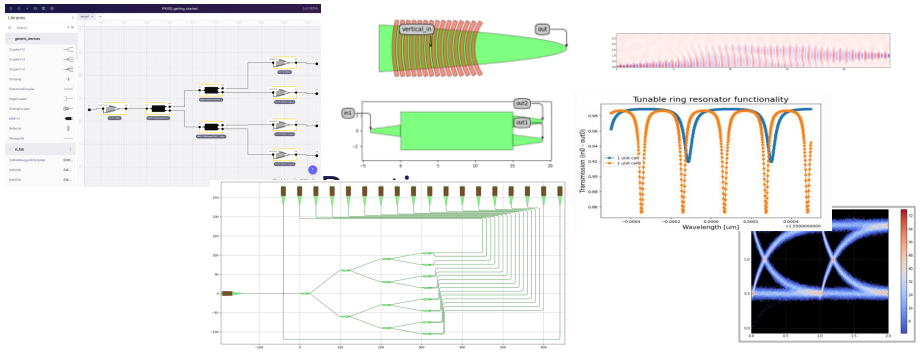
SMART PHOTONICS · amf · leti · SITRI · CompoundTek · LIGENTEC · imec · SILICON PHOTONICS · ihp · Fraunhofer HHI · Tower Semiconductor · imec PIX4life · AIM PHOTONICS · CORNERSTONE · IMECAS · SiEPIC FAB · phix · Tyndall National Institute · OpenLight · ALUVIA · UMEC · SiPhotonIC TECHNOLOGIES · LIONIX INTERNATIONAL

Help photonic IC designers enjoy the same powers as electronic IC designers

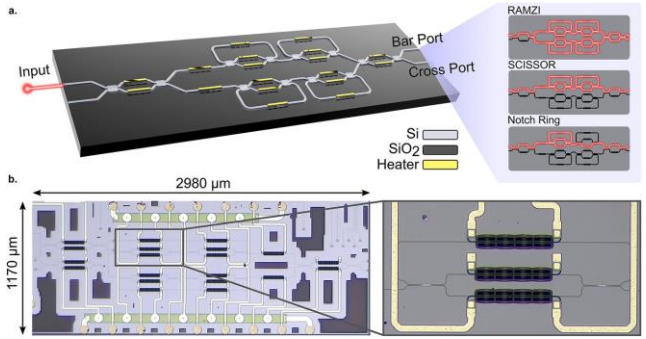
Luceda Photonics Design Platform



Full flow: schematic – layout – PnR - device model - simulation

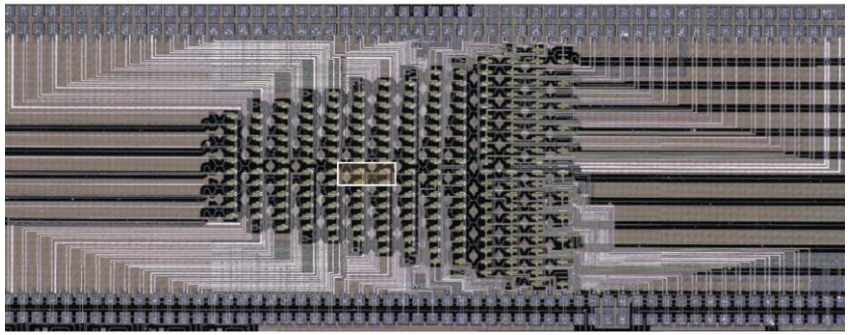


Microwave photonics



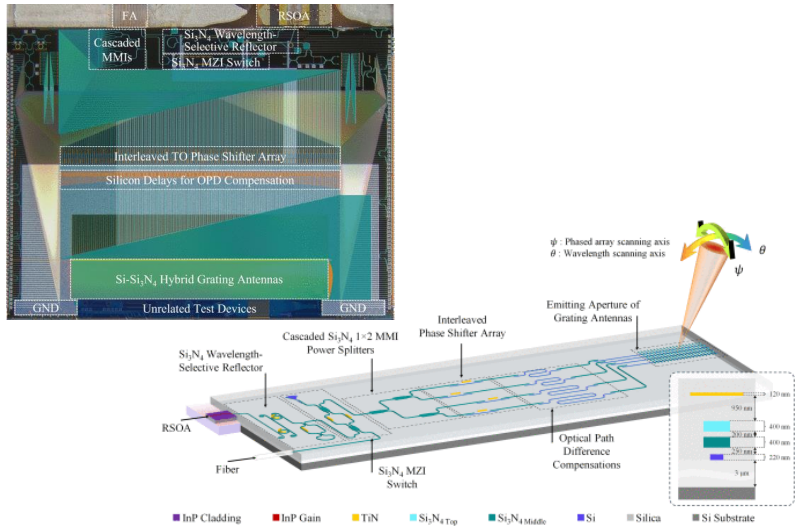
C. Catalá-Lahoz et al, APL Photonics. 8(11), 2023
doi:10.1063/5.0169544

Quantum photonics



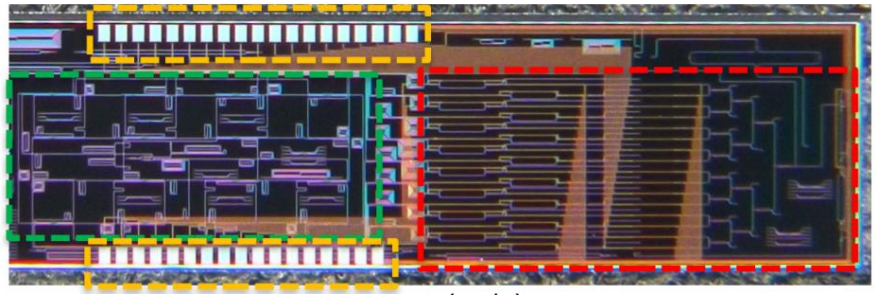
N. C. Harris et al. , Nanophotonics, vol. 5, no. 3, 2016
doi: 10.1515/nanoph-2015-0146

LiDAR



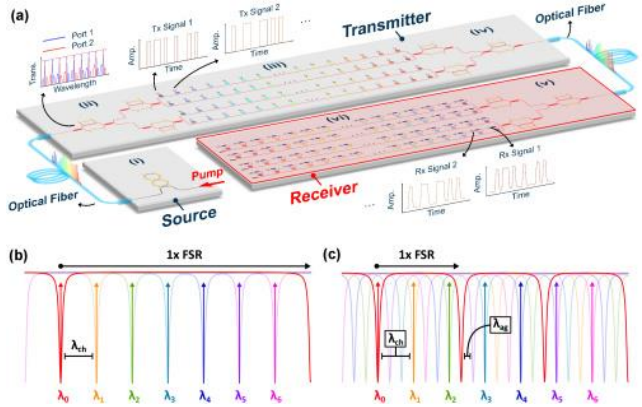
W. Xu et al. , J. Lightwave Technology, 41(3), 2023
doi: 10.1109/JLT.2022.3204096

Reservoir computing / ML / AI



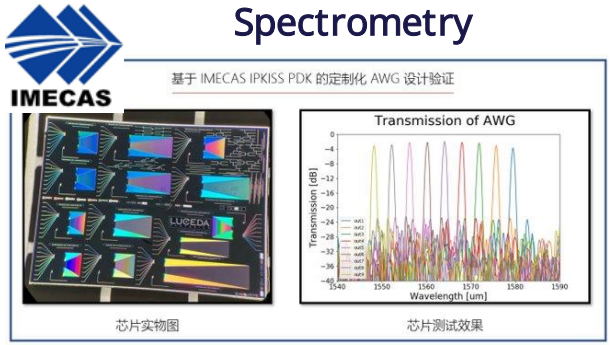
C. Ma et al. , Optics Express, 31 (21/9), 2023
doi:10.1364/OE.502354

High-speed data communication

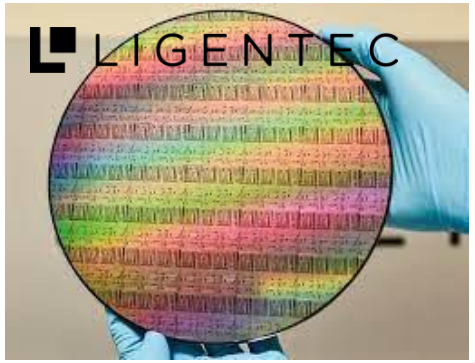


A. James et al. , Optica 10 (7), 2023
doi:10.1364/OPTICA.491756

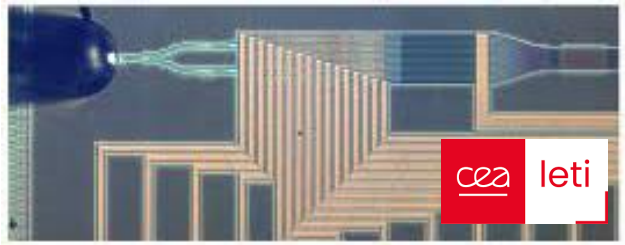
Spectrometry



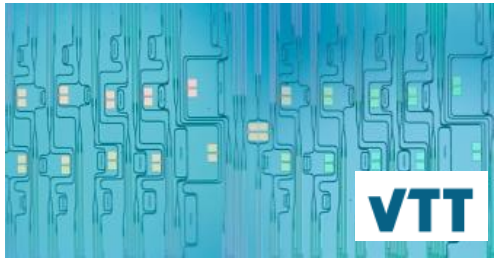
Silicon Nitride



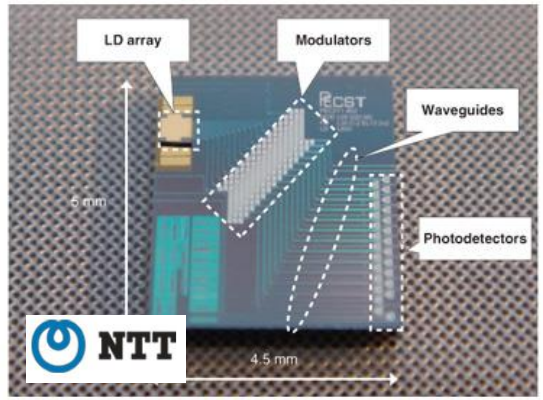
Silicon Photonics (sub-µm)



Silicon Photonics (multi-µm)

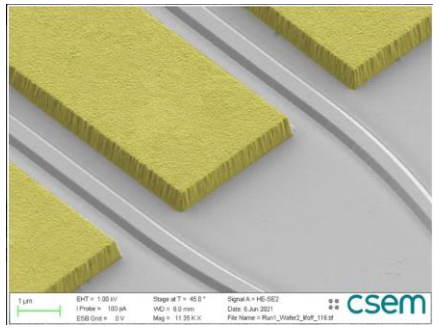


InP on SiPhotonics
Hybrid integration



Alumina

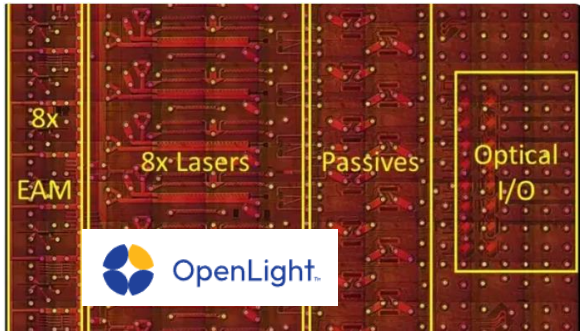
Thin-Film Lithium Niobate



Silicon Nitride
on Silicon Photonics

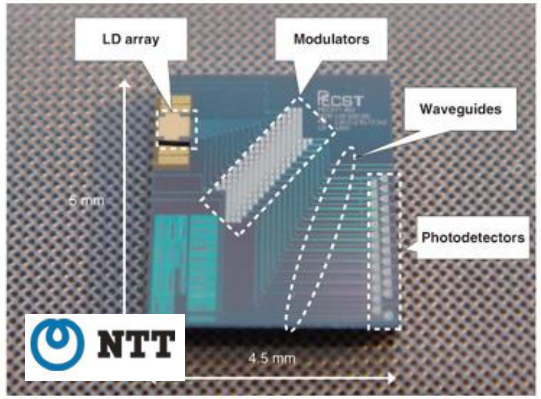
Silicon Photonics in CMOS

Indium Phosphide on Silicon Photonics
Dense heterogenous integration

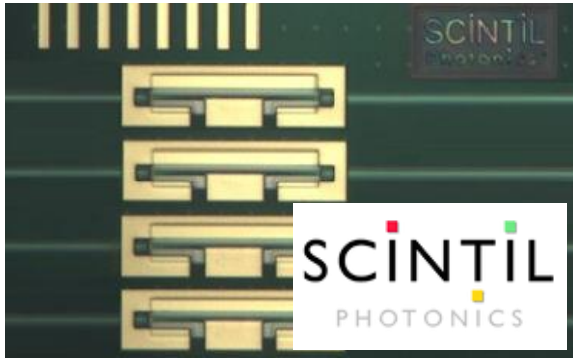


Heterogenous integration

InP on SiPhotonics
Hybrid integration

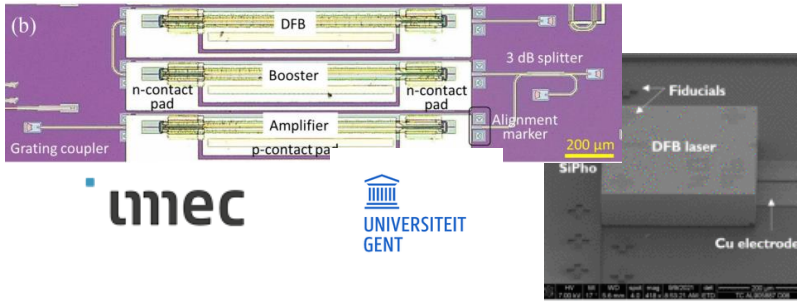


InP or GaAs on SiPhotonics



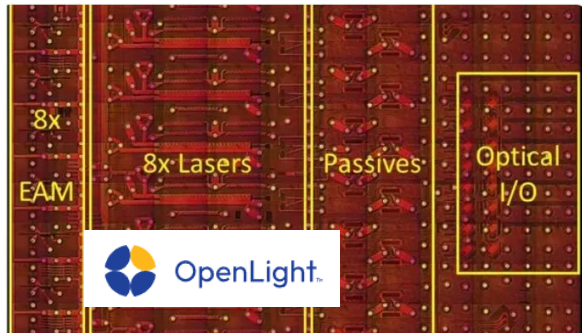
www.scintil-photonics.com

uTP printing and flip-chip integration
of III-V and TFLN on Silicon and Silicon Nitride

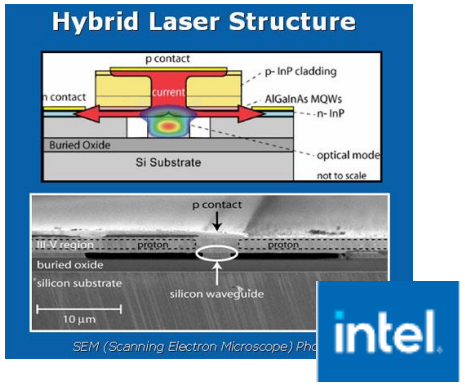


https://doi.org/10.1109/JSTQE.2022.3223641
https://doi.org/10.1109/JSTQE.2022.3222686

Indium Phosphide on Silicon Photonics

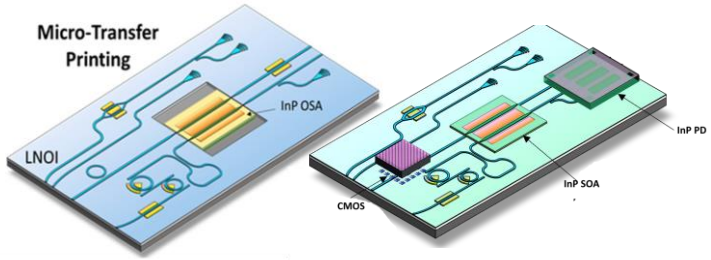


www.openlightphotonics.com



https://www.intel.com/content/www/us/en/architecture-and-technology/silicon-photonics/silicon-photonics-overview.html

InP and CMOS on Lithium Niobate



www.pattern-project.eu

Design challenges

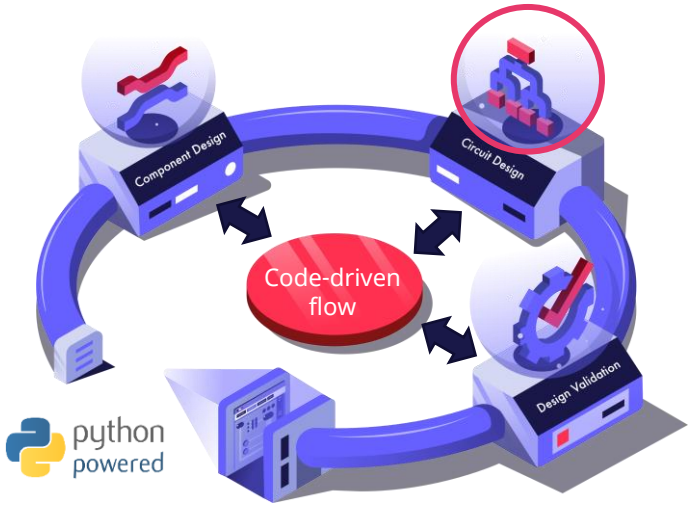
- 100 – 1000s of components
- PDK-based + custom device CAD
- Strong maturity differences between technologies & foundries
- Complex placement and routing: optical – electrical – RF
- Diverse technologies & heterogeneous integration
- Design for assembly / design for test
- Team communication & design IP management

Successful PIC Implementation

- ✓ Team communication
- ✓ Automation (place & route, …)
- ✓ Abstraction of technology details
- ✓ Flexibility to tweak the smallest detail
- ✓ Verification – connectivity / design rule / optical / functional
- ✓ Re-use predefined IP: Pcells, macros, functions
- ✓ IP Management in a team

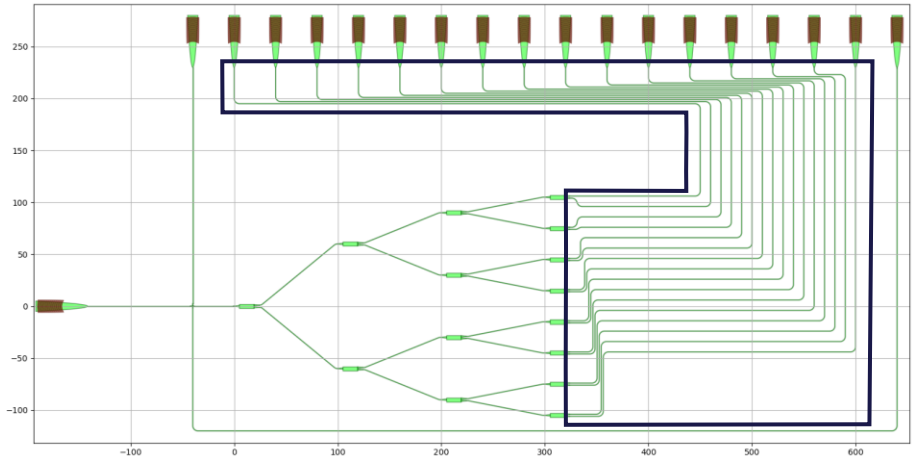
- ✓ Process Design Kits
- ✓ Assembly Design Kits

Circuit Design

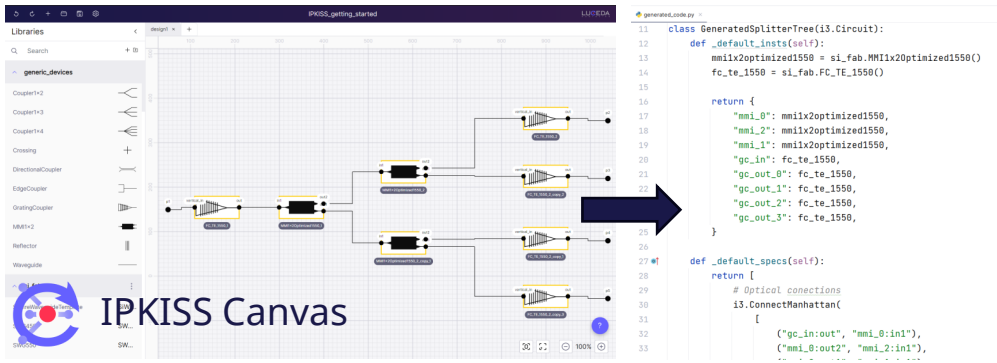


- Code-driven circuit design
- Smart optical and electrical routing
- Parametric circuits in layout & simulation
- Schematic capture with code assistance

Routing



Schematic capture with code assistance



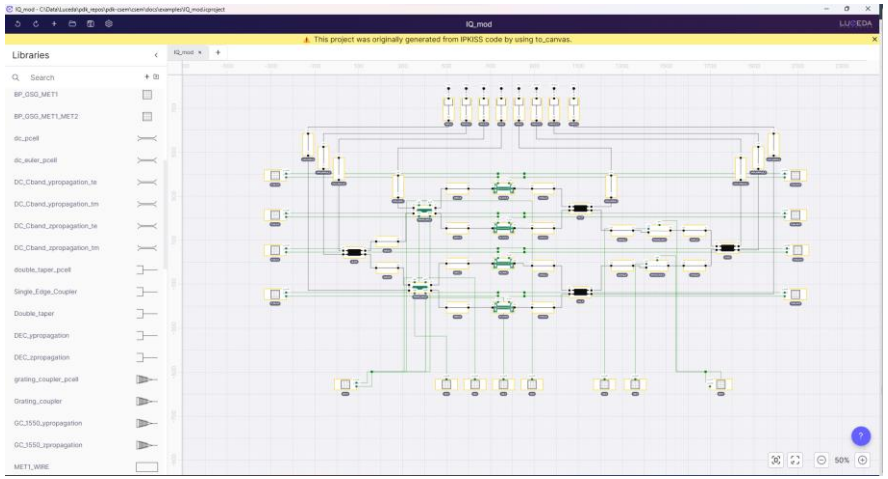
IPKISS Canvas

Canvas: Schematic as communication tool

✓ Very effective communication tool

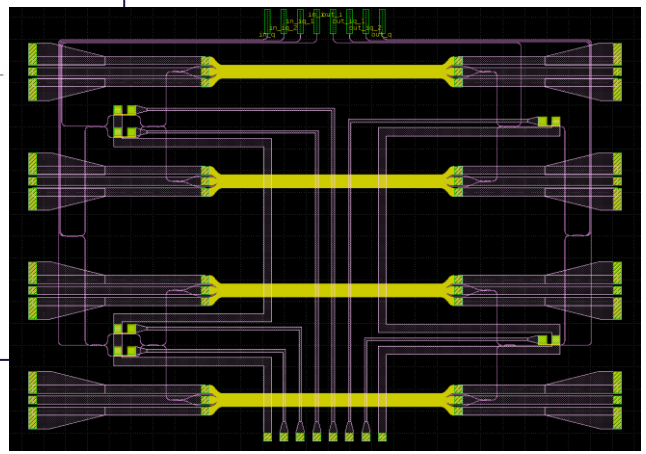
x Pure schematic driven design is difficult (today)

Design team



Implementation team

```
ec_placement_specs = [i3.Place(ec + ":b0", pos, angle=90) for ec, pos in zip(ecs, ec_positions)]
ec_input_routing_specs = [
    i3.ConnectManhattan(
        connections: "thermal_mzm_0:b0",
        "args: "input_q:b0",
        "conn_input_q",
        control_points=[i3.V(-bend_size - 2 * ec_bundle_pitch), i3.H(i3.END -
    ),
    i3.ConnectManhattan(
        connections: "sp_0_0:a0",
        "args: "input_iq_2:b0",
        "conn_input_iq_2",
        control_points=[
            i3.V(-bend_size - 1 * ec_bundle_pitch),
            i3.H(i3.END - bend_size - 1 * ec_bundle_pitch),
        ],
    ),
    i3.ConnectManhattan(
        connections: "sp_0_0:a1",
        "args: "input_iq_1:b0",
        "conn_input_iq_1",
        control_points=[
            i3.V(-bend_size - 0 * ec_bundle_pitch),
            i3.H(i3.END - bend_size - 2 * ec_bundle_pitch),
        ],
    ),
```



photonixFAB

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PATTERN

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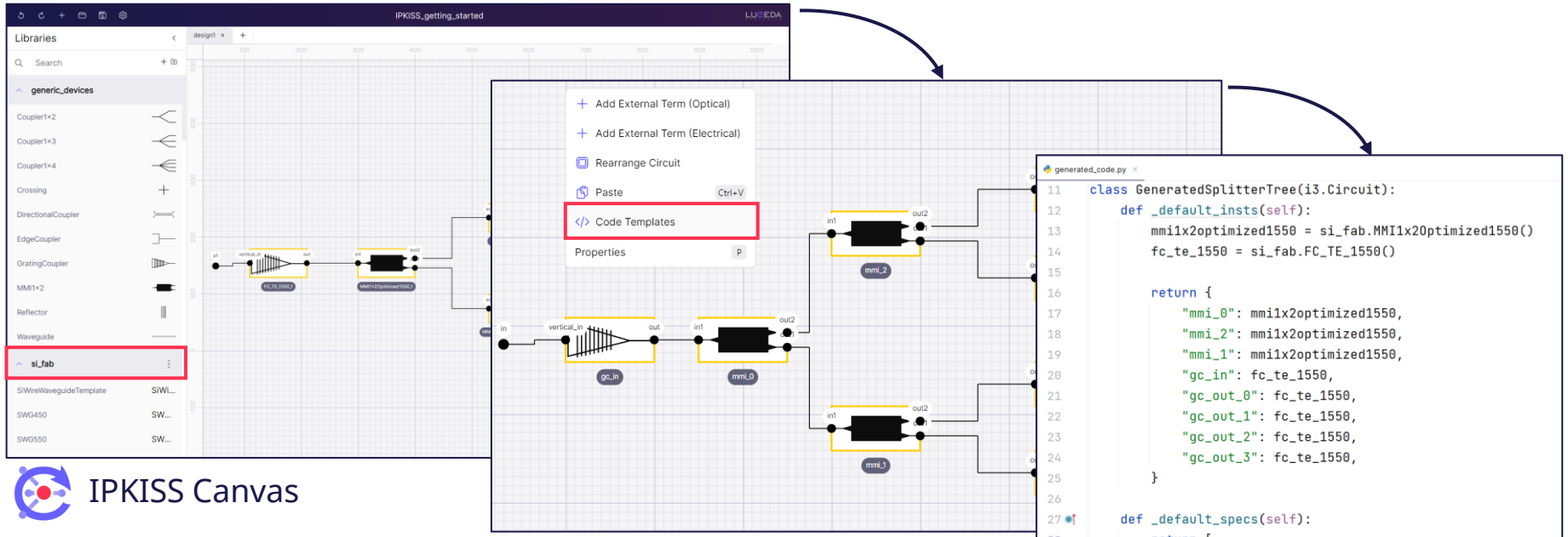
SiPho-G

Advanced GeSi components for next-generation silicon photonics applications

www.sipho-g.eu

Canvas: schematic as communication tool



IPKISS Canvas

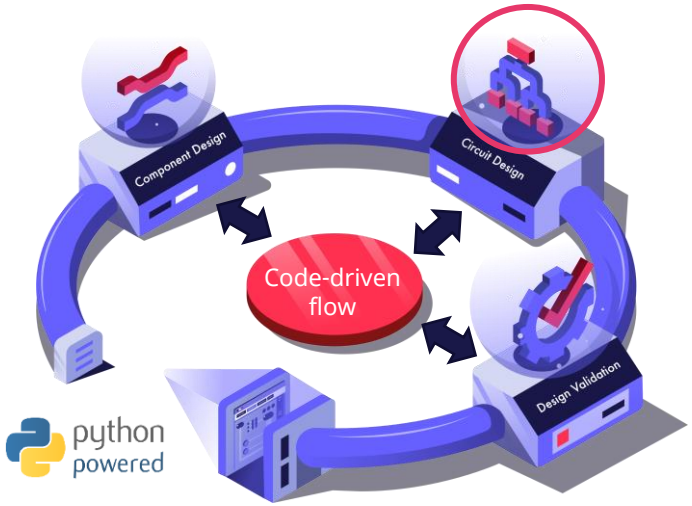
IPKISS Canvas

```python
class GeneratedSplitterTree(i3.Circuit):
    def _default_insts(self):
        mmi1x2optimized1550 = si_fab.MMI1x2Optimized1550()
        fc_te_1550 = si_fab.FC_TE_1550()

        return {
            "mmi_0": mmi1x2optimized1550,
            "mmi_2": mmi1x2optimized1550,
            "mmi_1": mmi1x2optimized1550,
            "gc_in": fc_te_1550,
            "gc_out_0": fc_te_1550,
            "gc_out_1": fc_te_1550,
            "gc_out_2": fc_te_1550,
            "gc_out_3": fc_te_1550,
        }

    def _default_specs(self):
        return [
            # Optical conections
            i3.ConnectManhattan(
                [
                    ("gc_in:out", "mmi_0:in1"),
                    ("mmi_0:out2", "mmi_2:in1"),
```

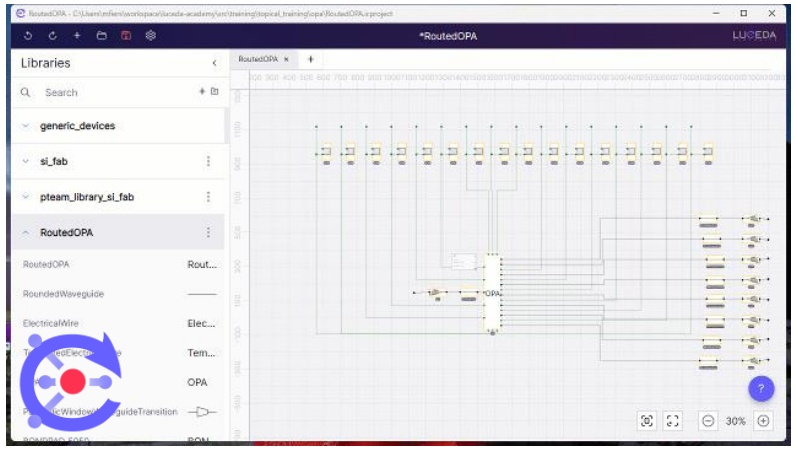
IPKISS Code

- Drag-and drop components from your PDK
- Connect components and give shape to your ideas
- Use ‘Code Templates’ to export the circuit to code
- Adjust the code to finalize the layout
- Inspect the circuit simulations

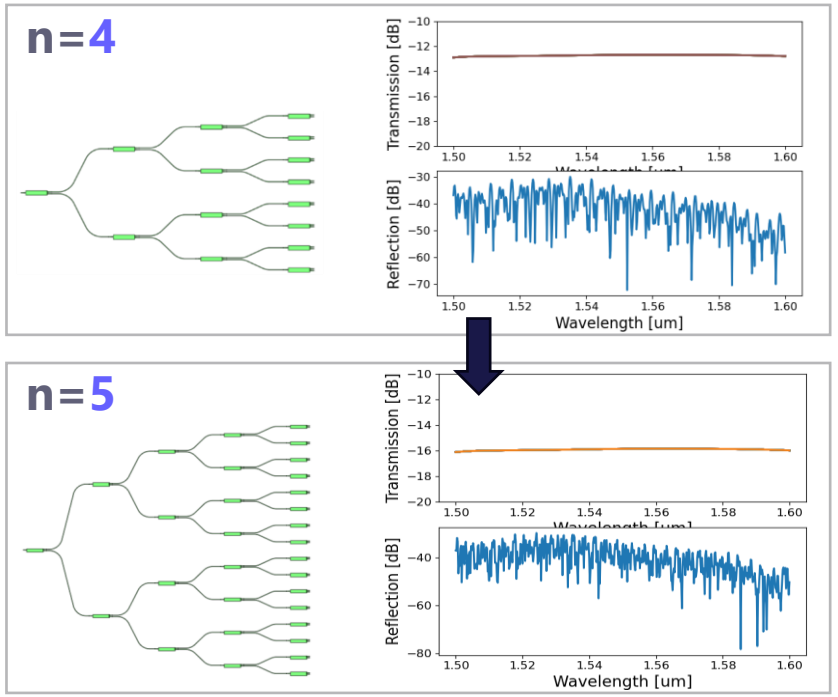
Circuit Design



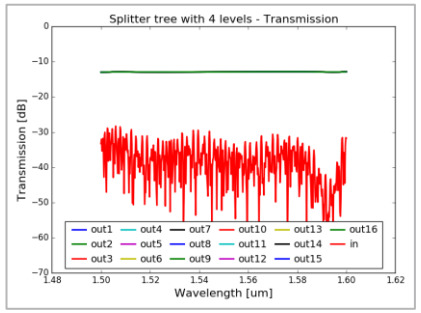
- Tight link layout-simulation
- Circuit simulations with CAPHE simulation engine
- Easy communication around the design process

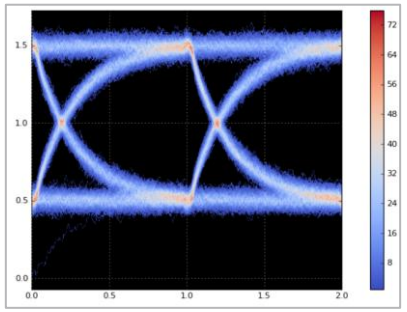


Tight link layout-simulation



Frequency & time domain simulations

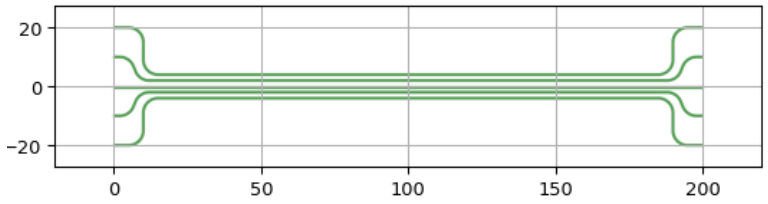
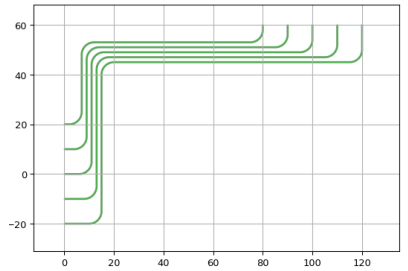
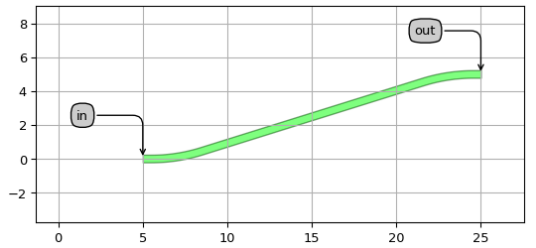


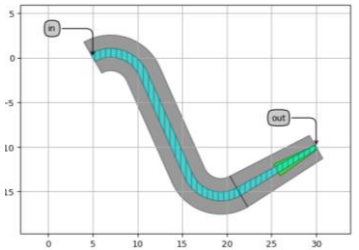


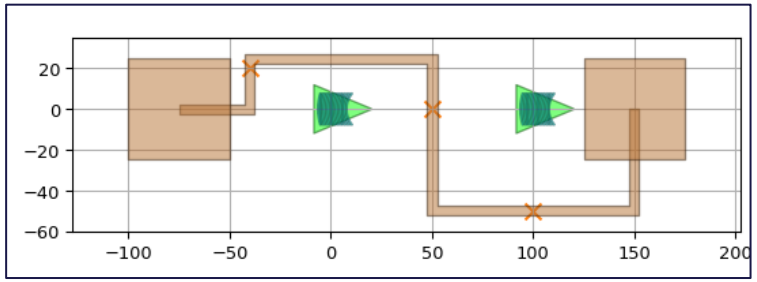
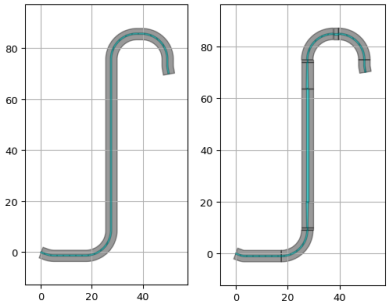
Routing

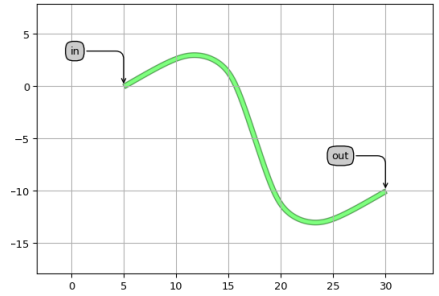
Automation + Control

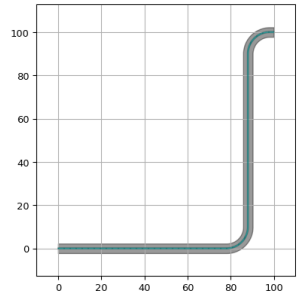
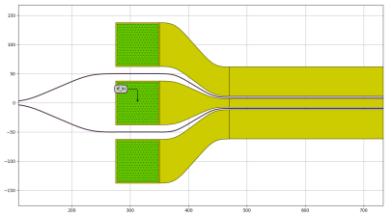
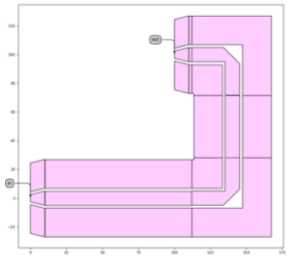
- ✓ Manhattan & non-Manhattan
- ✓ Optical and electrical
- ✓ Automatic angle adjust
- ✓ Automatic tapering
- ✓ Fine-grained control
- ✓ Bundle routing



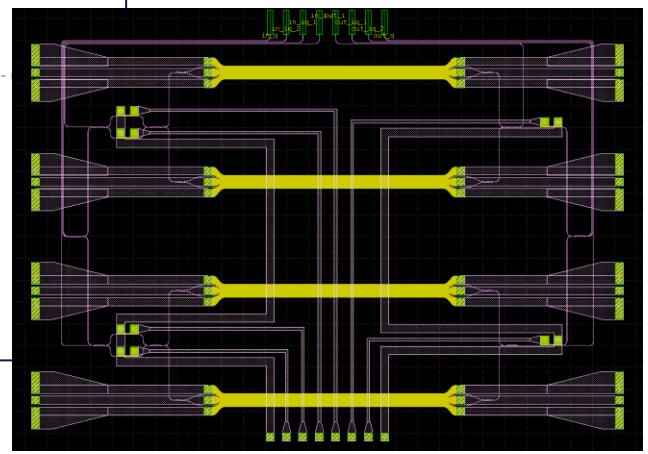


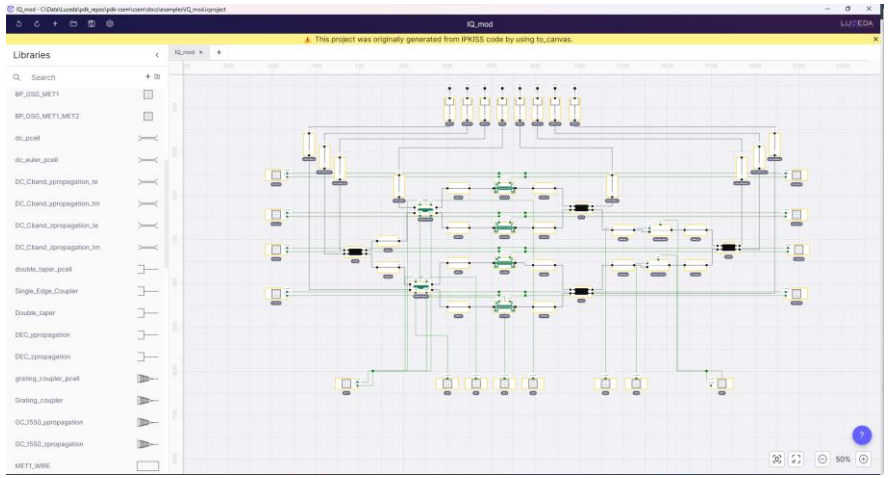




Design validation: schematic as a layout verification tool

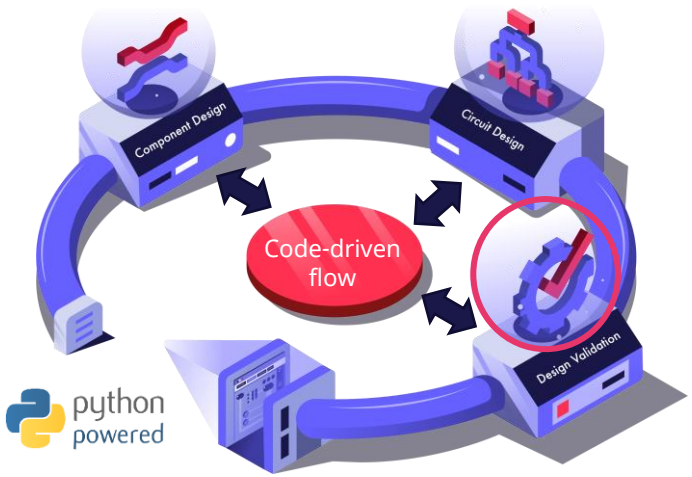
- Visual design check
- Annotation of layout attributes

```
ec_placement_specs = [i3.Place(ec + ":b0", pos, angle=-90) for ec, pos in zip(ecs, ec_positions)]
ec_input_routing_specs = [
    i3.ConnectManhattan(
        connections="thermal_mzm_0:b0",
        "args: "input_q:b0",
        "conn_input_q",
        control_points=[i3.V(-bend_size - 2 * ec_bundle_pitch), i3.H(i3.END -
    ),
    i3.ConnectManhattan(
        connections="sp_0_0:a0",
        "args: "input_iq_2:b0",
        "conn_input_iq_2",
        control_points=[
            i3.V(-bend_size - 1 * ec_bundle_pitch),
            i3.H(i3.END - bend_size - 1 * ec_bundle_pitch),
        ],
    ),
    i3.ConnectManhattan(
        connections="sp_0_0:a1",
        "args: "input_iq_1:b0",
        "conn_input_iq_1",
        control_points=[
            i3.V(-bend_size - 0 * ec_bundle_pitch),
            i3.H(i3.END - bend_size - 2 * ec_bundle_pitch),
        ],
    ),
```

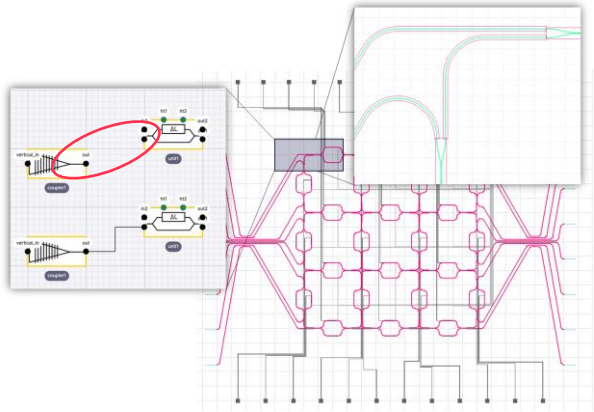




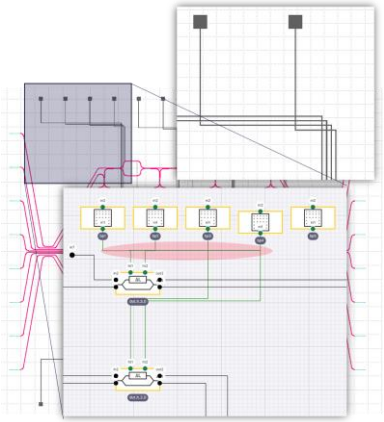
Design validation



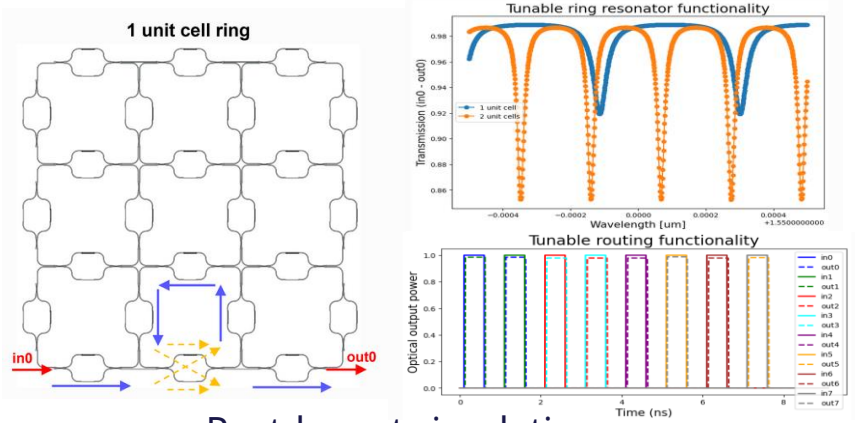
- Connectivity and functional verification with IPKISS Canvas
- Netlist extraction (optical and electrical)
- Post-layout simulations with CAPHE



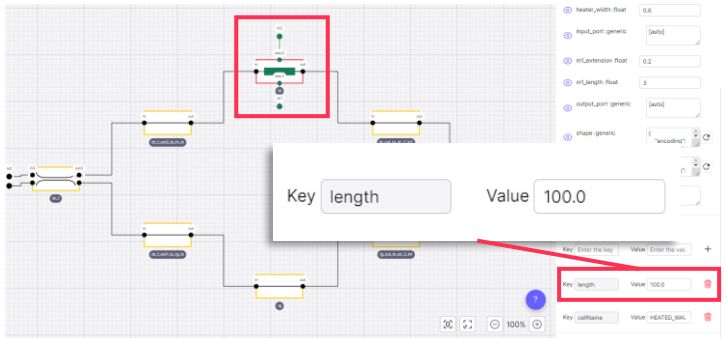
Optical connectivity



Electrical connectivity

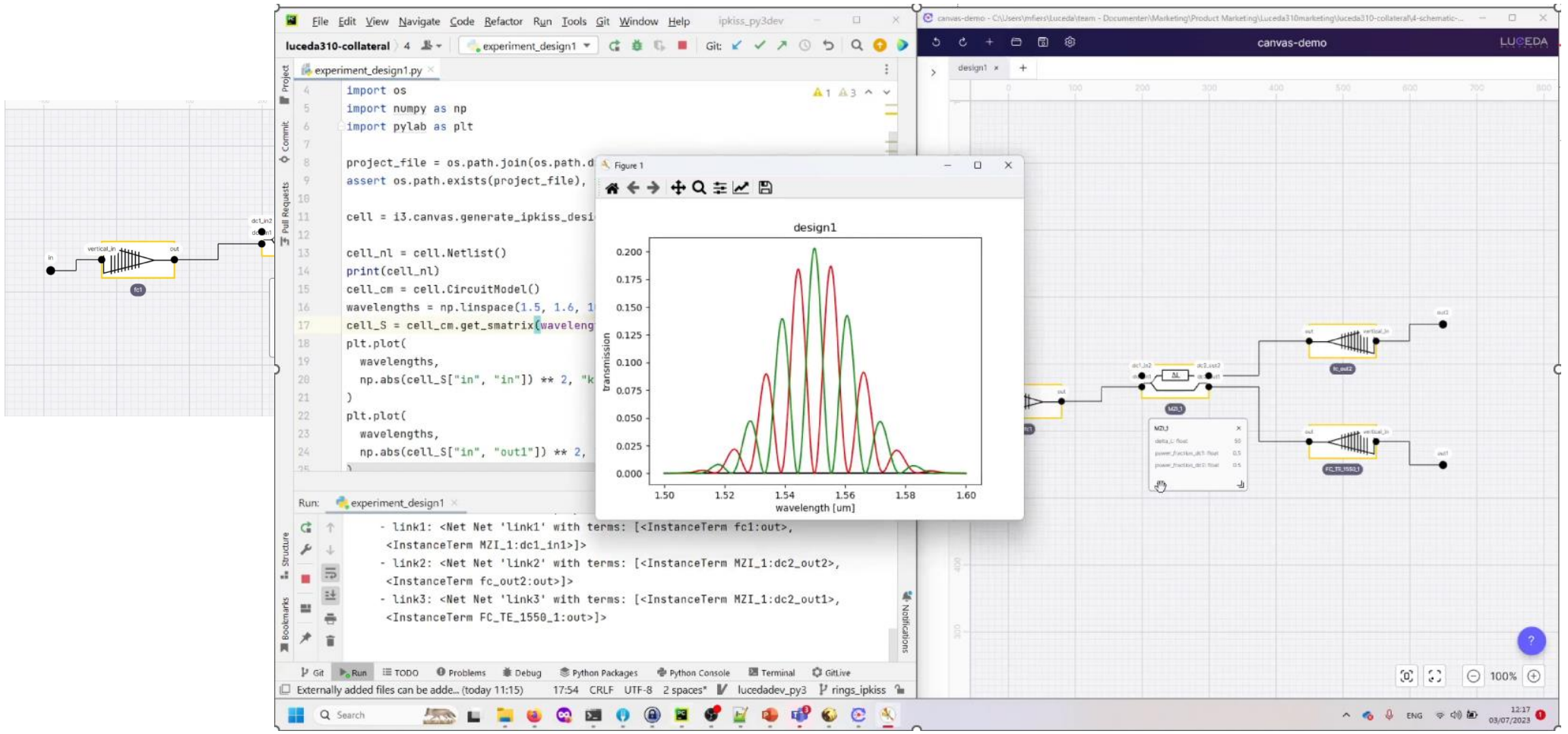


Post-layout simulations

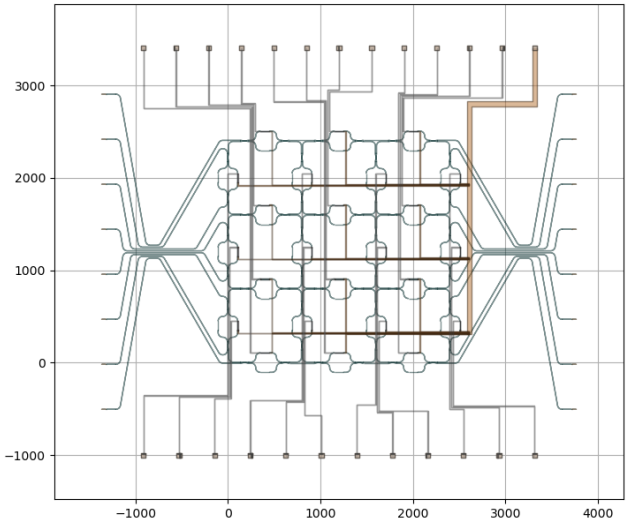


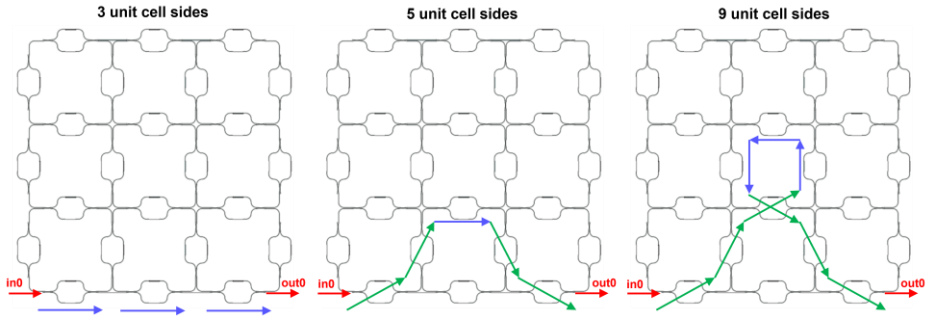
Waveguide length

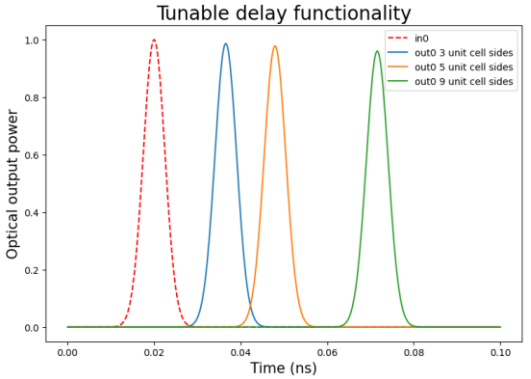
Design validation: linked layout and model

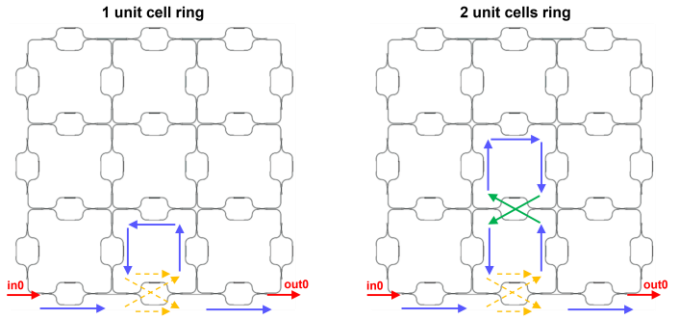


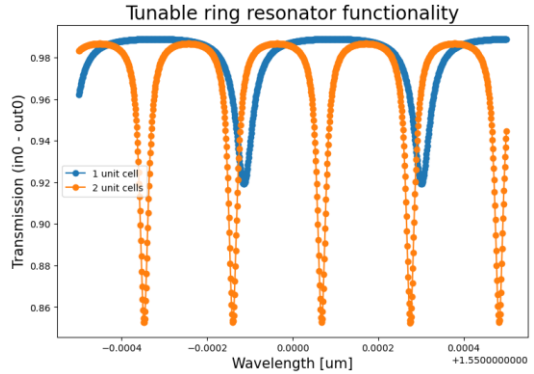
Design validation: linked layout and model







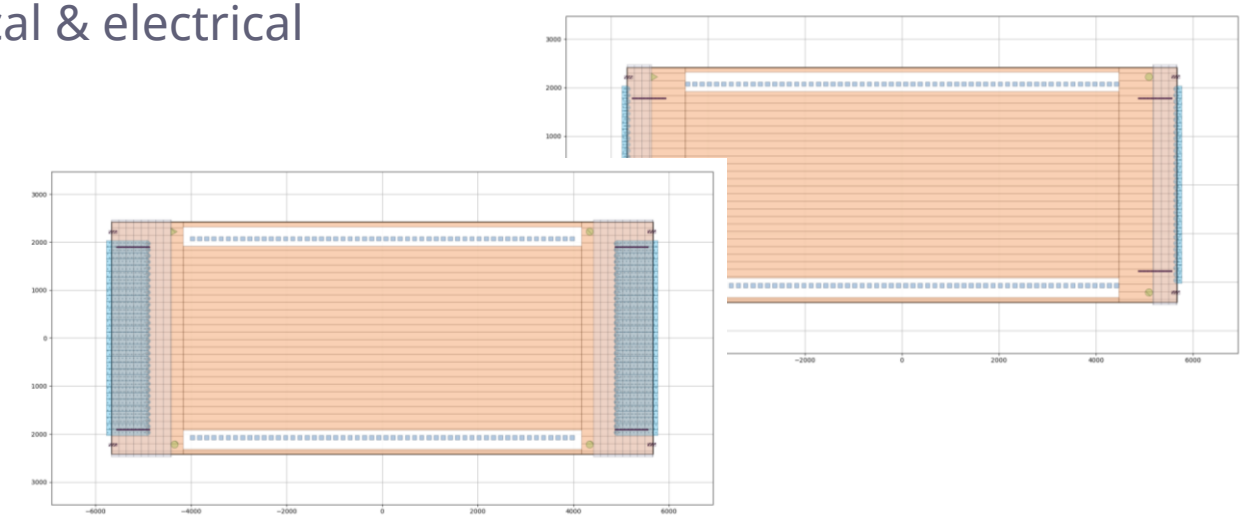




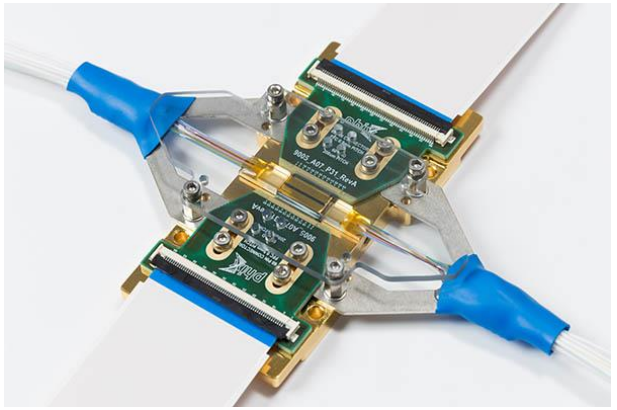
Design-for-Assembly / Design-for-Test

Assembly Design Kit

- ✓ Design rule aware
- ✓ Correct by construction where possible
- ✓ Verify against rules
- ✓ Optical & electrical



PHIX Characterization Package



phix PHOTONICS ASSEMBLY

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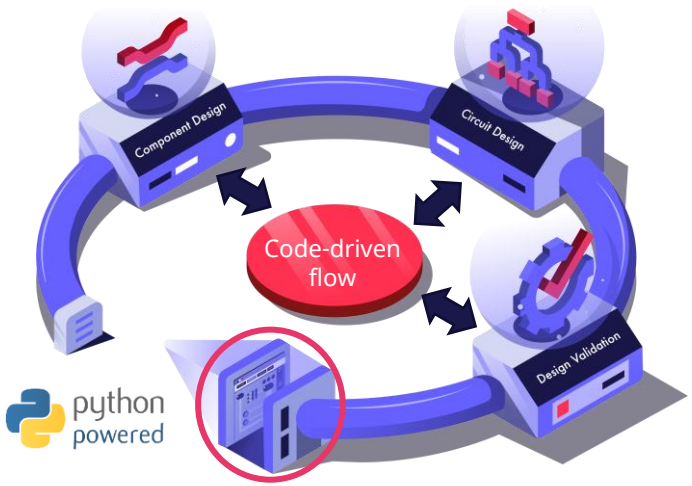
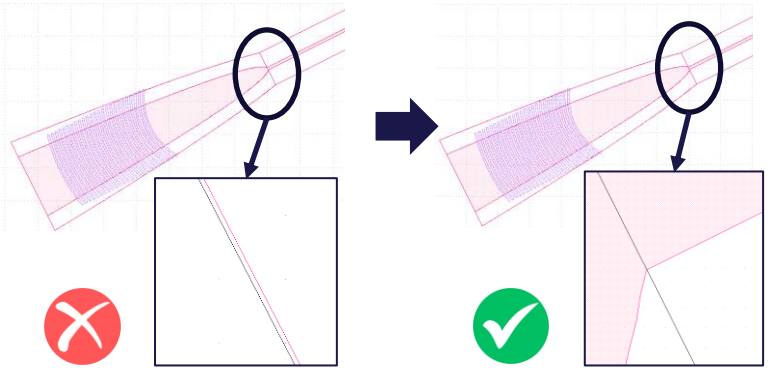
Tape-out preparation

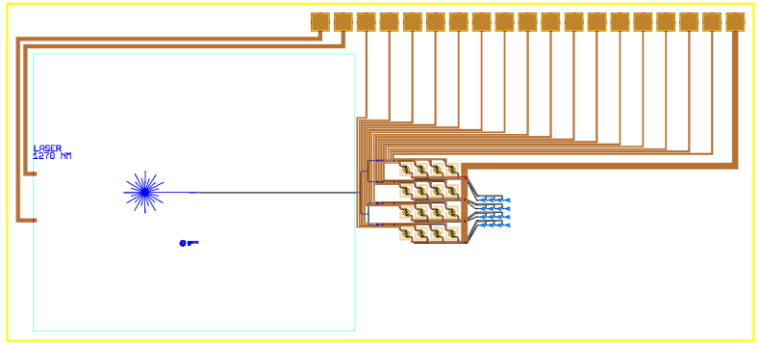


- Tape-out prep: acute angle patching, snapping errors, …
- Tape-out (GDSII)

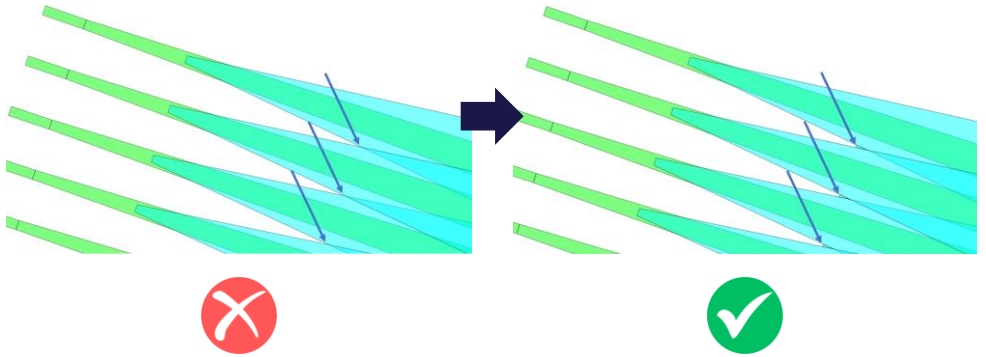
Layout flattening to fix snapping errors



Tape-out



Acute angle patching



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