

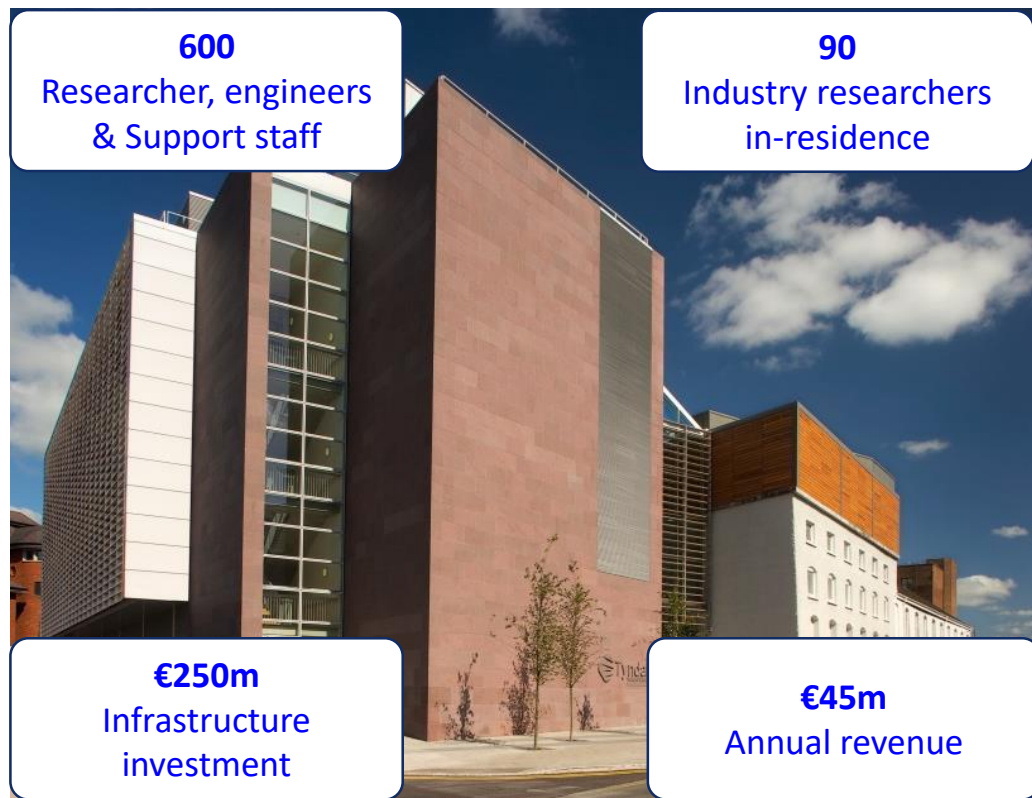
Heterogeneously integrated InP-laser on Silicon Photonics realized by micro-transfer printing

Samir Ghosh, James O'Callaghan & Brian Corbett

Tyndall National Institute
Cork, Ireland

SEMICON Europa' 22

Tyndall in nutshell



Research Focus

- Deep-tech
- Nanotechnology
- Electronics
- Photonics
- Quantum engineering
- Wireless and energy
- Magnetics

Cleanroom



Need for integration

- Foundry-based Si photonics platforms are already matured with efficient modulator (PN-junction), detector (Ge)
- Lasing/ amplification are lacking in Si
- III-V compound semiconductor are efficient gain material

Existing competitive technologies

Hybrid integration

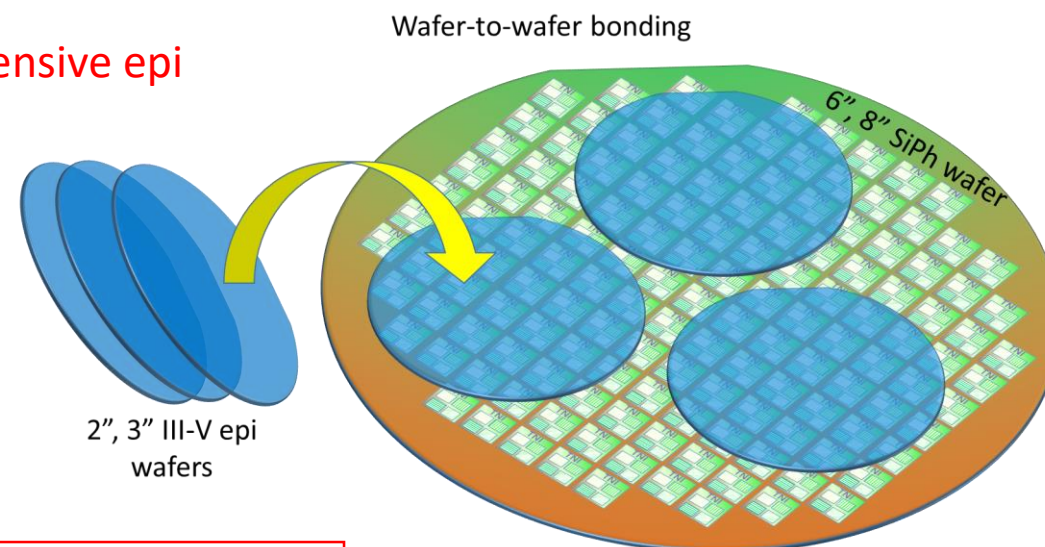
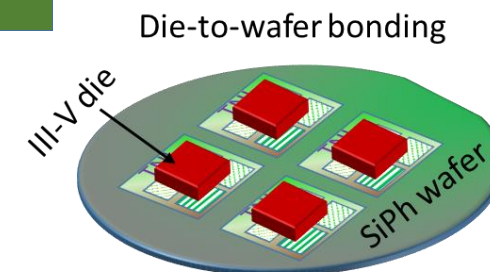
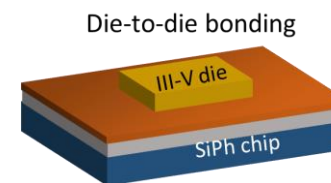
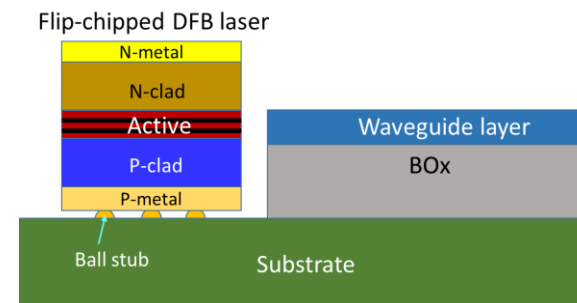
- Co-packaging
- Flip-chip

Heterogeneous integration

- Die-to-die bonding
- Die-to-wafer
- Wafer-to-wafer bonding

- Low throughput
- No known-good die
- CMOS-process disruption
- Yield
- Inefficient usage of expensive epi materials
- Large foot-print
- Expensive

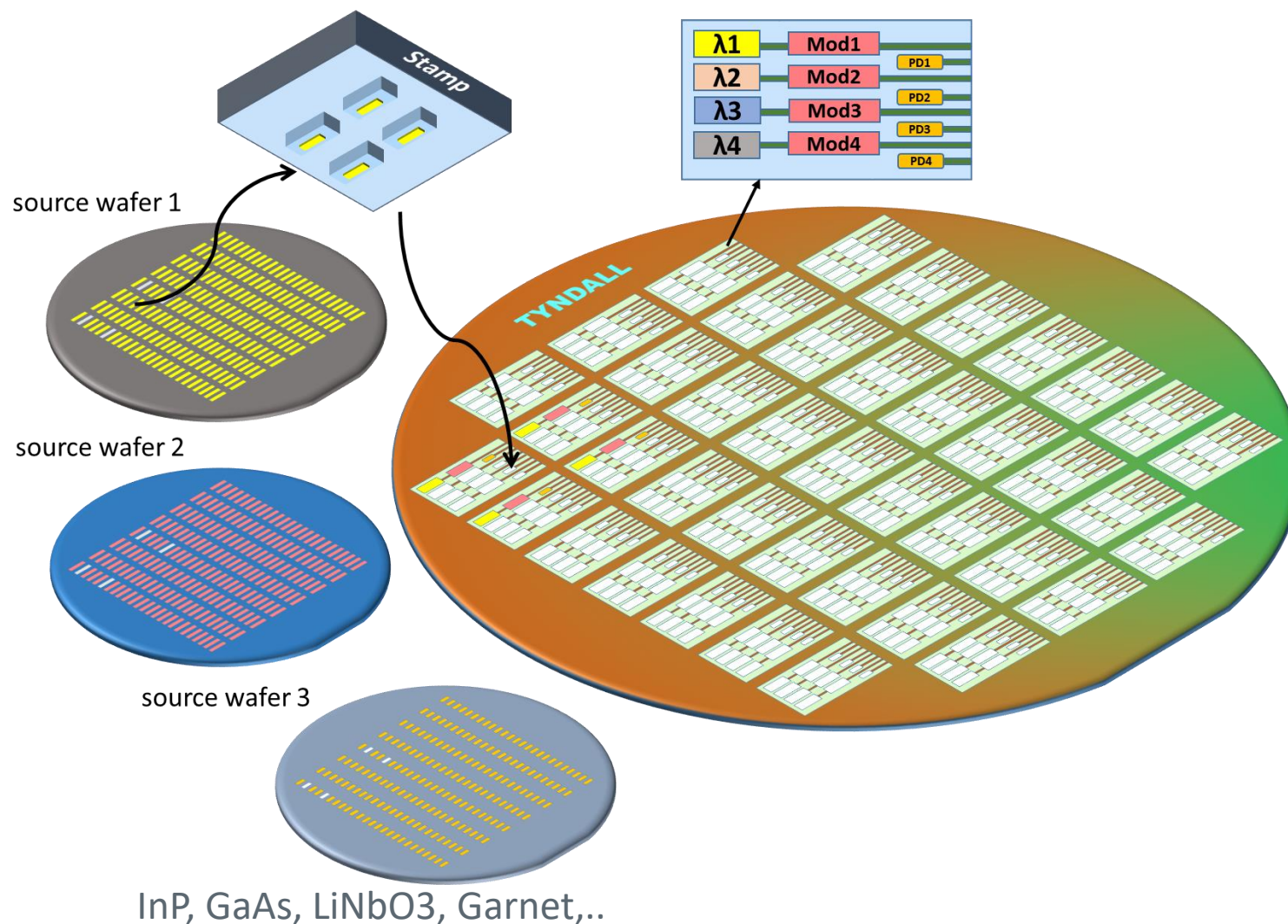
Micro-Transfer printing technology is the technology for heterogeneous integration



Proprietary information

Micro-transfer printing technology-Why ?

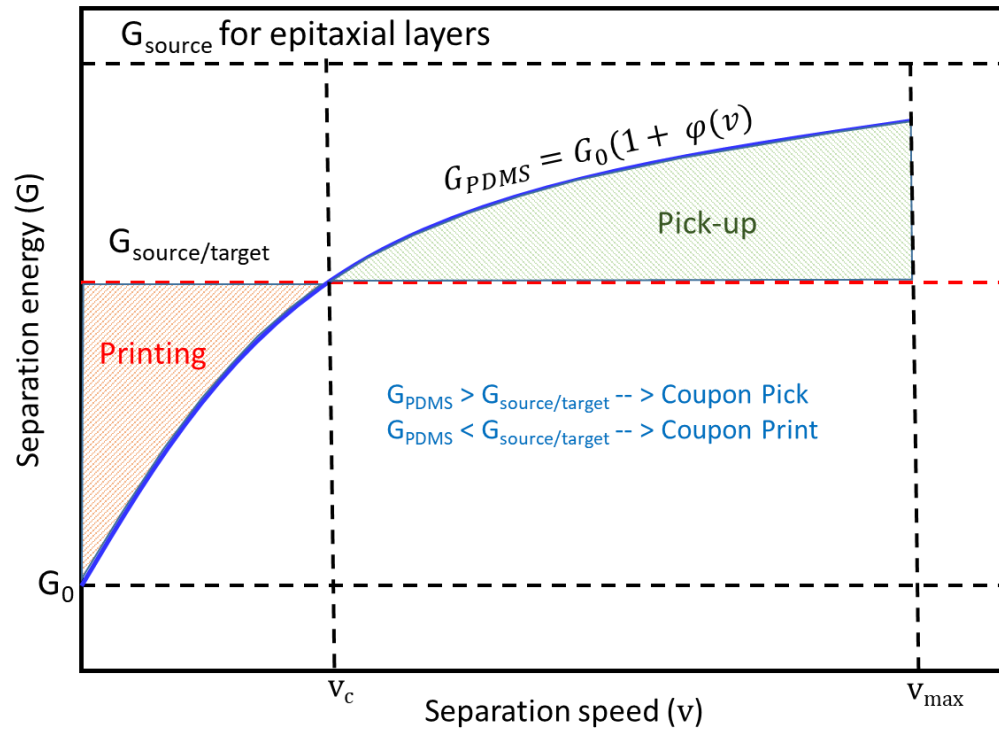
- Massively parallel without hamper front-end and back-end CMOS processing (Not sequential)
- No source to target size incompatibility issue (any size to any size)
- Simultaneous transfer of multiple coupons (varying epi-composition, thickness) on same target wafer
- Pretesting is feasible to identify good coupons
- Efficient usage of expensive epi material
- High yield



Proprietary information

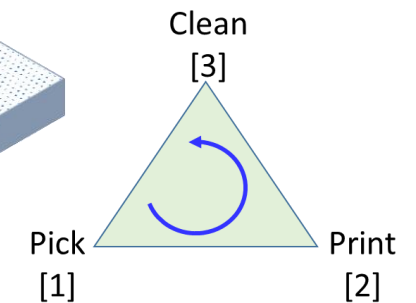
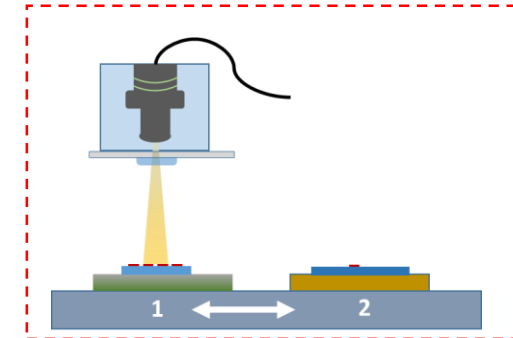
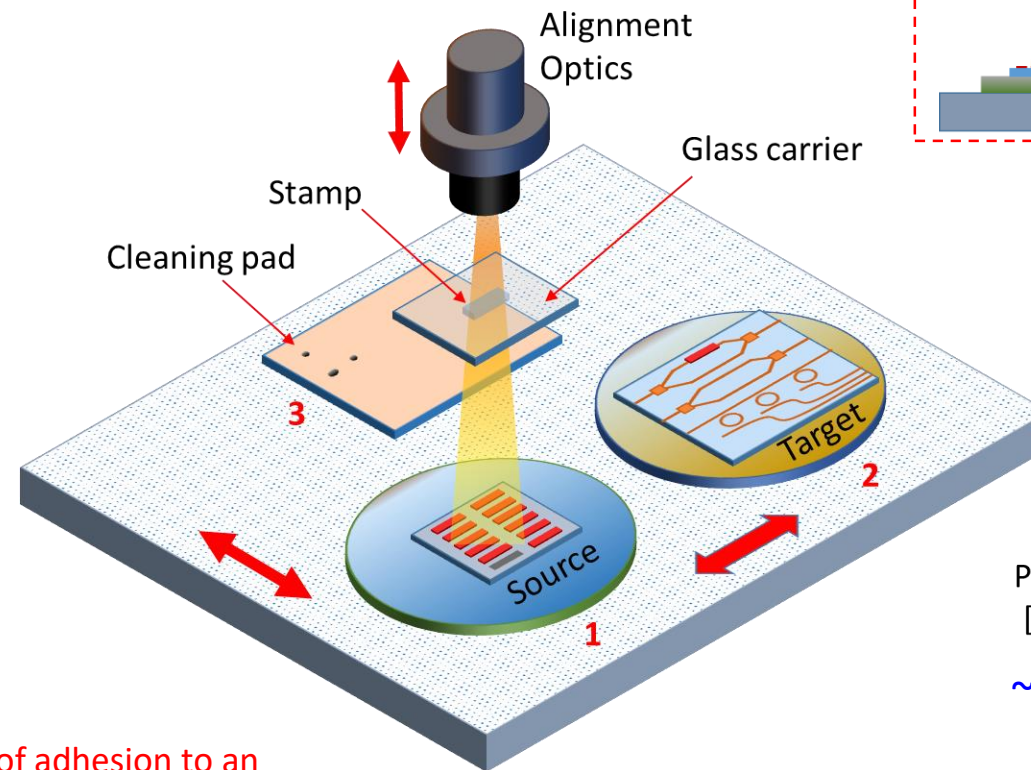
μTP – Operation principle

Physical mechanism: Viscoelasticity
(rate-dependent separation energy) ^[1]



Stamp properties required:

- Soft/deformable (not to damage source)
- Transparent (for optical alignment)



~ 1 min/print cycle

[1] Matthew A. Meitl *et al.*, "Transfer printing by kinetic control of adhesion to an elastomeric stamp," Nat. Material 5 (2006)

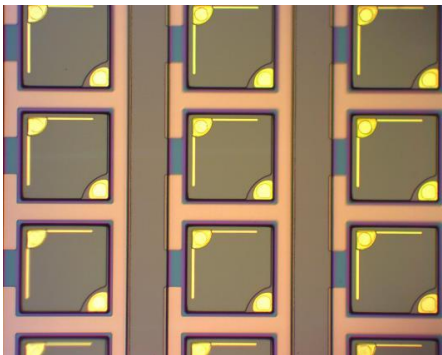
Proprietary information

μTP for display technology-Example

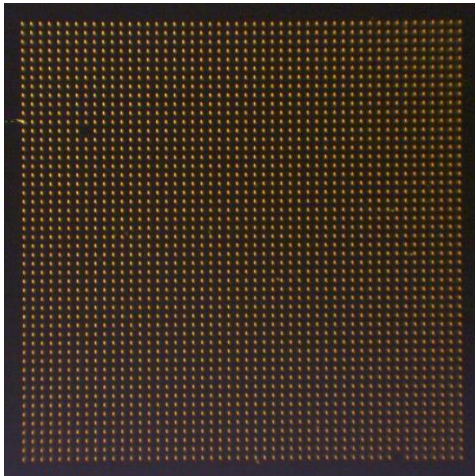
Transfer printing micro-LEDs for RGB microdisplays

Heterogeneous integration – LED transferred with driver electronics

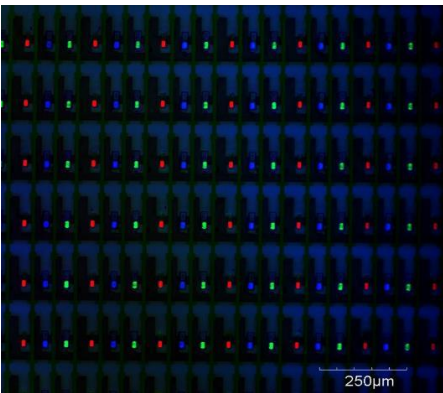
LED wafer



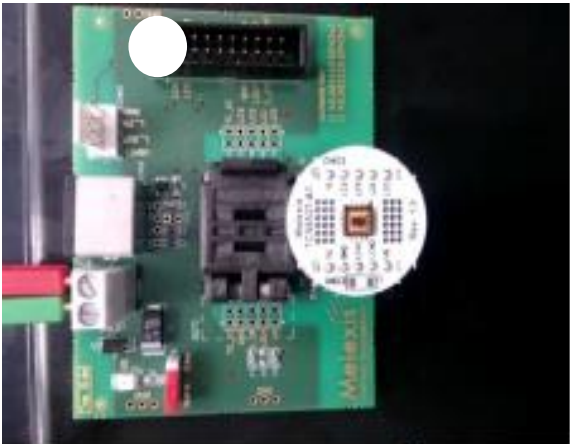
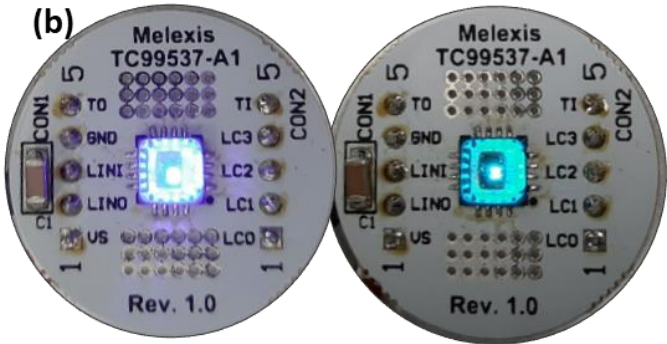
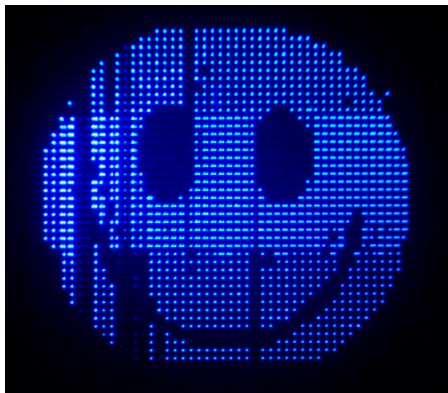
50 x 50 LED



Red, blue, green LEDs transferred
(optically excited)



Electrically driven



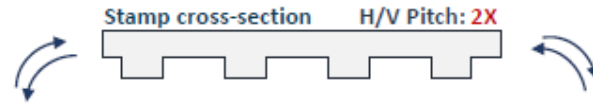
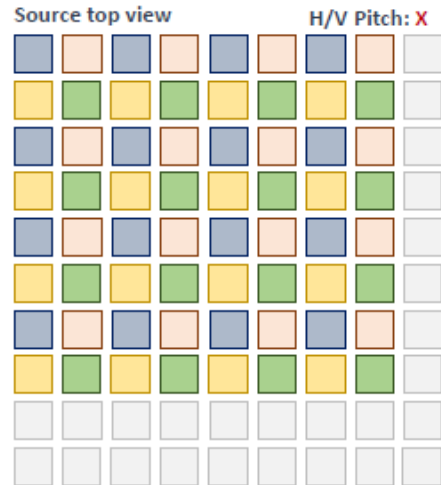
Proprietary information

μTP scaling

Single printing vs. Array printing

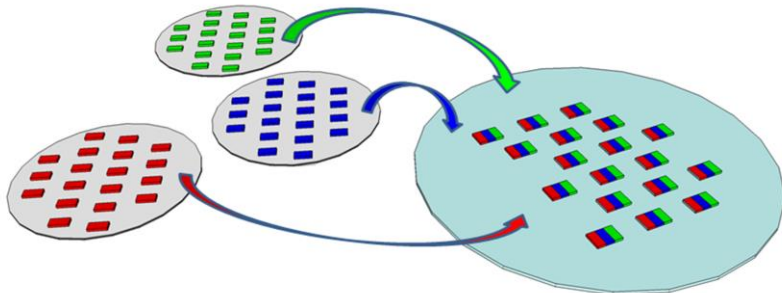
~ 1 min/print cycle

LED source wafer

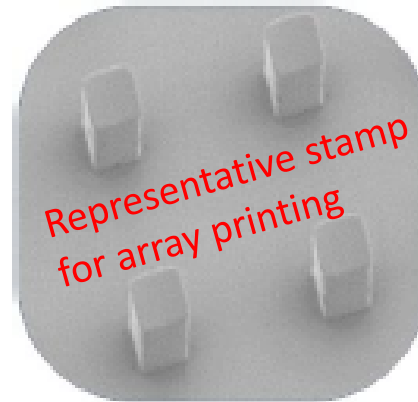


What it involves:

- Target print site pitch = $m \times \text{Source coupon pitch}$ ($m = 1, 2, \dots$ integer)
- Stamp with arrayed post matching source pitch



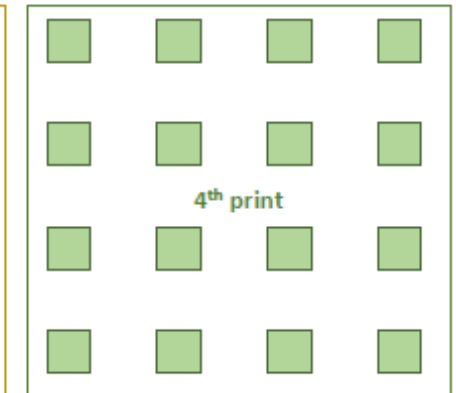
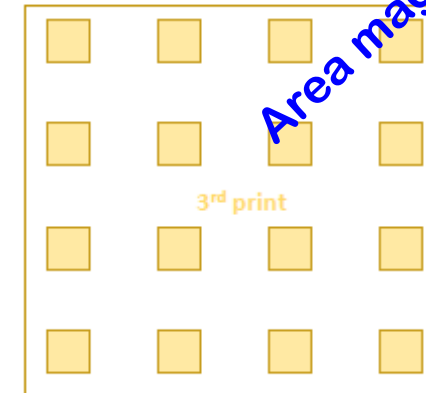
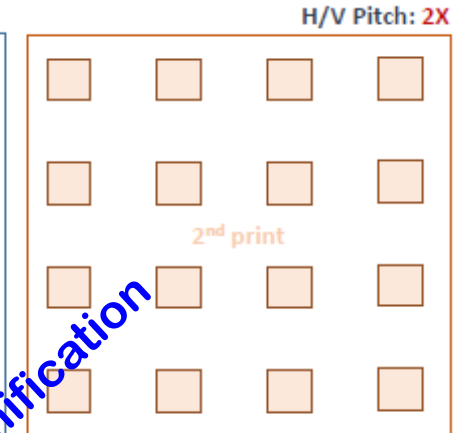
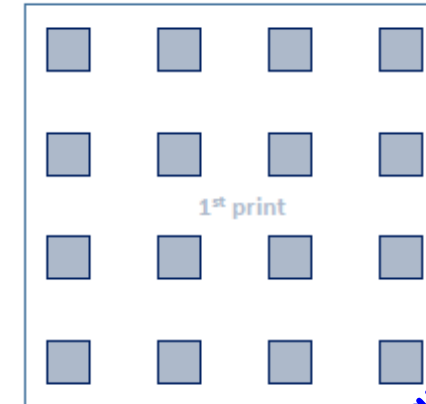
Multi-epi transferring to target



Representative stamp
for array printing

Target wafer

Target top view



Area magnification

- Printing time will be shortened drastically
- Essential for large-area displays

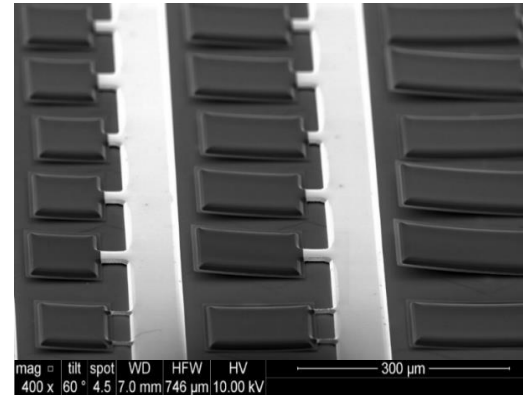
Proprietary information

μ TP for Si Photonics

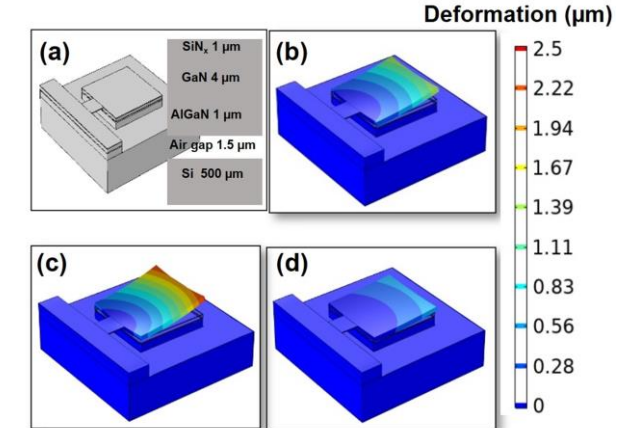
Challenges

- Tighter optical alignment
- Coupon flatness/ stress management
- Coupon backside smoothness
- Coupon size
- Adhesiveness
- Thermal managements
- Wafer-scale process
- Yield

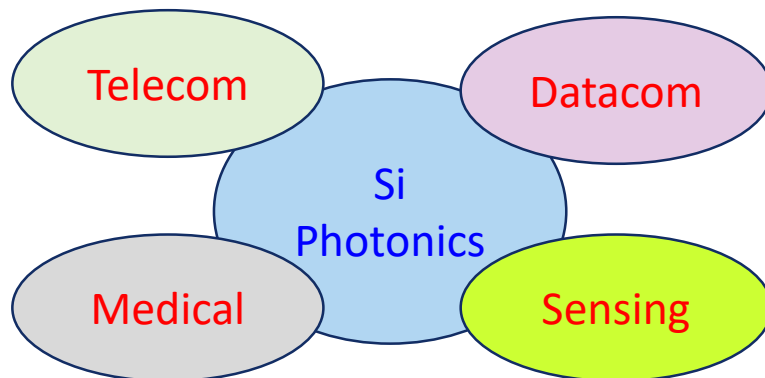
Example of coupon bending



Ex. Simulated stress



Technology readiness level (TRL) ~ 3 – 4 out of 10



Visible, O-band, C-band, Mid-IR

Available Si/SiN thicknesses

- 220 nm SOI
- 400 nm SOI
- 3 µm SOI
- 300 nm SiN-OI

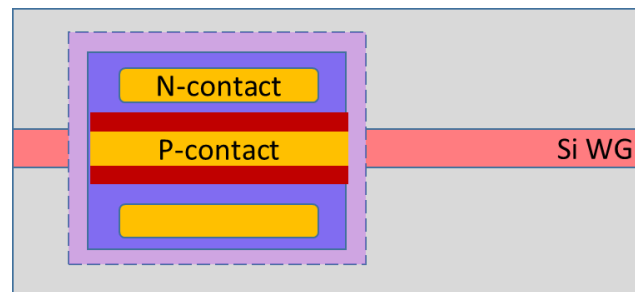
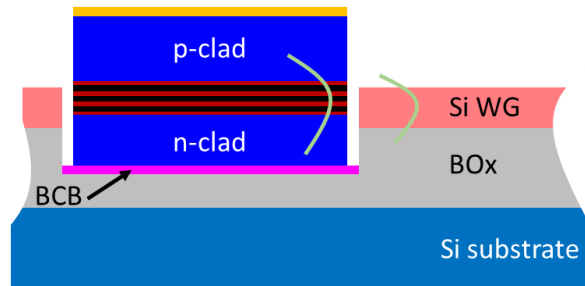
- Optical coupling strategies need to be different
- Printing strategy will be different

Proprietary information

Optical coupling schemes

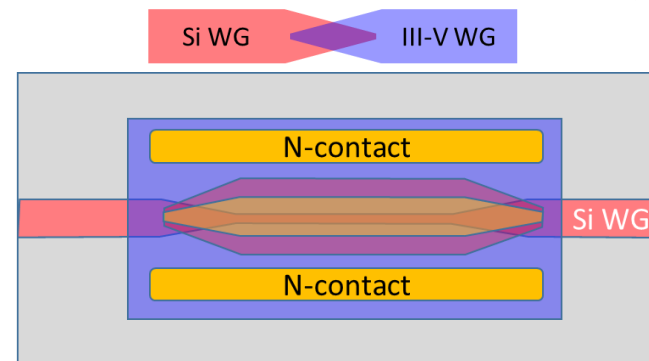
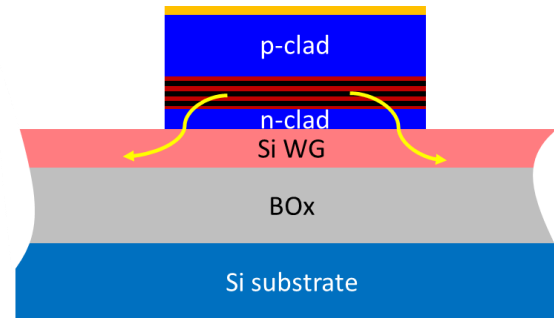
End-fire coupling

- Printing on etched trench/recess
- Precise control on n-cladding thickness, recess depth
- Smooth etch-facet
- Mode size



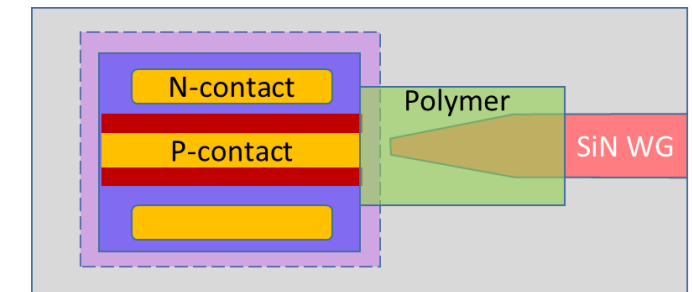
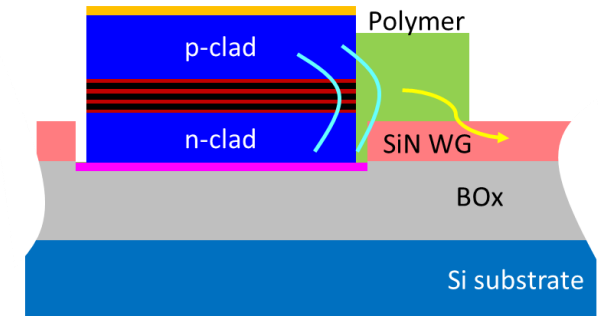
Evanescent coupling (**This work**)

- Low index contrast (InP/Si)
- Thinner n-cladding
- Lateral ridge alignment w.r.t Si wg
- Taper tip

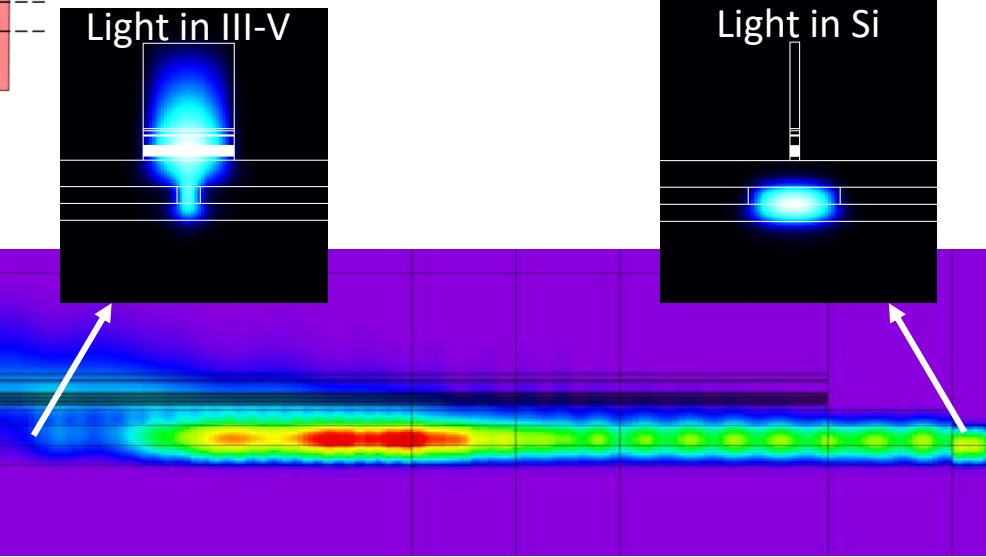
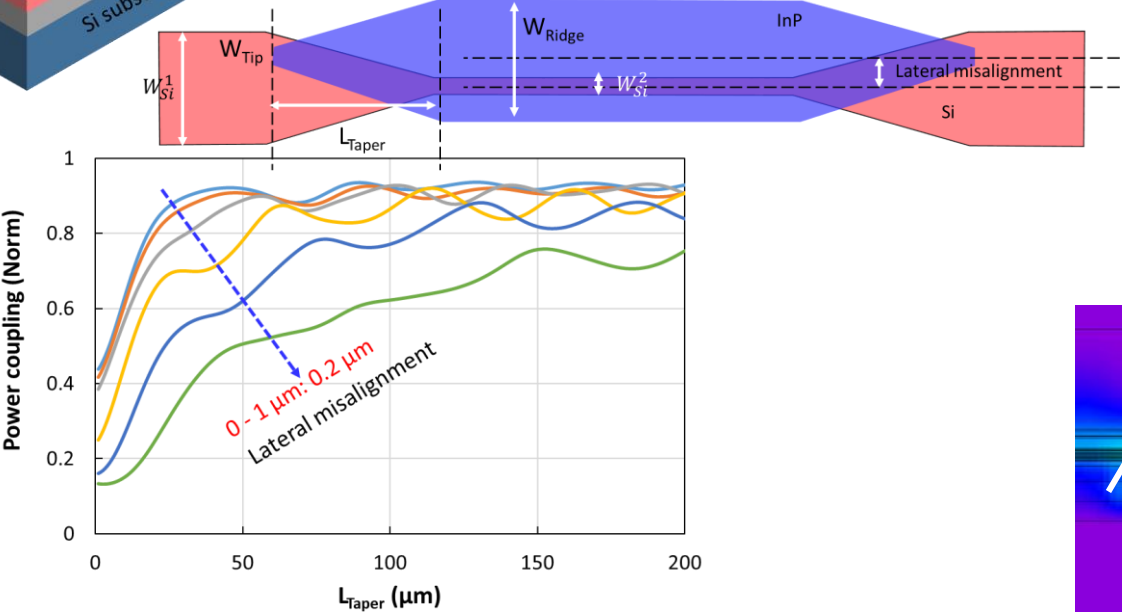
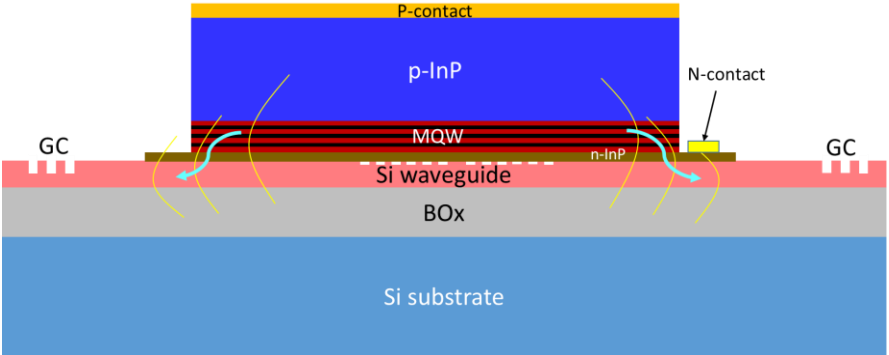
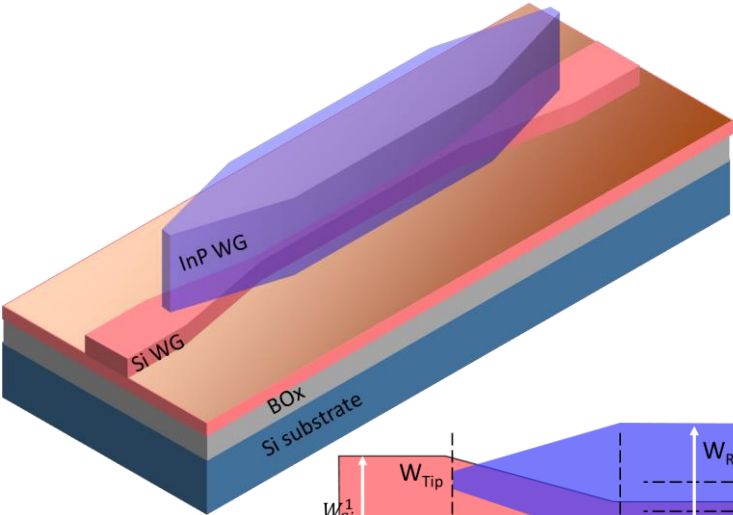


Hybrid-approach

- High-index contrast (InP/SiN)
- Extra processing for polymer



Evanescent Tapering

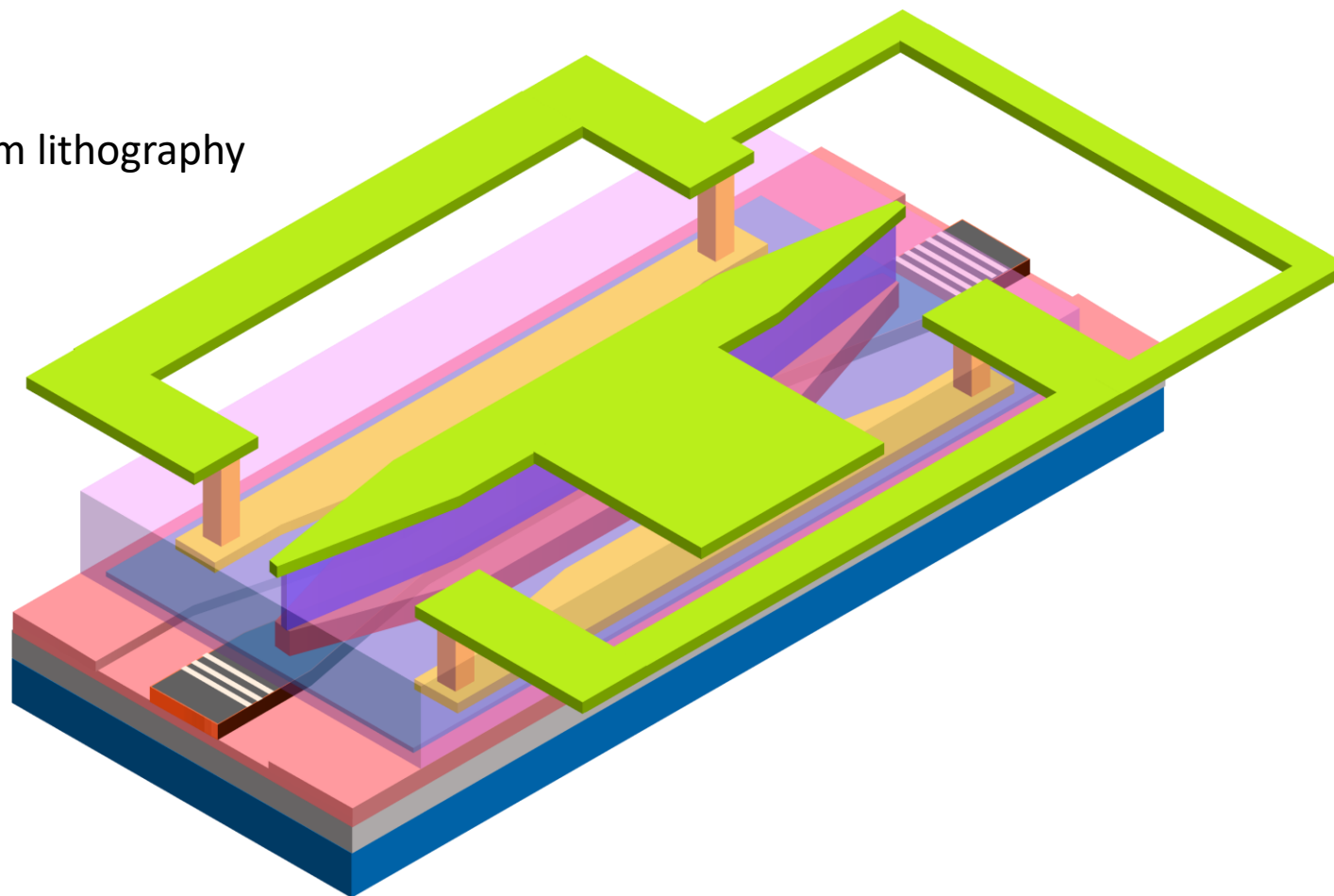


This work addressing lateral misalignment

Proprietary information

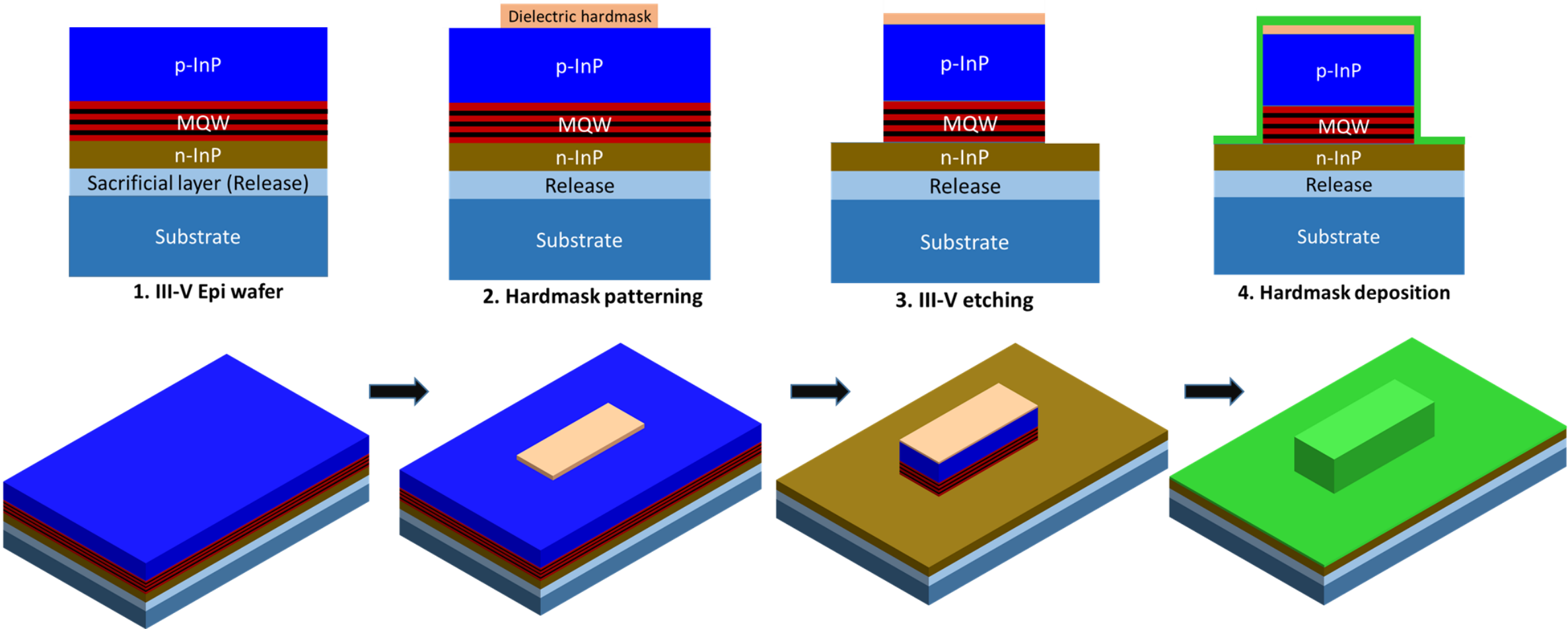
Alignment tolerant μ TP

- III-V source coupon preparation
- Transfer printing III-V on Si target
- Define ridge waveguide by Electron-beam lithography
- Metallization (N, P, routing)



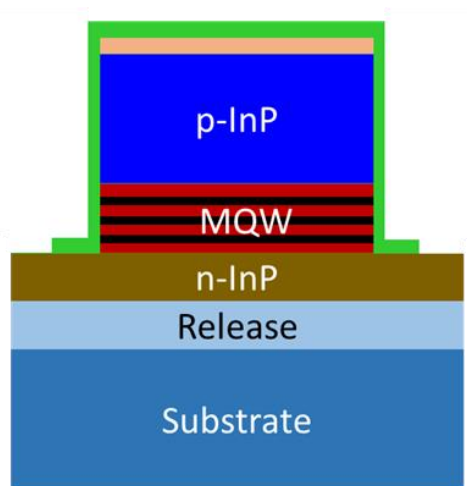
Proprietary information

III-V coupon preparation (1)

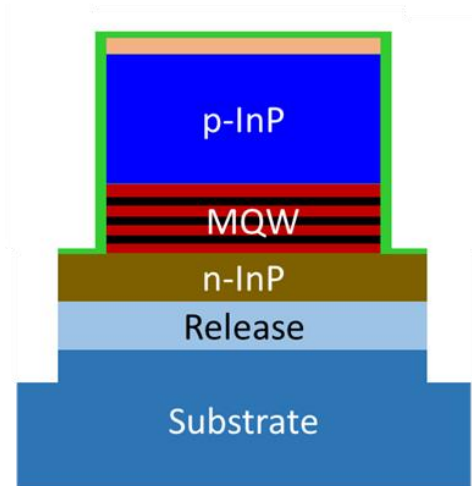


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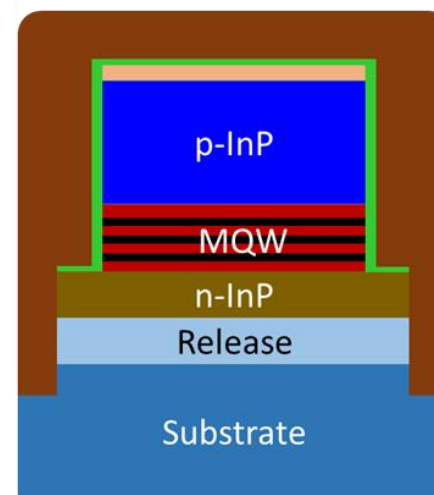
III-V coupon preparation (2)



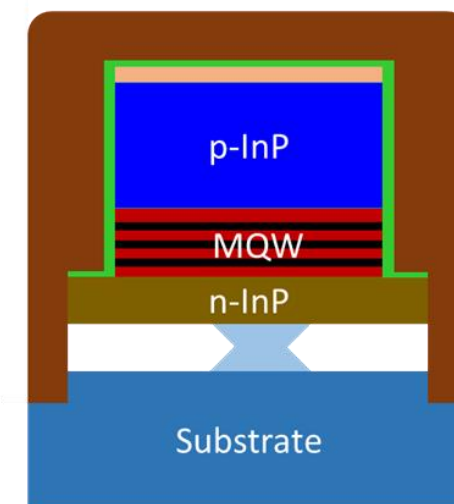
5. Ledge patterning



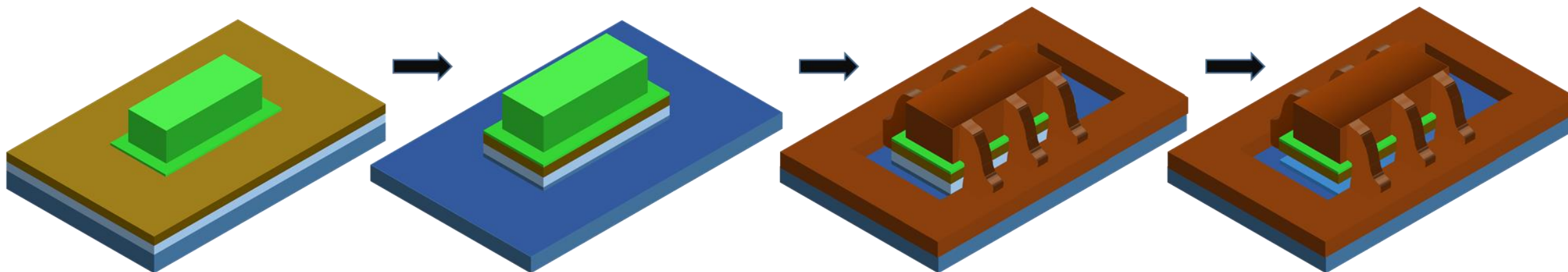
6. III-V etching into substrate



7. Resist tethering



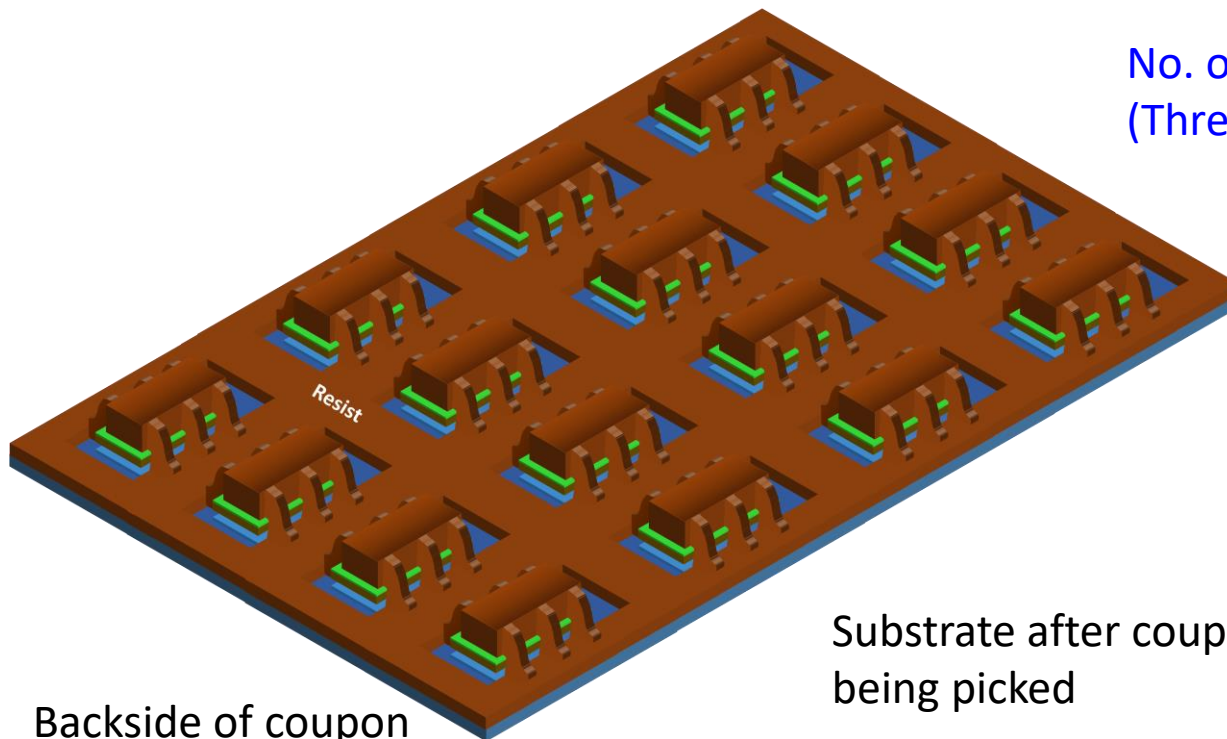
8. Release undercut



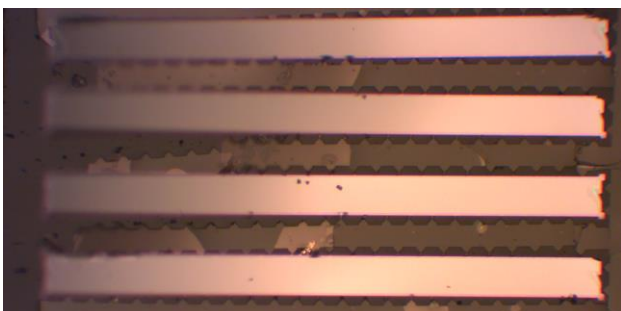
Proprietary information

III-V coupon preparation (3)

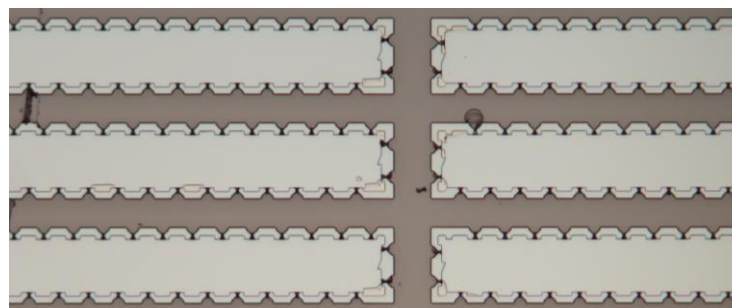
No. of laser coupons from a 2" InP source wafer ~ 8500
(Three different lengths: 1 mm, 1.25 mm, 1.5 mm)



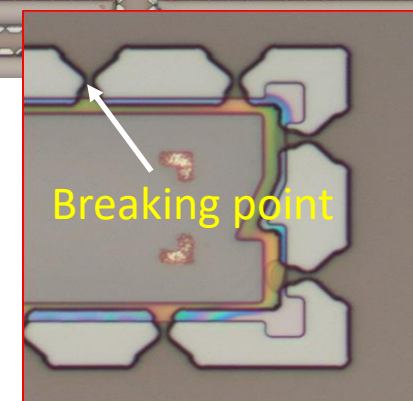
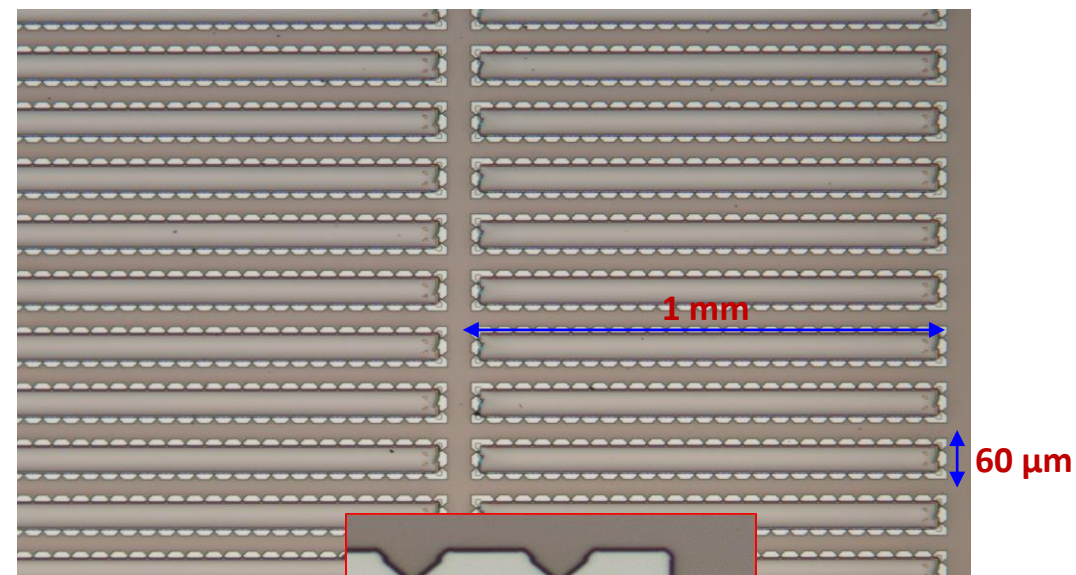
Backside of coupon



Substrate after coupon being picked



100 % suspended coupon with smooth backside

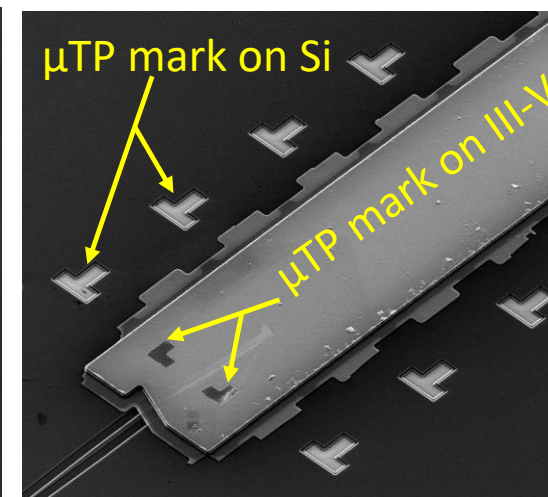
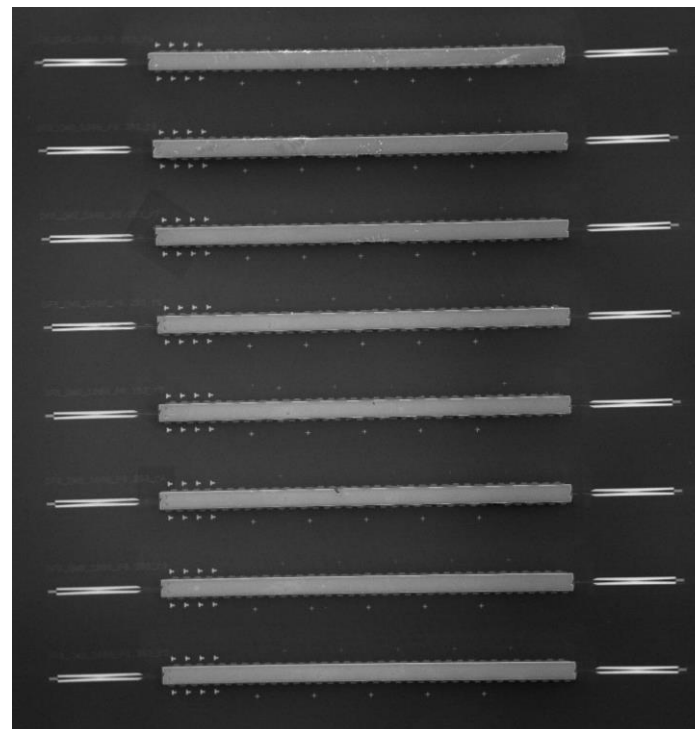
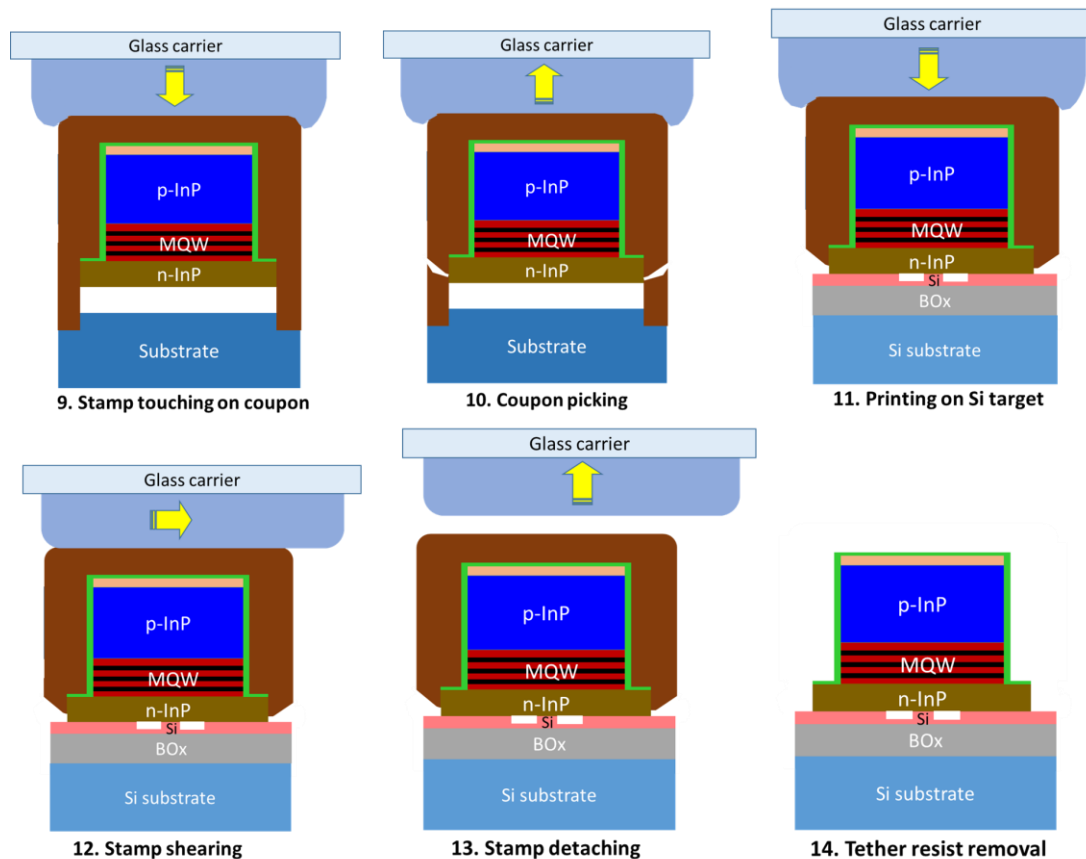


Proprietary information

Transfer printing

Target preparation

- Acetone + IPA clean + DI water
- Transfer printing



- Print yield ~ 100 % (coupon print/coupon picked) achieved
- Recipe developed for optimum tether resist removal

Proprietary information

Key process steps

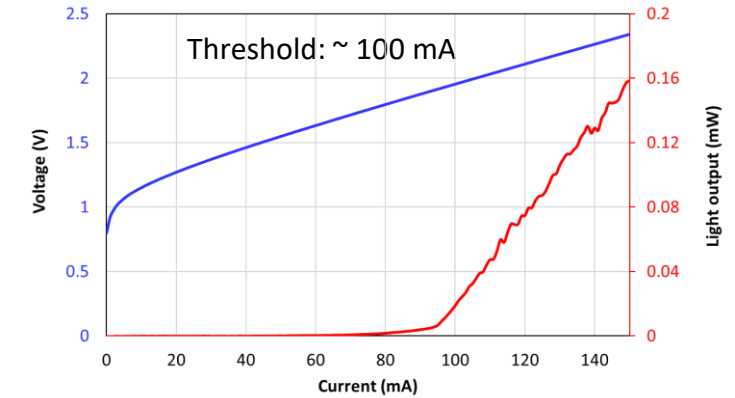
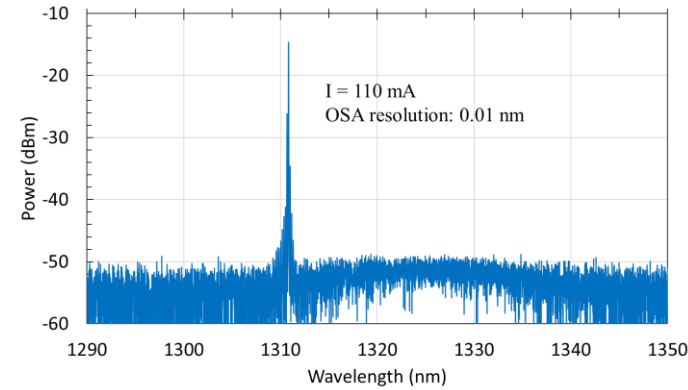
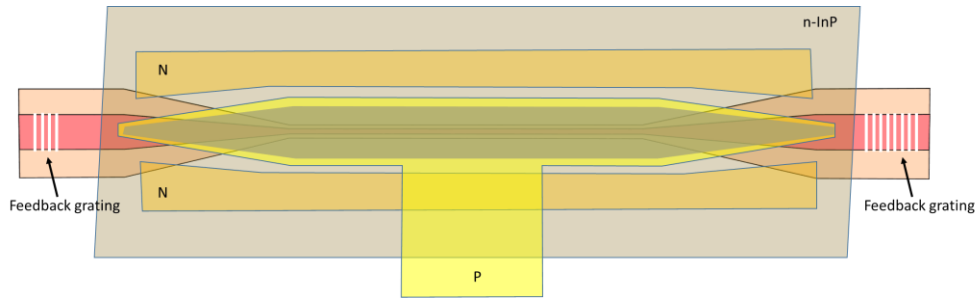
- Hardmask deposition on printed target
- Electron beam lithography to define ridge
- Selective hardmask opening
- Mesa etching
- N-metal
- Planarization by BCB and etch-back
- P-metal
- Via opening
- Final connection metallization
- Selective removal of BCB, hardmasks

Key developments

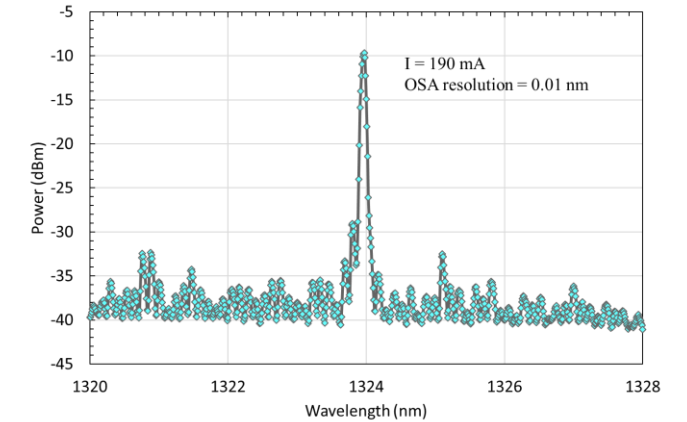
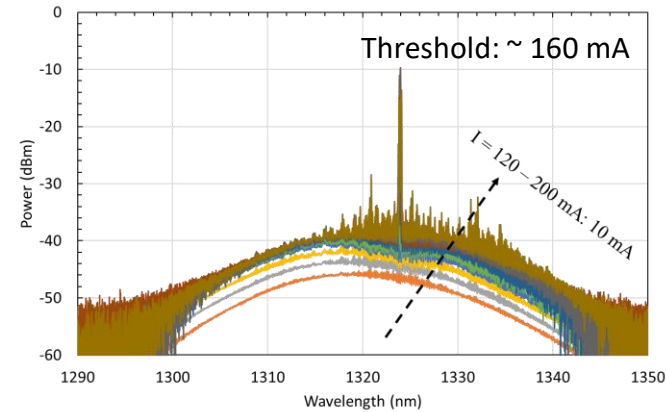
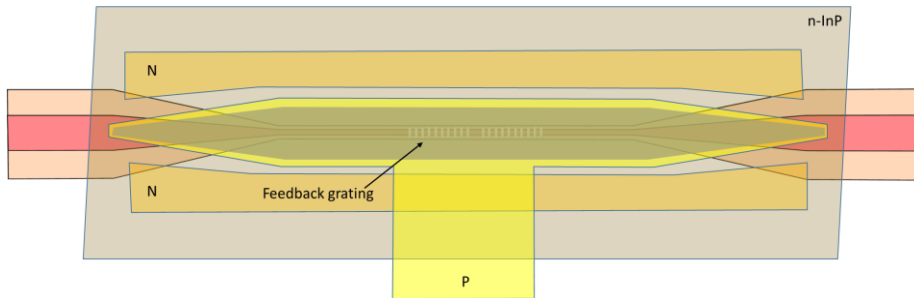
- Defining InP ridge waveguide on SOI target with sub-500 nm accuracy
- Protecting Si waveguide during all the etches
- Opening selective areas at the end applying dry and wet etching

Lasing characteristics

DBR-laser



DFB-laser (Quarter-wave shifted)



- Lasing observed → Tapering works, all metallization are fine
- Higher threshold is due to weak feedback which can be solved by design optimization

- Lasing proved that our approach worked
- Established a robust III-V coupon preparation method
- A reliable recipe has been realized for transfer printing
- Printed coupon survived multiple lithography and etching steps
- Sub-500 nm alignment accuracy has been achieved between InP gain block and SOI target waveguide
- Overall yield ~ 95% (Coupon survived at last/Coupon transferred)
- Future goals are better alignment, lower threshold, higher power
- Scaling our approach for wafer-level
- We are at ~ 3 – 4/10 in technology readiness level (TRL); Next step is to industry take over for further development in real manufacturing environment