ASMC ADVANCED SEMICONDUCTOR MANUFACTURING CONFERENCE

AUGUST 24–26, 2020 VIRTUAL EVENT

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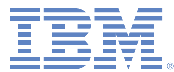

EVENT GUIDE

MONDAY, AUGUST 24 *Available On-Demand starting at 8:30am EDT.*

Welcome to the Conference
Fred Bouchard, SpareTech and Armando Anaya, Northrop Grumman, Conference Co-Chairs

Presentation of 2019 Best Paper and Best Student Paper Awards

- **ASMC 2019 Entegris Best Paper:**
  Using High-Speed Video Analysis for Defect Investigation and Process Improvement
  Adam Chalupa and Eric Ritschdorff, PhD, Samsung Austin Semiconductor
- **ASMC 2019 GLOBALFOUNDRIES Best Student Paper:**
  Simultaneous Denoising and Edge Estimation from SEM Images Using Deep Convolutional Neural Networks
  Narendra Chaudhary and Serap A. Savari, Texas A&M University

9:00AM EDT [SIMULIVE]* — **KEYNOTE** — SPONSOR EDWARDS
Manufacturing Leadership in the Era of Artificial Intelligence
Thomas Sonderman, President, SkyWater Technology

** [SIMULIVE] are pre-recorded presentations releasing at specific times. All presentations are pre-recorded unless specified [LIVE].*

TUESDAY, AUGUST 25

9:00AM EDT [SIMULIVE]

KEYNOTE — SPONSOR EDWARDS

Nanoscale III-V Electronics: A Few Lessons Towards Sustained CMOS Innovation

Jesús del Alamo, PhD, Donner Professor, Professor of Electrical Engineering, Massachusetts Institute of Technology (MIT)

10:15–11:45 [LIVE]

PANEL DISCUSSION — SPONSOR ASNA www.asnaglobal.com

Exascalers, Hyperscalers: Computing at the Edge—Different Modes, Different Nodes

Zoom Webinar login details will be available on the Virtual Keynotes & Panel Discussion *page during the conference.*

Moderator: Paul Werbaneth, Director of Product Management, Ichor Systems

Panelists:

- Buvna Ayyagari-Sangamalli, Head of Design Technology, Applied Materials
- Xavier Lafosse, PhD, Commercial Technology Director, Advanced Optics & Precision Glass Solutions, Corning
- Anna Topol, PhD, Chief Technology Officer, IBM Research
- Carl P. Evans III, Founder, Tercero Technologies

[LIVE] TUESDAY TECHNICAL TRACK OPEN DISCUSSIONS

Join us for nine [LIVE] discussions on Zoom across two days with content experts including speakers, committee, sponsors, and industry peers. It's the perfect opportunity to ask questions, comment, and discuss the nine Technical Tracks. *Zoom Meeting login details will be available on the* Virtual Open Discussions *page during the conference.*

12:00–12:45PM — **PARALLEL SESSIONS**

- **Advanced Equipment Processes and Materials (AEPM)**
- **Contamination Free Manufacturing (CFM)**

1:00–1:45PM — **PARALLEL SESSIONS**

- **Defect Inspection (DI)**
- **Factory Optimization (FO)**

WEDNESDAY, AUGUST 26

9:00AM EDT [SIMULIVE]

KEYNOTE — SPONSOR EDWARDS

Will China Take Semiconductor Industry Lead from USA?

Robert Maire, President, Semiconductor Advisors

10:00 [SIMULIVE]

TUTORIAL — SPONSOR AIR WATER MACH INC. to maximize the ability of seals

Contamination Control

- MaryTheresa Pendergast, PhD, Director of Engineering, Entegris
- Archita Sengupta, PhD, Sr. Technologist, Intel Corporation
- Ryan Pavlick, PhD, Filtration and Purification Technologist, Intel Corporation

[LIVE] WEDNESDAY TECHNICAL TRACK OPEN DISCUSSIONS

Join us for nine [LIVE] discussions on Zoom across two days with content experts including speakers, committee, sponsors, and industry peers. It's the perfect opportunity to ask questions, comment, and discuss the nine Technical Tracks. *Zoom Meeting login details will be available on the* Virtual Open Discussions *page during the conference.*

12:00–12:45PM — **PARALLEL SESSIONS**

- **Advanced Metal Structures (AMS)**
- **Advanced Metrology (AM)**

1:00–1:45PM — **PARALLEL SESSIONS**

- **Advanced Process Control (APC)**
- **Smart Manufacturing (SM)**
- **Yield Enhancement (YE)**

ON-DEMAND TECHNICAL TRACKS

YIELD ENHANCEMENT/YIELD METHODOLOGIES (YE)

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Chairs: Ishtiaq Ahsan, IBM Research; Janay Camp, KLA; Gary Green, Green Technology Consulting; Dieter Rathei, D R Yield; Sagar Kekare, KLA; Reshmi Mitra, Samsung Austin Semiconductor; Larry Pulvirent, SkyWater Technology

1.1 Simulated CWAC to Eliminate First Wafer Effect and Improve Process Capability *(Manuscript Only)*
Kunal Raghuwansi, John LeClair, Dmitry Zhernokletov, Samsung Austin Semiconductor

1.2 Middle of Line (MOL) Process Investigation in Ring Oscillator Failure
Victor Chan, M. Bergendahl, S. Choi, A. Gaul, J. Strane, A. Greene, J. Demarest, J. Li, C. Le, S. Teehan, D Gao, IBM Research

1.3 Characterization of Doped Oxide Films PSG/BPSG/FSG via DSIMS in Order to Eliminate Nonzero Kilometer Failures from Semiconductors Used in Automotive Industry
Thanas Budri, Jeffrey Klatt, Texas Instruments

1.4 Qualifying Inline Xe Plasma FIB—Returning Milled Wafers Back to Production
Franz Niedermeier, Rolf Kammerer, Wolfgang Kipferl, Stephan Henneck, Infineon; Haim Pearl, Applied Materials

1.5 Middle of Line: Challenges and Its Resolution for FinFET Technology
Shiv Kumar Mishra, Erik Geiss, Aditya Kumar, Arkadiusz Malinowsk, Gao Wen Zhi, Wenhe Lin, Bangun Indajang, Dustin Slisher, GLOBALFOUNDRIES

10.1 In-Situ Preclean Run Path Impact on Selective Cobalt Cap Deposition and Electromigration
Matthew Shoudy, Hosadurga Shobha, Huai Huang, Son Nguyen, IBM Semiconductor Technology Research; Chao-Kun Hu, IBM T.J. Watson Research Center

10.2 Machine Learning Assisted Prototyping
Andres Torres, Ivan Kissiov, Richard Gardner, Ken Jantzen, Martin Niehoff, Mohamed Essam, Mentor, A Siemens Business; Stefan Schueler, Carsten Hartig, GLOBALFOUNDRIES

10.3 A Systematic Study on BEOL Defectivity Control for Future AI Application
James H.-C. Chen, Fee li Lie, Scott DeVries, Carol Boye, Sanjay Mehta, Thamarai S. Devarajan, Mary-Claire Silvestre, Wei-Tsu Tseng, Massud A. Aminpur, IBM Research

10.4 Uniformity and Yield Optimization for a Highly Diverse Product Mix
Raymond Van Roijen, Mark Lucksinger, Matthew Fields, Robert Baiocco, Min S. Oh, Derek Stoll, GLOBALFOUNDRIES

5.12 Excursion Prevention Strategy to Increase Chip Performance by Photomask Tuning
Ofir Sharoni, Yael Sufrin, Avi Cohen, Carl Zeiss; Rolf Seltmann, RS-Lithoconsult; Aravind Narayana, Thomas Thamm, GLOBALFOUNDRIES

5.31 Study of Process Window Discovery Methodology for 28 nm and Beyond Technology Node Process Window Limiting Structures
Xingdi Zhang, Hunglin Chen, Yin Long, Kai Wang, Shanghai Huali Integrated Circuit Corporation

5.33 Using GAN to Improve CNN Performance of Wafer Map Defect Type Classification *(Manuscript Only)*
Yongsung Ji, Samsung Electronic; Jee-Hyong Lee, Sungkyunkwan University

5.34 Yield Improvement by Measuring: We Need to Know Where the Particles Come From
Max van den Berg MSc, Festo SE & Co. KG

ON-DEMAND TECHNICAL TRACKS

ADVANCED METROLOGY (AM)

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Chairs: Vivek Jain, ASML; Delphine Le Cunff, STMicroelectronics; Felix Levitov, Applied Materials; Alok Vaid, GLOBALFOUNDRIES; Ronny Haupt, NOVA; Sean Teehan, IBM Research; Padraig Timoney, GLOBALFOUNDRIES; Franz Heider, Infineon Technologies Austria; Jay Mody, GLOBALFOUNDRIES; Brett Williams, ON Semiconductor

2.1 Development of Inner Spacer Process Control to Enable Nanosheet FET Technology
Dexin Kong, Daniel Schmidt, Mary Breton, Abraham Arceo de la pena, Julien Frougier, Andrew Green, Jingyun Zhang, Veeraraghavan Basker, Nicolas Loubet, Ishtiaq Ahsan, IBM Research; Aron Cepler, Mark Klare, Marjorie Cheng, Roy Koret, Igor Turovets, NOVA Measuring Instruments

2.2 The Adoption of Machine Learning in the Measurement of Copper Contact on the Main Chip in Advanced 3D NAND Technology Nodes
Michael Meng, Albert Li, Andrew Zhang, Leeming Tu, Haydn Zhou, Jian Mi, Yangtze Memory Technologies Co.; Xi Zou, Onto Innovations

2.4 Characterization of Sub-Micron Metal Line Arrays Using Picosecond Ultrasonics
M. Mehendale, M Kotelyanskii, R. Mair, P. Mukundhan, Onto Innovation; J. Bogdanowicz, L. Teugels, A.-L. Charley, P. Kuszewski, imec

2.5 Spectroscopic Ellipsometry Imaging for Process Deviation Detection via Deep Learning Approach
Thomas Alcaire, Delphine Le Cunff, Victor Gredy, STMicroelectronics; Jean-Hervé Tortai Université Grenoble Alpe, CNRS, CEA-LETI *(Student Paper)*

11.1 Overlay Improvement for Semiconductor Manufacturing Using Moiré Effect
Yoshinori Hagio, Kentaro Kasa, Sho Kawadahara, Manabu Takakuwa, KIOXIA Corporation; Yosuke Takahata, Katsuya Kato, Akihiro Nakae, Western Digital Corporation

11.2 Improved Duplicate Photomask Matching Using AIMS™ Metrology for 14 nm and Smaller *(Manuscript Only)*
Jean Raymond Fakhoury, Mark Lawliss, Tom Faure, Amy Zweber, Yurong Ying, Chris Magg, Bradley Morgenfeld, GLOBALFOUNDRIES

11.3 SEM Image Denoising and Contour Image Estimation Using Deep Learning
Narendra Chaudhary, Serap A. Savari, Texas A&M University; Varvara Brackmann, Michael Friedrich, Fraunhofer Institute for Photonic Microsystems

11.4 Computational Process Control Compatible Dimensional Metrology Tool: Through-Focus Scanning Optical Microscopy
Ravi Kiran Attota, National Institute of Standards and Technology

15.1 Dimensional Control of Line Gratings by Small Angle X-Ray Scattering: Shape and Roughness Extraction
Jérôme Reche, Patrice Gergaud, Yoann Blancquaert, University Grenoble Alpes, CEA, LETI, Maxime Besacier, University Grenoble Alpes, Guillaume Freychet, NSLS II, Brookhaven

15.2 Advanced Wafer Backside Bevel Characterization Using Geometry Measurement System
André Striegler, Thomas Lindner, GLOBALFOUNDRIES Module One LLC & Co. KG, Dresden, Germany; Florian Flach, Priyank Jain, Chiou Shoei Chee, Madhan Kanniyappan, KLA

15.3 Investigation of Photoluminescence Voltage PL-V Measurement: Correlation to Capacitance Voltage C-V for Si/dielectric Interface Characterization
T. Nassiet, J. M. Bluet, G. Bremond, Université de Lyon; R. Duru, D. Le Cunff, A. Arnaud, STMicroelectronics *(Student Paper)*

15.4 Ultra Large Pitch and Depth Structures Metrology Using Spectral Reflectometry in Combination with RCWA Based Model and TLM Algorithm
Annalisa Del Vito, ST Microelectronics; Ilya Osherov, Adam Michal Urbanowicz, Yinon Katz, Kobi Barkan, Igor Turovets, Ronny Haupt, NOVA

5.23 Roughness and Nanotopography Measurement of a Silicon Wafer Using Wave Front Phase Imaging
J.M. Trujillo-Sevilla, J.M. Ramos-Rodríguez, Juan Trujillo, Jan Olaf Gaudestad, Wooptix

5.32 Tilt Angle and Dose Rate Monitoring of Low Energy Ion Implantation Processes with Photomodulated Reflectance Measurement
A. Pongracz, J. Szívós, F. Ujhelyi, Zs. Zolnai, Ö. Sepsi, Á. Kun, Gy. Nádudvari, J. Byrnes, Semilab; Leonard M. Rubin, Edward D. Moore, Axcelis Technologies

ON-DEMAND TECHNICAL TRACKS

DEFECT INSPECTION (DI)

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Chairs: Alexa Greer, KLA; Israel Ne'eman, Applied Materials; Alex Varghese, IBM Research; Abhishek Vikram, Anchor Semiconductor; Shravan Matham, IBM Research; Oliver Patterson, Hermes Micro-Vision; Qintao Zhang, Applied Materials

3.1 Creative Use of Vector Scan for Efficient SRAM Inspection
Oliver D. Patterson, Hsiao-Chi Peng, Haokun Hu, Hermes Microvision (An ASML company); Chih-Chung Huang, GLOBALFOUNDRIES

3.2 Analysis of Systematic Weak Point Structures Using Design Based Automatic Defect Classification and Defect Review SEM Platform
Teresa A. Esposito, Felix Levitov, Applied Materials; Shi-Hui Jen, Qian Xie, Danda Acharya, Julie Lee, GLOBALFOUNDRIES

3.3 Electron Beam Inspection: Voltage Contrast Inspection to Characterize Contact Isolation
Richard F. Hafer, Andrew Stamper, GLOBALFOUNDRIES; Jerry Hsieh, Hermes Microvision Inc.

3.4 Double Feature Extraction Method for Wafer Map Classification Based on Convolution Neural Network
Yuan-Fu Yang, Min Sun, National Tsing Hua University *(Student Paper)*

3.5 Generative Adversarial Networks for Synthetic Defect Generation in Assembly and Test Manufacturing
Rajhans Singh, Arizona State University and Intel; Ravi Garg, Nital S. Patel, Martin W. Braun, Intel Corporation

8.1 Automated Wafer Defect Classification Using a Convolutional Neural Network Augmented with Distributed Computing
Hairong Lei, Cho Teh, Hetong Li, Po-Hsuan Lee, Wei Fang, Hermes Microvision (An ASML company)

8.2 Advanced Inspection Methodology for the Maximum Extension of Nitride Test Wafer Recycling
Yu-Yuan Ke, Kuang-Hsiu Chen, Shin-Ru Chen, Guan-Wei Huang, Wesley Yu, Po-Jen Chuang, Chun-Li Lin, Chih-Wei Huang, Jun-Ming Chen, United Microelectronics Corporation; Nachiketa Janardan, Tung-Ying Lee, Ethan Chen, Chao-Yu Cheng, Shao-Ju Chang, KLA

8.3 Laser-Based Hair Crack Detection on Wafers
Alexander Fuchs, Franz Pernkopf, Graz University of Technology; Robin Priewald, Bright Red Systems *(Student Paper)*

8.4 Real-Time Tool Health Monitoring and Defect Inspection During Epoxy Dispense Process
Chris Edwards, Meghana Narayana Swamy, Ravi Garg, Tim Karaniuk, Cody L. Morgan, Debashis Panda, Intel Corporation

5.16 In-Line Photoresist Defect Reduction Through Failure Mode and Root-Cause Analysis
S. Goswami, S. Hall, W. Wyko, J.T. Elson, J. Galea, J. Kretchmer, General Electric Global Research Center

5.19 NextGen Calibration Utility for Tool Setup and Matching in Real-Time Automated Visual Inspection Systems
Chris Edwards, Cody L. Morgan, John Rudolph, Danniel Slinker, Debashis Panda, Intel Corporation

5.20 Particle Improvement for Low-K Process in Diffusion Furnace *(Manuscript Only)*
Viboth Houy, Janice Lam, Halima Ali, Samsung Austin

5.30 Systematic Missing Pattern Defects Introduced by Topcoat Change at PC Lithography: A Case Study in the Tandem Usage of Inspection Methods
M. Fields, R. VanRoijen, M. Lucksinger, GLOBALFOUNDRIES

ON-DEMAND TECHNICAL TRACKS

ADVANCED EQUIPMENT PROCESSES AND MATERIALS (AEPM)

SPONSOR

Chairs: Thirumalesh Bannuru, Applied Materials; Katie Lutker, TEL; Jean Wynne, IBM Research

4.1 Comparing PVD Titanium Nitride Film Properties and Their Effect on Beyond 7 nm EUV Patterning
Scott DeVries, Ekmini Anuja De Silva, Donald Canaperi, Andrew Simon, Abraham Arceo de la Pena, Wei Wang, Joseph Maniscalco, Luciana Meli, Brock Mendoza, IBM Research

4.3 Oval-Shaped OP-Layer Hole Etching: Shape Deformation, Local Arcing and Hole Bridging Improvements
Zusing Yang, Yao-Yuan Chang, Ming-Tsung Wu, Hong-Ji Lee, Nan-Tzu Lian, Tahone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co.

4.4 PMOS SiGe Epitaxial Growth Process Improvement to Increase Yield and Throughput *(Manuscript Only)*
Vikas Kaushal, Rakesh Mahadevapuram, Guozhen Yue, Arvind Raviswaran, Samsung Austin Semiconductor

4.5 Energy Density and Temperature Calibration for FEOL Nanosecond Laser Annealing
Yasir Sulehria, Oleg Gluschenkov, IBM Research; Michael Willemann, Shaoyin Chen, Thirumal Thanigaivelan, Veeco Instruments

5.4 Characteristics of SiGe Oxidation and Ge Loss According to Ge Content *(Manuscript Only)*
Meejung Kwon, Songl Han, Je Hyeok Ryu, Chiyoung Lee, Yoon Young Lee, Byoung Hoon Kim, PSK

5.6 Effect of In Situ Capping on Phase Change Memory Device Performance
K. W. Brew, R. Conti, I.Saraf, G. Rodriquez, M. Lippitt, N. Saulnier, IBM; Y. Xu, S. Manita, T. Masuda, T. Jimbo, ULVAC

5.13 Impact of Asymmetric Memory Hole Profile on Silicon Selective Epitaxial Growth in 3D NAND Memory
Yao-Yuan Chang, Zusing Yang, Ming-Tsung Wu, Hong-Ji Lee, Nan-Tzu Lian, Kuang-Chao Chen, Tahone Yang, Chih-Yuan Lu, Macronix International Co., Ltd.

5.24 Science of Sealing: Advanced Materials for High-Temperature Applications
Thomas S. Reger, Gary J. Reichl, Greene, Tweed

5.25 Selective Metal Deposition to Increase Productivity *(Manuscript Only)*
Robert L. Rhoades, Revasum; Rashid Mavliev, IPGrip; Knut Gottfried, Fraunhofer ENAS

ON-DEMAND TECHNICAL TRACKS

ADVANCED PROCESS CONTROL (APC)

SPONSOR

Chairs: John Jensen, Lam Research; Agnes Roussy, École des Mines de Saint-Étienne; Raymond van Roijen, GLOBALFOUNDRIES

6.1 Towards Excursion Detection for Implant Layers Based on Virtual Overlay Metrology
Leon van Dijk, Kedir Adal, Maialen Larrañaga, Richard van Haren, ASML; Mathias Chastan, Laboratoire Jean Kuntzmann; Auguste Lam, STMicroelectronics

6.2 Advanced Process Control (APC) for Selective EPI Process in 300 mm Fab
Hongying Peng, Jonathan Caruso, Dinesh Balasubra Manian, Shiladitya Chakravorty, Ryan Mickelson, Jensen Tay, Stephen Cabral, Lixin Lu, Churamani Gaire, Judson Holt, Glyn Braithwaite, Dali Shao, Wei Hua Tong, GLOBALFOUNDRIES

6.3 Novel Overlay Correction by Synchronizing Scan Speed to Intra-Die Fingerprint on Lithography Scanner
Masakazu Hamasaki, Yoshinori Hagio, Kentaro Kasa, Yoshimitsu Kato, Manabu Takakuwa, KIOXIA Corporation; Tsutomu Obata, Shunichi Nakao, Manabu Miyake, Katsuya Kato, Yosuke Takahata, Akihiro Nakae, Western Digital Corporation

6.4 A Data Mining for Real Time Process Monitoring with Mass Spectrometry *(Manuscript Only)*
Soyeon Park, Sungbin Lee, Eunsun Hong, Bumsik Kim, Jihye Yi, Gyeom Kim, Jinho Kim, Jungdae Park, Samsung Electronics

6.5 A Framework for Semi-Automated Fault Detection Configuration with Automated Feature Extraction and Limits Setting
Jianshe Feng, Haoshu Cai, Jay Lee, University of Cincinnati; Michael Armacost, James Moyne, Jimmy Iskandar, Fei Li, Applied Materials

5.7 Effect of Sparse or Asymmetric Sampling on the Estimation of Photolithography Overlay Regression Parameters
Tim Conway, Ronak Kamat, SkyWater Technology

5.11 Estimation of Process Time Delay Between Chamber Measurements and Optical Emission Spectrum
Taikang Ning, Trinity College; CH Huang, J. A. Jensen, V. Wong, H. Chan, Lam Research

5.22 Repeatability of Nanoimprint Lithography Followed Through Line Roughness Extraction
Hubert Teyssedre, Jérôme Reche, University Grenoble Alpes, CEA, LETI; Florian Delachat, Intitek for Industry; Manuela Stirner, Jonas Khan, Peter Ledel, EV Group *(Student Paper)*

ON-DEMAND TECHNICAL TRACKS

FACTORY OPTIMIZATION (FO)

SPONSOR

Chairs: Thomas Beeg, Wolfspeed; Jagdish Prasad, Silfex (Lam Research); Stefan Radloff, Intel Corporation; Dave Gross, SkyWater Technology; Alin Ila, Intel; Patrick R. Varekamp, PhD, GLOBALFOUNDRIES

7.1 AMHS Capability Assessment Based on Planned Product Mixes
Robert Schmaler, Christian Hammel, FabFlow GmbH; Christian Schubert, Infineon Technologies Dresden

7.2 An Artificial Neural Network Based Algorithm for Real Time Dispatching Decisions
Shiladitya Chakravorty, GLOBALFOUNDRIES; Nagendra N. Nagarur, Binghamton University

7.3 Order Release Methods in Semiconductor Manufacturing: State-of-the-Art in Science and Lessons from Industry
Jacob Lohmer, Christian Flechsig, Rainer Lasch, Technische Universität Dresden; Konstantin Schmidt, Benjamin Zettler, Germar Schneider, Infineon Technologies Dresden *(Student Paper)*

7.4 Output Improvement in High Volume Fabs by Reducing Recipe Qualifications
Ace Chen, Chris Keith, Maryam Anvar, Haim Albalak, Applied Materials

7.5 Dynamic Dispatching for FOUP Cleaning
Karthik Iyer, John Barker, Shiladitya Chakravorty, Binay Dash, GLOBALFOUNDRIES

14.1 Eliminating He as Wafer Cooling Gas in PECVD Wafer Fabrication Equipment *(Manuscript Only)*
Gerald Joseph Brady, Jon David Sumega, Terry Powell, Eric Madsen, Lam Research

14.2 Method for Improving Stability of Plasma Ignition of Target X in a Multi-Cathode Magnetron PVD System
Jessica Gruss-Gifford, Virat Mehta, Oscar van der Straten, Gabriel Rodriguez, Maxwell Lippit, Donald Canaperi, IBM Research

14.3 ALD TiN Surface Defect Reduction for 12 nm and Beyond Technologies
Aditya Kumar, Kyle Pratt, Olugbenga Famodu, Bhavyen Patel, GLOBALFOUNDRIES

14.4 A High Throughput PMOS Source-Drain Process Optimized within FINFET Architecture for High Volume Chip Manufacturing *(Manuscript Only)*
Rakesh C. Mahadevapuram, Vikas K Kaushal, Arvind Raviswaran, Samsung Austin Semiconductor

5.2 Additive Manufacturing Applications for Quality Improvement and Cost Reduction *(Manuscript Only)*
William James Blalack, Samsung Austin Semiconductor

5.8 Empirical Relationship between Cycle Time Impact and Batching on Furnaces in Semiconductor Foundry
Nivedha Rajasekaran, Vikram Arjunwadkar, Richard Man, GLOBALFOUNDRIES

5.17 Innovative Approach on Dynamic Behavior of LPCVD Nitride Process on Diffusion Furnace *(Manuscript Only)*
Satyajit Shinde, Chee Huei Chan, Marcus Minchew, Lawrence Mbonu, Samsung Austin Semiconductor

5.21 Practical Considerations for High Throughput Wafer Level Tests of Silicon-Photonics Integrated Devices
Kate McLean, Calvin Ma, Subharup Gupta Roy, Fen Guan, Hanyi Ding, Bart Green, GLOBALFOUNDRIES

5.27 Staggering Preventive Maintenance Actions at CMP Using a Dispatching Algorithm
Srikanth Ramakrishnan, Shiladitya Chakravorty, Jensen Tay, David Olsen, Peter Zumpano, GLOBALFOUNDRIES

ON-DEMAND TECHNICAL TRACKS

SMART MANUFACTURING (SM)

SPONSOR

Chairs: Eric Eisenbraun, SUNY Polytechnic Institute; Jan Rothe, GLOBALFOUNDRIES; Satyajit Shinde, Samsung Austin Semiconductor

9.1 Reinforcement Learning for Efficient Scheduling in Complex Semiconductor Equipment
Doug Suerich, Terry Young, PEER Group

9.2 Improving Factory Scheduling with Statistical Analysis of Automatically Calculated Throughput *(Manuscript Only)*
Holland Smith, Cabe Nicksic, INFICON FPS

9.3 Trace Data Analytics with Knowledge Distillation
Janghwan Lee, Wei Xiong, Samsung Electronics; Wonhyouk Jang, Samsung Display

9.4 Q-Learning Based Route-Guidance and Vehicle Assignment for OHT Systems in Semiconductor Fabs *(Manuscript Only)*
Young Jae Jang, Illhoe Hwang, Department of Industrial and Systems Engineering, KAIST

5.9 Environmental Improvements Through Media Packaging *(Manuscript Only)*
Ryan Parrott, Patrick Dunaway, Intel Corporation

5.18 Integrated Sub-Fab Monitoring System Improving Data Visibility and Abatement Uptime
Xin Li, Scott Veirs, Tony Betts, John Dalziel, Ania Zemlerub, Yuee Feng, Edwards Vacuum; Dinesh Saigal, Applied Materials

ADVANCED METAL STRUCTURES (AMS)

Chairs: Marc Bergendahl, IBM Research; Shubhodeep Goswami, GE Global Research; Rob Pearson, Rochester Institute of Technology

12.1 Nano Ni/Cu-TSVs with an Improved Reliability for 3D-IC Integration Application
M. Murugesan, K. Mori, H. Hashimoto, J.C. Bea, T. Kojima, T. Fukushima, M. Koyanagi, Global INTegration Initiative (GINTI), NICHe, Tohoku University

12.2 Polysilicon Fuse Electrical Voiding Mechanism
Gang Liu, Rommel Relos, Bohumil Janik, Robert Davis, Tracy Myers, Derryl Allman, Jeff Hall, Steven Vandeweghe, Santosh Menon, Ed Flanigan, ON Semiconductor

12.3 Aluminum Voiding and Delamination Induced by High Intrinsic Stress
Cindy Daigle, Michelle Beauchemin, Thomas Moutinho, Christopher Qualey, Texas Instruments

12.4 Bondpad Design Structural vs. Electrical Tradeoffs
Brett Williams, Robert Davis, Justin Yerger, Derryl Allman, Bruce Greenwood, Troy Ruud, ON Semiconductor

ON-DEMAND TECHNICAL TRACKS

CONTAMINATION FREE MANUFACTURING (CFM)

SPONSOR

Chairs: Jennifer Braggin, Entegris; Christopher Ebert, Linde; Christopher Long, IBM Research

13.1 Particle Defect Reduction Through YF3 Coated Remote Plasma Source for High Throughput Dry Cleaning Process *(Manuscript Only)*
Hyojeong Seo, Jeonghye Yang, Young Jae Ma, Jongwoo Park, Mi Kyoung Kim, David H. Seo, Sung Jin Yoon, Sang Jong Park, PSK Inc.

13.2 Impact of Process Chambers Exhaust on Wafer Defectivity in Wet Clean Tools
Kedari Matam, Brown Peethala, Charles Taft, Zachary Gardner, Michael Liefels, George Yang, Sankar Muthumanickam, Devika Sil, IBM Semiconductor Technology Research

13.3 Formation and Removal of Tungsten Flake and Metallic Film Defects in Tungsten Contact CMP
Bryan Egan, Robert Solan, Hong Jin Kim, GLOBALFOUNDRIES

5.1 5000+ Wafers of 650 V Highly Reliable GaN HEMTs on Si Substrates: Wafer Breakage and Backside Contamination Results
Saurabh Chowdhury, YiFeng Wu, Likun Shen, Lee McCarthy, Primit Parikh, David Rhodes, Transphorm USA; Tsutomu Hosoda, Kotani, Kenji Imanishi, Yoshimori Asai, Tsutsumo Ogino, Kenji Kiuchi, Aizu Fujitsu Semiconductor Wafer Solutions (AFSW)

5.3 Back-Side Residue Analyses and Reduction in FinFET Middle of Line Wafers CFM: Contamination Free Manufacturing *(Manuscript Only)*
Reshmi Mitra, Alper Konuk, Samsung Austin Semiconductor