Packaging Integration
- A Complementary Solution to CMOS Scaling
利用封装集成技术应对CMOS缩微挑战

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2019.03.21
Higher performance and increased functionality
Smaller form factor, lower power consumption, lower cost.

- Multiple sensors
- High density integration
- Low power consumption
- Smaller packaging profile
- High reliability
CMOS TO PACKAGING SCALING

**CMOS scaling becomes difficult**

- Technology nodes become more and more expensive

**Packaging scaling becoming attractive**

- High density system level packaging solutions become available
ADVANCED PACKAGING REQUIREMENTS

**Advanced Packaging Technologies**

**Cost**
- Lower packaging cost
- Lower test cost

**Number of I/Os**
- Lower pitches
- No standard
- Smaller dies
- Higher density of I/Os

**Variable Integration**
- IPD
- System in Package
- 3D

**Form-factor**
- Lower Z-height
- Smaller footprint

**Electrical performance**
- Smaller Interconnect lines
- Higher frequencies
- Higher package speed
- Lower parasitics

**Thermal performance**
- Lower power consumption
- Higher package density

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ADVANCED PACKAGING TREND

**DENSITY**
- High Capacity / mm³
  - Package on Package

**POWER**
- Lower Power Use
  - Package in Package

**BANDWIDTH**
- Quicker Data Transfer
  - TSV/FC Stacking

SiP

PoP

More components & performance in the same area / cost
2D to 3D offers short interconnections between modules and enable flexible and scalable platforms
ADVANCED PACKAGING FORECAST

- Multiple players from both OSAT, Foundry and IDM
- Growth rate higher than industry average with FO CARG @36%
EARLY ADOPTIONS OF ADVANCED PACKAGINGS

WLCSP Device Categories

Analog & mixed signal
- IPD
- PA/BAW/SAW
- IC drivers
- PMU
- A & V

Wireless Connectivity
- RF Transceiver
- BT+FM+WLAN
- WLAN
- GPS, AGPS
- Radar

Opto
- CMOS image sensor
- ALS

MEMS & sensors
- Inertia sensor (Accel/Gyro)
- Magnetic
- Oscillator
- FBAR/BAW filters
- Gas and chemical sensors

Misc Logic and Memory
- Logic gates
- EEPROM/DRAM/SRAM/Flash
- MCU

• Advantage of Fan-in: A good fit for consumer electronics
Fan-out has certain advantages over Fan-in and FCBGA

- High board level reliability
- Higher potential of SiP integration
- Relatively small footprint

- Shorter interconnection
- Thinner package
- Lower cost and
By 2030, FO-SiP along with 2.5D/3DIC could be replacing most single die packaging today.
DIFFERENT F-O’S

Not all Fan-outs look the same, but they all aim to achieve the same goal using new interconnects such as TSV, bumping and RDL

- High integration with low profile
- Scalable system packaging capabilities
- High reliability with new materials
- From homogeneous to heterogenous
**CWLCSP i-COR STRUCTURE**

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Fan Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass Thickness</td>
<td>200–400um</td>
</tr>
<tr>
<td>Organic Substrate Thickness</td>
<td>400um</td>
</tr>
<tr>
<td>RDL Type</td>
<td>Fan Out</td>
</tr>
<tr>
<td>RDL on Compliant Layer</td>
<td>Ti/Cu</td>
</tr>
<tr>
<td>Interconnect</td>
<td>Au Stud Bump</td>
</tr>
<tr>
<td>Sensor Assembly on Glass</td>
<td>Flip Chip</td>
</tr>
<tr>
<td>Second level interconnect</td>
<td>BGA</td>
</tr>
</tbody>
</table>

**Sample Structure**

**Front Side View**

**Back Side View**

Sample Structure
## RELIABILITY RESULTS

<table>
<thead>
<tr>
<th>TSV CSP Configuration</th>
<th>Package Quall</th>
<th>Product Quall</th>
<th>Pre-con</th>
<th>THS (85℃/85%RH)</th>
<th>TCT(-55/+125℃)</th>
<th>HTS(+125℃)</th>
<th>LTS(-50℃)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Internal</td>
<td>Customer</td>
<td>MSL3</td>
<td>MSL2</td>
<td>168 504 1008</td>
<td>200 500 1000</td>
<td>168 504 1008</td>
</tr>
<tr>
<td>Fan-out CIS (Glass substrate)</td>
<td>✔</td>
<td>✔</td>
<td>0/154</td>
<td>-</td>
<td>0/77 0/77 0/77</td>
<td>0/77 0/77 0/77</td>
<td>0/45 0/45 0/45</td>
</tr>
<tr>
<td>Fan-out CIS (Organic substrate)</td>
<td>✔</td>
<td>✔</td>
<td>0/154</td>
<td>0/154</td>
<td>0/77 0/77 0/77</td>
<td>0/77 0/77 0/77</td>
<td>0/45 0/45 0/45</td>
</tr>
<tr>
<td>SIP CIS (Organic substrate)</td>
<td>✔</td>
<td>✔</td>
<td>0/154</td>
<td>0/154</td>
<td>0/77 0/77 0/77</td>
<td>0/77 0/77 0/77</td>
<td>0/45 0/45 0/45</td>
</tr>
</tbody>
</table>
I-COR DUAL CAMERA PACKAGE SOLUTION

**Key Feature**

- Two CIS sensors in one package
- Best Coplanarity and assembly accuracy between two sensors
- Interconnect two sensors in 1st level package
- Different optical coating glass can be integrated in one package
- Additional chips (ie: DSP, Memory...) can be integrated to realize more powerful and compact SIP solution
Si BASED FAN-OUT

* Related IP already been issued since 2010

Si interposer R&D in CWLCSP

* Various structures of Si interposer (IP owned by China WL CSP)

Confidential
COMPANY HIGHLIGHTS

- Founded in 2005
- Approximately 1800 employees worldwide
- Listed on the Shanghai Stock Exchange: #603005
- Proven high-volume sensor technologies – multiple billions shipped

- Pioneered China wafer level Through Silicon Via (TSV) and Lens manufacturing industry
- Focused on driving innovation and growth through customer partnerships
- Broad internally developed and acquired technology & IP portfolio

Numerous growth opportunities targeting multi-billion dollar markets
- Imaging, Biometrics and Structured Light for mobile, security, automotive and industrial applications
FOCUSED ON SENSOR SOLUTIONS

Three major areas of our focus
- Optical
- Imaging
- Biometrical

Standardized and custom sensor application solutions
- Miniaturization & Integration
  - Single sensor packages
  - Integrated modules
  - Multi-sensor modules
  - Monolithic Integration

Diversified business with balanced application and customer portfolio
- Balanced product mix
- Broad customer base in each application
- Strong supply chain partnership

Clear financial target model
- Services revenues growth target (CAGR) 2018-2020 of more than 200%

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Instead of W/B, advanced packaging service providers use new interconnects such as TSV, RDL, bumping and various bonding techniques as building blocks to realize more complex structures.
OUR BUSINESS GOAL IS TO BE THE GLOBAL LEADER IN SENSOR SOLUTIONS

Our Mission: Invent, develop, and commercialize unique sensor and system level miniaturization technologies to enable intelligent devices everywhere.

Technology Center
Palo Alto, CA
- Technology Research
- IP Management
- Technology Research & Intellectual Property Development

Headquarters
Suzhou, CH

Operations Center
Suzhou, CH
- Interconnect, Package, Optical Module Design
- Process Development, Integration and Testing
- Product Development & High Volume Manufacturing

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### Structure Through Silicon Via Micro-Via in Trench

<table>
<thead>
<tr>
<th>Structure</th>
<th>Through Silicon Via</th>
<th>Micro-Via in Trench</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV Isolation</td>
<td>PECVD (SiO₂, Si₃N₄)</td>
<td>PECVD (SiO₂) or Polymer</td>
</tr>
<tr>
<td>TSV metallization</td>
<td>Aluminum (Al) or Titanium / Copper (Ti/Cu)</td>
<td>Aluminum (Al) or Titanium / Copper (Ti/Cu)</td>
</tr>
<tr>
<td>TSV aspect ratio</td>
<td>≤ 1:10</td>
<td>≤ 1:5</td>
</tr>
<tr>
<td>TSV diameter</td>
<td>≥ 35µm</td>
<td>≥ 40µm</td>
</tr>
<tr>
<td>TSV pitch</td>
<td>≥ 70µm</td>
<td>≥ 80µm</td>
</tr>
<tr>
<td>TSV Process</td>
<td>Via silicon etch followed by dielectric deposition</td>
<td>Trench and micro-via silicon etch followed by dielectric coating</td>
</tr>
</tbody>
</table>

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12-INCH CIS TSV CSP PACKAGE CONFIGURATIONS

I - µVia in Via

- Si trench etching followed by Via over the pad opening and Pad laser drilling
- Via Isolation material: Photoimagable Polymer
- Through Pad CA: Line\(2\pi r PT\)
- Reliability: JEDEC MSL 3 / 4
- Designed for Low Cost

II - Via in Trench

- Si trench etching followed by Via over the pad opening
- Via Isolation material: PECVD (SiO2) and Polymer
- On Pad Surface Landing, Contact Area: Surface\(\pi r^2\)
- Reliability: JEDEC MSL 2 / 3 / AEC-Q100 Grade-2

III - Vertical Via

- Single Via etching over the bond pad
- Via Isolation material: PECVD (SiO2) and Polymer
- Designed for Versatile Sensor Designs and High Product Reliability

Available with (1) Cavity substrate cover, with (2) directly bonded optically transparent substrate or (3) without protective substrate
RAPIDLY EXPANDING FAN-OUT PACKAGING MFG INFRASTRUCTURE

VERSATILE STRUCTURE

- Developed for image sensors with large pixel array
- The design allows integration of multiple sensors in a single package.
- Available with and without AR/IR coated optical glass, with and without back side sensor shielding
- JEDEC Level 1 & 2 moisture sensitivity
FINGER-PRINT SENSORS

PROCESS:
- TSV packaging
- Sensor assembly on the substrate
- Encapsulation and module assembly

MANUFACTURING CAPACITY UP TO 120M MODULES

BENEFITS:
- Ultra-thin module height
- Small form factor (X,Y,Z)
- Versatile design
- Low noise level - performance enhancement
- Scratch resistant surface
- JEDEC Level 1 & 2 moisture sensitivity

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OPTICAL COMPONENTS

• Optical surface quality:
  - PtV < 1 µm
  - Roughness <10nm
• Available with and without AR/IR coated optical glass, with and without sensor back side shielding
• Reliability: JEDEC Level 2 & 3
MEMS PACKAGING SOLUTIONS FOR ULTRA-SMALL DEVICES

W2W and D2W integration for ultra small systems packaging

- Wafer Level TSV Package
  - Concept
  - Wafer to Wafer Bonding
  - Capping Substrate
  - MEMS

- Stack Die Package
  - Die to Wafer Bonding
  - Die to Die Bonding

- TSV SIP
  - Fine Pitch TSV Die Stack

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THE COMPLETE TURNKEY SOLUTIONS

**Design & Logistics Solutions**
- Design chain management
- Design for Manufacturing (DFM)
- Design for Cost (DFC)
- Full design and verification of WL, leadframe, laminate, etc. platforms
- Electrical, thermal, mechanical and optical characterization
- Quick turn prototype service

**Assembly & Testing**
- Turnkey solutions for TSV, Wire Bond and Flip Chip
- High-volume Wafer Level lens manufacturing
- 3D components assembly
- Wafer to wafer and die to wafer bonding, micro-joining
- Integrated and SMT passives
- Sensor module design and manufacturing

**FA & Reliability**
- Package, module and board-level
- Bump reliability
- Underfill / EMC adhesion
- Drop tests, bend tests, solder joint reliability
- Materials Lab
- Failure Analysis

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OUR INNOVATION ENGINE DRIVES PATENT GROWTH

Hundreds of issued patents and patent applications

Broad Distribution of Patent Assets

Note: Asset categorization denotes illustrative area of applicability only.
Advanced Packaging Challenges

- Advanced packaging viewed as replacement/augmentation of Moore’s law, i.e, More than Moore
- The roadmap grows from WLP, F-O, SiP and ultimately 3D
- We are quickly entering the IOT and AI Era, which drives the need for various new types of packaging such as fan-out and heterogeneous system integration
- Wafer-level technologies were firstly adopted some products, with fan-out gaining traction at this moment. Both wafer and panel technologies are being developed
- Cost reduction and yield improvement remain as challenges
Enabling Smart Objects Everywhere

Smaller | Lower Power | Intelligent | Sensing