Global Assembly & Packaging Market Overview

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Market Driven Products - Equipment

Ball Bonders
- IConn ProCu
- IConn
- ConnX Plus
- ConnX
- ConnX-LED
- ConnX-VLED

Wafer Level Bonders
- PowerFusion
- 3700Plus 3600Plus
- ATPremier Plus

Manual Wire Bonders
- iBond5000
- 4700
- 4522
- 4524
- 4526

Software
- KNet
- AutoOLP

Service
- K&S Care
Market Driven Products - Consumables

Capillaries

- iCap
- DuraCap
- ARCUS
- SIGMA II
- Fortus
- NEXXUS
- CIC
- Lumos

Capillary for Gold Wire Bonding

Capillary for Copper Wire Bonding

Wedge Tools

- Wedge Tools
- Ribbon Tools

Dicing Blades

- Opto PCB
- Opto ceramic
- Uni Plus
- Silicon
- AccuPlus
- Copper
- Nova

New

Blades for Package Singulation

Blades for Wafer Dicing
Semiconductor Assembly Overview
– Wire Bond Perspective

Kulicke & Soffa
Technology . Innovation . Solutions
IC Package Assembly Market

- IC Shipment had been growing steadily and continue to grow
- Growth driver – mobile and communication devices
Assembly Packaging Trend

- IC growth is driven by mobile devices – hand-phone, media tablet, and notebook computers
- There are more mobile phones than people on earth
- Demand for mobility and usability drives packaging miniaturization – reduce weight and power consumption
- Mobile gadget gets smaller and increase functionality – demand for more IC per unit, either integrated or/and smaller
- About 80% of IC packages are wire bonded – the balance uses flip chip and other interconnect technologies
- Packaging cost drives the conversion of gold bonding wire to copper - ~35% of packages are copper wire bonded
Semiconductor Fabrication Supply Chain - 2012

Semiconductor Industry $292B
Wafer Fabrication $123B
Design, G&A & Profit $91B
Test $34B
Assembly $44B
Assembly Process $26B
Assembly material $18B
Assembly Equipment $4.2B

Source: Prismark

OSAT share of total assembly & test market: ~41%
IC Packaging Value

Source: Prismark
Packaging Demand

- Demand for performance and mobility resulted
  - Increased functionality per chip – higher I/O
  - Squeeze higher I/O on a smaller chip – finer pitch
  - Stacked die
  - Smaller package size – lower package height – lower loop
- Lower cost
  - High density matrix packaging – larger LF configuration
  - Copper wire
  - More productive equipment
Ultra Fine Pitch Applications

- Chip complexity and functionality integration increases I/O count per chip
- Chip size reduction means a finer pitch pad is necessary to pack all the I/O in
Looping Requirement

- Standard Package
- Small Size & High Density
- Multi-stacked & PoP
- Higher Stack >10 die stacked

Loop Height

- >8mil
- >4mil
- <3mil
- <2mil

Ultra Low Loop
Advanced Loop

QDP
SIP
MCP
MCP-I (4 Chip)
DDP

Confidential
Ultra Low Loop

- As mobile gadget gets smaller, packaging gets smaller and thinner
- Thinner packages and more complicated chip demand advances in packaging technology – finer pitch, lower loop height, multi-layer wire, complicated layout
A Slow Start To High Volume Copper Ball Bonding – now at Full Speed

Higher End = Higher Wire Count
As gold wire becomes a larger portion of the packaging cost, the drive to minimize gold content accelerates the copper transition

Increasing maturity of copper ball bonding process & cost advantage

1990s to early 2000s
Performance in High Power Devices (TO & SO)

Early Development & Low Volume Production

Mid 2000s
Low Pin Count ICs (SOIC & PDIP)

Late 2000s
High Pin Count ICs (BGA & QFP)

High volume production started in late 2009
Copper Wire Transition

- Process Knowledge
- Process Stability
- Equipment, Tools, & Wire Knowledge
- Gold to Copper Transition
- Reliability Knowledge
- New Production Methods
- High Volume Production

Calendar Year

Q4 2007, Q1 2008, Q2 2008, Q3 2008, Q4 2008, Q1 2009, Q2 2009, Q3 2009, Q4 2009, Q1 2010, Q2 2010, Q3 2010, Q4 2010, Q1 2011, Q2 2011, Q3 2011, Q4 2011, Q1 2012, Q2 2012, Q3 2012, Q4 2012, Q1 2013, Q2 2013, Q3 2013, Q4 2013
COMPARISON OF 500 CSP PACKAGING COST
(Assumes High Volume)

Source: Prismark
Finer pitch and higher productivity are values that help improve packaging cost.

Pitch had reached its limit and productivity growth is expected to continue.
Accelerates Copper Transition

- K&S introduced IConn ProCu<sup>PS</sup>, an advanced copper wire bonder
  - Faster throughput with specialized copper processes, ProCu Bond and ProCu SSB
  - **New process tools and features that make the complex capabilities easy to use**

- Robust solution enable customer to accelerate transitioning to copper wire bonding production
- R&D has shifted towards developing solution that enable ease-of-use and capability to bond the latest technology node
IC Packaging Moving Forward

- Wire bonded packages continue to dominate in the near future
  - Most versatile and cost effective solution
  - Copper wire had reduces packing cost significantly and had demonstrated capability to bond on 28nm node chip – R&D on next node
  - Conversion to copper is a necessity to be competitive, silver alloy wire is a possible alternative
- Flip-chip will grow at a faster rate in the high performance chip segment – CPU, GPU, AP,…
  - IC performance requirement will drives FC growth despite the higher cost
- Cost and package size will determine the mode of interconnect
- Material cost, efficient process, productivity are some of the cost driver
- R&D in wire bonding will continue to challenge the technological boundary to stay relevant
- OSAT growth with exceed IC shipment growth – as fabless companies grow and IDM outsource mode
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