Global Semiconductor Packaging Materials Outlook

EXECUTIVE SUMMARY

Semiconductor Equipment and Materials International (SEMI®) and TechSearch International, Inc. have cooperated in the development of Global Semiconductor Packaging Materials Outlook, a comprehensive market research report on the global semiconductor packaging materials markets. Interviews were conducted with more than 140 semiconductor manufacturers, packaging subcontractors and packaging materials suppliers to gather information for the report.

Following a record year in terms of semiconductor sales and unit shipments, 2011 turned into a low growth year as challenges across the global economy resurfaced. The Tohoku earthquake and tsunami disrupted the industry supply chain as numerous key suppliers, in particular several leading packaging materials suppliers, lost production capability for several weeks and longer. Large customers experienced less of an impact from supply shortages than smaller fabless companies. Suppliers in other geographic regions, such as Korea and Taiwan, will likely experience some increase in market share as they compete with Japanese suppliers and as customers diversify purchases geographically.

By the second quarter, the supply chain had largely recovered and the semiconductor industry showed signs of improving. The rebound in part was likely the result in inventory replenishment as global economic challenges resulted in clearly slower industry conditions in the third quarter and into the fourth quarter.

Packaging technology continues to be an important industry segment enabling growth in electronics that are increasing in functionality in a mobile form factor. Demand for smartphones and media tablets exploded throughout the 2010 recovery and into 2011. Important growth areas in packaging include chipscale packaging (CSP)—both laminate and leadframe based, stacked-die and other 3-D packaging form factors, wafer-level packaging (WLP), power device packaging, LED packaging, and other system-in-package (SiP) type technologies. The outlook for advanced packaging continues to remain strong, and this includes ball grid array (BGA), CSP (including leadframe-based), flip chip, and WLP packages. These package types will have strong unit growth rates over the next four years. More traditional packaging technologies will see demand stagnant or grow at single-digit rates.

Materials are critical in achieving demanding performance and reliability requirements, especially as the semiconductor industry migrates to 28 nm and below silicon technology. The increase number of materials and layers within packages introduce issues of compatibility and interactions within the package and post-packaging at the board level. Thermal dissipation and electromigration are issues to be addressed, in part, through materials in emerging package applications. All the issues and challenges to be addressed require “low cost” material solutions so pressure continues for suppliers to solve the technical issues while delivering a low cost material to the customer.

As such downward pricing pressures remain a constant issue across the industry, though rising raw material costs continue squeeze both suppliers and their customers. Higher material prices have impacted the market for bonding wire, die attach,
solder balls and other materials. For bonding wire, copper wire now represents about 22% of the market. This transition has resulted in the need for newer mold compound, liquid encapsulant, and die attach formulations to reduce chloride ion content and moisture uptake as copper wire is more susceptible to corrosion. Other new material suppliers continue to introduce products, so a market long been dominated by Japanese manufacturers is undergoing some changes as non-Japanese companies advance in their product offerings.

Advancements and changes continue in the semiconductor packaging materials market, and over the next several years some opportunity areas include:

- Bump pitch reductions are expected in the future with the introduction of 28 nm node silicon. Many company roadmaps show 130 µm copper pillar pitch (50 µm peripheral pitch).
- CSPs are moving toward finer line and spaces (15 µm), to handle fine bump pitch of 140 µm.
- Companies have targets for substrates with 9 µm lines and spaces in 2013. Core layers are fabricated with 12 µm lines and spaces with vias as small as 50 µm and capture pads as small as 110 µm.
- Need improved materials to reduce warpage in thin core materials.
- For 28 nm and below silicon technology, substrate materials will need to have lower coefficient of thermal expansion (CTE), low Z-axis expansion, low dielectric constant (Dk \( \leq 4 \)), and low dissipation factor over a wide frequency band (Df \( \leq 0.01 \)).
- Substrate materials and processes for embedding electronic components.
- On-going develop of leadframe surface treatments and plating process technologies to enhance packaging reliability.
- Low cost solutions for handling thin leadframe CSP strips.
- Improve productivity and throughput of copper bonding wire.
- Wire alloy and metallurgical development to support on-going migration to smaller diameter bonding wire and more complex wiring schemes.
- Mold compounds, liquid encapsulants, and die attach materials with low ionic levels compatible with copper wire bonding.
- Mold compounds with improved reliability and warpage control performance with a balance of fine filler levels at a low cost.
- Good wettability and good reflow level performance of die attach film (DAF) materials.
- Thermally conductive DAF materials.
- Liquid encapsulants formulations with improved flow properties for fine pitch applications.
- Low Tg and high modulus underfill for future ultra low-k devices.
- Formulations, either capillary or pre-applied type, compatible with fine pitch micro bumps.
- No-flow, or “wafer-applied” underfill.
• Solder ball alloys compatible with for smaller diameter balls requirements as pitches shrink from 0.5 to 0.4 and 0.3 mm
• Integrating WLP dielectrics into larger die size and higher I/O applications.
• WLP materials for packaging LED device at the wafer level
• High-end gel, compound and phase-change material (PCM) alternatives for TIM1 needed for microprocessors
• TIM materials compatible with low pressure processing during assembly

In total, the semiconductor packaging materials covered in this investigation are forecasted to grow from $22.2 billion in 2011 on a global basis to $25.0 billion in 2015, excluding thermal interface materials. This represents a compound annual growth rate (CAGR) under 3%. Excluding gold wire, CAGR increases to 5.5%. Thermal interface materials will add $537 million and $692 million in 2011 and 2015, respectively, to the packaging materials market.

The global market for laminate substrates for IC packages is forecasted to experience a compound annual growth rate (CAGR) of almost 8% from 2011 through 2015 on the basis of square meters of materials processed. The growth rate for flip chip CSP laminates will be stronger; 15% CAGR, while wire bond PBGA substrates will decline over the forecast period. The total substrate market, including flex/tape substrates, will reach $9.8 billion in 2011.

Both in units and total revenues, the leadframe market remains a sizeable portion of the total packaging materials market. This market, however, is one of low revenue growth, though leadframe CSP and LED packages will be strong growth areas for units shipped. The market is estimated to be $3.8 billion in 2015.

Higher gold metal pricing has resulted in the increase use of copper bonding wire by both integrated device manufacturers (IDMs) and fabless companies. This transition has strengthened with gold pricing reaching more than $1,700/trz in 2011. As a result, the transition to copper wire is strong, reaching about 22% of wire shipments, and increasingly centered on higher pin count, finer diameter applications. Silver wire is under investigation for LED packaging. Total wire shipments were 20.7 billion meters in 2011 and are forecasted to increase by 7% CAGR through 2011.

Green requirements, low ion containing, and low moisture absorption are a key drivers in mold compound material development. Newer formulations are needed for over molding more complex and larger matrix substrate designs. Total mold compound revenues will be an estimated $1.3 billion in 2011 and are forecasted to approach $1.5 billion by 2015.

The main application for underfill today is flip chip. Selection of the correct flip chip underfill is critical for reliability especially as future devices will be fabricated with ultra low-k materials and continue to use Pb-free bumps. While companies have made progress in eliminating the need for underfill in BGA and CSP packages, Japanese handset and some smart phone makers use underfill. The total underfill market will be an estimated $150.0 million in 2009 and will grow at a CAGR of about 11.6% through 2013.

Liquid encapsulant revenues will be $544 million in 2011 and will increase to $804 million by 2015. LED applications are a strong growth opportunity for these materials.

The die attach film (DAF) market continues to experience strong unit growth, though revenues have weakened with more competition in the market. Die attach materials are being formulated to further improve reliability and to be compatible with thin die applications. The die attach materials market will reach $697 million in 2011 and is estimated to grow to $816 million by 2015.

Solder ball revenues will be $494 million in 2011 and will increase to $864 million by 2015. Higher metal prices have contributed to the average selling price of solders doubling over the past two years. Approximately 90% of solder balls are used for BGAs and CSPs, and 10% for WLPs.

The WLP dielectrics market is forecasted to grow from $68 million in 2011 to $120 million in 2015. Historically, the devices packaged in WLPs were small die sizes with low pin counts (<100), but new product introductions having higher pin counts (up to 500) and 8 mm x 8 mm die sizes (see Table 11.1, page 78) are available.

Thermal interface material (TIM) is needed to manage thermal performance as power density requirements increase in many device applications. The TIM market will be $537 million in 2011 and is forecasted to grow to $692 million by 2013.

Estimated 2011 global market size and key trends in each semiconductor packaging materials segment are summarized in the following Table, on page 4.
# Global Semiconductor Packaging Materials Outlook

- **Sample Only** -

<table>
<thead>
<tr>
<th>Semiconductor Packaging Materials Segment</th>
<th>Estimated 2011 Global Market Size $M</th>
<th>Comments</th>
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</thead>
<tbody>
<tr>
<td><strong>Laminate Substrates</strong></td>
<td>$9,720</td>
<td>Wireless applications migrate from wire bond CSP to flip chip CSP. Coreless structures still in development. IC package substrate production has transitioned from Japan to Taiwan and will slowly expand into China.</td>
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<tr>
<td><strong>Flex Circuit/Tape Substrates</strong></td>
<td>$106</td>
<td>Declining market due to transition to thin rigid laminate.</td>
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<tr>
<td><strong>Leadframes</strong></td>
<td>$3,601</td>
<td>Continued growth in LF CSP and strong growth in LED leadframes. Investments in larger matrix frame designs, new etch capacity, and alternative materials for some discrete, power, and LED applications.</td>
</tr>
<tr>
<td><strong>Bonding Wire</strong></td>
<td>$5,458</td>
<td>With high gold metal pricing, copper wire represents 22% of wire shipped. Silver wire being evaluated, especially in LED applications.</td>
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<tr>
<td><strong>Mold Compounds</strong></td>
<td>$1,349</td>
<td>Improved reliability and warpage control. Improved flow for matrix leadframe and substrate designs. Compatibility with copper bonding wire.</td>
</tr>
<tr>
<td><strong>Underfill Materials</strong></td>
<td>$150</td>
<td>Low stress for low-k and ultra low-k. Lower viscosity materials with wider process windows. No-flow or pre-applied materials. Edge fill used for some WLP and CSP.</td>
</tr>
<tr>
<td><strong>Liquid Encapsulants</strong></td>
<td>$544</td>
<td>Improved reliability formulations for high wire density applications. Increase refractive index and thermal stability for LED.</td>
</tr>
<tr>
<td><strong>Die Attach Materials</strong></td>
<td>$697</td>
<td>Shift in supplier market share for DAF materials. Low cost die attach film for thin chip applications.</td>
</tr>
<tr>
<td><strong>Solder Balls</strong></td>
<td>$494</td>
<td>Lead-free balls a majority shipments. Material development on-going to improve mechanical performance. New suppliers in China.</td>
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<tr>
<td><strong>Wafer Level Package Dielectrics</strong></td>
<td>$68</td>
<td>Many WLP use RDL. Growth in fan-out design for high I/O die. New product introductions higher pin count up to 500 I/O</td>
</tr>
<tr>
<td><strong>Thermal Interface Materials</strong></td>
<td>$537</td>
<td>Growing needs in thermal management from stacked-die packaging to power devices and HBLED. Low viscosity and fast cure materials for thin bondlines.</td>
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</table>

Source: SEMI Industry Research and Statistics and TechSearch International, November 2011