Advancing high performance heterogeneous integration through die stacking

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IBM Demonstrates 3D Chip Technology in Micron Memory Cube

Richard Wilson
Friday 02 December 2011 00:01

IBM has announced that Micron will begin production of a memory device built using its commercial CMOS manufacturing technology to employ through-silicon vias (TSVs).

.equalTo(10,255)

Computerworld

July 15, 2011 - 5:37 A.M.

Apple's A6 processor: 28-nm, 3D IC and made by TSMC

By Jonny Evans

While we wait for Lion, interesting to note the next Apple [AAPL] A6 processor will be made by Taiwan Semiconductor Manufacturing Co. (TSMC) and will be a 3D IC 28-nanometer low-power powerhouse, sweetly tucked inside your iPhones and future model iPads.

Xilinx Says Four Chips Act Like One Giant

By Don Clark

Chip makers have been living by Moore's Law for decades. But that pace of progress is not fast enough for some people, and Xilinx thinks it can help.

Intel co-founder Gordon Moore, in the observation that Silicon Valley residents know by heart, predicted a relentless shrinking of the size and cost of components found on chips. The transistor transistors transistors...
Why Now?

Market: Insatiable Bandwidth

- 64 Exabytes/mo. of IP Traffic
- 34% CAGR

Technology: Cost, IO

- Power density is primary limiting factor for gates and I/O
- SOC’s & platforms: demand highest performance/watt
- 15x drop in I/O-to-logic ratio by 2020
What Does 3D Buy Us?

› Connectivity

› Capacity

› Crossovers
Connectivity
Enables High Bandwidth, Low Power Die-to-Die Communication

100x bandwidth/watt advantage over conventional methods
## Capacity Beyond Moore’s Law

### Big Single Monolithic Die

<table>
<thead>
<tr>
<th>Area</th>
<th>Die Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exponential Dependency</td>
<td></td>
</tr>
<tr>
<td>Linear Dependency (Bali)</td>
<td></td>
</tr>
</tbody>
</table>

### Multiple Small Die Slices

- Greater capacity, faster yield ramp
“Crossover SoCs” with Heterogeneous Die

A crossover is a vehicle built on a car platform and combining, in highly variable degrees, features of a traditional sport utility SUV with features from a passenger vehicle.
CoWoS Process Flow (Courtesy TSMC)

Bottom die
- Stacking (μbump)
  - Wafer Molding
  - Carrier bonding
  - B/S grinding
  - B/S C4 bumping

Top-die
- Transfer glass to tape
- Singulation
- TIS (Stacking, C4)
- TIS (Ring+Lid)
- Build up Subs.
- Thermal Interface Metal (TIM)

Top view
Bottom view
Side view

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OSAT Co(CoS) Process Flow

- Wafer with TSV u-pad/bump, Probe
- Carrier Mount
  - Thin & TSV Reveal
  - UBM & C4-bump
- Carrier De-mount to Film frame
- Dice
- Interposer-on-Substrate
- Package
Virtex-7 2000T: Homogeneous Stacked Silicon Interconnect (SSI) technology

- Virtex-7 2000T – 2 million logic cells
  - ~2,000 BGA balls
  - ~20,000 C4 bumps
  - ~200,000 ubumps
  - ~6.8B transistors
- 4-layer metal Si interposer with TSV
- 4 FPGA sub-die in package
- >10,000 inter-die connections
- Shipping today
Heterogeneous Integration
## What happened to System on a Chip?

<table>
<thead>
<tr>
<th></th>
<th>Logic</th>
<th>Memory</th>
<th>Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global Revenue 2011</td>
<td>$150B</td>
<td>$68B</td>
<td>$45B</td>
</tr>
<tr>
<td>Moore Scaling</td>
<td>Good</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>Technology “Vintage”</td>
<td>2012</td>
<td>2012</td>
<td>2000</td>
</tr>
<tr>
<td>Transistor Characteristics</td>
<td>High performance/ Low leakage</td>
<td>Low leakage/ moderate performance</td>
<td>Stable with good voltage headroom</td>
</tr>
<tr>
<td>Metallization</td>
<td>&gt;9 layers</td>
<td>&lt;5 layers</td>
<td>&lt;6 layers</td>
</tr>
<tr>
<td>Differentiators</td>
<td>High density logic</td>
<td>Charge storage</td>
<td>Passives, Optical</td>
</tr>
</tbody>
</table>
What's the problem with multiple packages?

- The packaging chasm:
  - Two orders difference in package trace/width vs silicon metallization
  - I/O also isn't scaling due to bump pitch and chip to chip loading issues
  - Leads to increased area, power and complexity (SERDES)

To scale in X dimension
Virtex-7 HT: Heterogeneous SerDes

- Yield optimized
- Noise isolation
- 28G process optimized for performance
- FPGA process optimized for power

- 2.8Tb/s ~3X Monolithic
- 16 x 28G Transceivers
- 72 x 13G Transceivers
- 650 GPIO
Virtex-7 H580T – Dual FPGA Slice with 8x28Gb/s Serial Transceivers
Interposer Routing & DCAP

Wire coupling, no shielding

Wire coupling, with shielding

SSN, no DCAP

SSN, with DCAP

Wire Length Histogram

3mm

6mm
SSI Enables Scalable FPGAs

**XC7VH290T**
- Network: 2 x 100G
- GTZ (28G): 8
- GTH (13G): 24
- Logic Cells: 284K

**XC7VH580T**
- Network: 2 x 100G
- GTZ (28G): 8
- GTH (13G): 48
- Logic Cells: 580K

**XC7VH870T**
- Network: 1 x 400G or 4 x 100G
- GTZ (28G): 16
- GTH (13G): 72
- Logic Cells: 876K
High Bandwidth Integrated Memory

- Higher memory bandwidth at lower power: 1Tbps – 2Tbps
- ~1Gb/s per interposer wire
- Simple extension of existing work

Diagram:
- Wired Comms Line Card
- MAC
- Bridging FPGA
- Packet Processing/Traffic Manager
- TCAM
- DDR3
- Bridging FPGA
- Control Plane CPU

Implement in FPGA: [MAC, Bridging FPGA, Packet Processing/Traffic Manager, TCAM, DDR3, Bridging FPGA]
Implement in ASIC/ASSP: [Control Plane CPU]
2nd Generation 3D IC
Co-optimized for Extra Performance, Power and Integration

- **Homogeneous/heterogeneous 3D**
  - 3rd Generation fabric & die architecture
  - Wide memory for high performance buffering

- **2nd Generation 3DIC Interconnect**
  - More than 5x die-to-die interconnect bandwidth
  - Industry standards interface

- **Cutting Edge Functionality**
  - Future XCVR protocol support (56Gb/s)

- **1.5x Integration/BOM**
  - 1.5x Logic (3-4x vs. 28nm monolithic)
3D TSV-on-Active: The Next Frontier

Who’s on top?

High performance chip on top for thermal and TSV process availability

Bottom die supports power TSV’s for top die (Swiss cheese) in older technology (TSV friendly)

Floor-planning critical:
- Thermal concerns (stacked thermal flux)
- TSV keep out zones in bottom die to avoid stress induced performance impact
Challenges

➤ Cost
– Wafer backside processing is complicated
– “Device quality” wafers used for interposers
– KGD methodologies still emerging

➤ Scalability
– Micro-bump scaling is limited
– Super-sized interposers (>30mm x 30mm)
– Improve TSV aspect ratio

➤ Design Support
– Multi-die analysis without Multi-mode Multi-corner explosion
– Thermal modeling based on vertical hotspots
Summary

- Economic and technology forces are aligned to enable 3-D stacking

- The “end game” will see three distinct technologies: Logic, Memory, Analog

- Heterogeneous integration is already here
Thank You

Questions?
400Gb/s Line Card Application

- Up to 16 x 28 Gb/s GTZ Transceivers
- Up to 72 x 13.1 Gb/s GTH Transceivers

Components:
- Virtex-7 HT
- Network Processor
- Fabric Interface
- Packet Queues and Lookup Memory (SRAM, TCAM, DRAM)

Connections:
- 4 x 100G Optical Interface
- Switch Fabric
- CFP2/CFP4 Optical Module