Advancing high performance heterogeneous integration through die stacking

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The First Wave of 3D ICs

IBM Demonstrates 3D Chip Technology in Micron Memory Cube

Richard Wilson
Friday 02 December 2011 00:01

IBM has announced that Micron will begin production of a memory device built using its commercial CMOS manufacturing technology to employ through-silicon vias (TSVs).

COMPUTERWORLD

Apple's A6 processor: 28-nm, 3D IC and made by TSMC

By Jonny Evans

July 15, 2011 - 5:37 A.M.

While we wait for Lion, interesting to note the next Apple [AAPL] A6 processor will be made by Taiwan Semiconductor Manufacturing Co. (TSMC) and will be a 3D IC 28-nanometer low-power powerhouse, sweetly tucked inside your iPhones and future model iPads.
Why Now?

Market: Insatiable Bandwidth

- 64 Exabytes/mo. of IP Traffic
- 34% CAGR

Technology: Cost, IO

- Power density is primary limiting factor: gates and I/O
- SOC’s & platforms: demand highest performance/watt
- 15x drop in I/O-to-logic ratio by 2020

Source: ITRS
What Does 3D Buy Us?

- Connectivity
- Capacity
- Crossovers
Connectivity
Enables High Bandwidth, Low Power Die-to-Die Communication

100x bandwidth/watt advantage over conventional methods
Capacity Beyond Moore’s Law

Big Single Monolithic Die

- Greater capacity, faster yield ramp

Multiple Small Die Slices

- Exponential Dependency
- Linear Dependency (Bali)

Greater capacity, faster yield ramp
“Crossover SoCs” with Heterogeneous Die

A crossover is a vehicle built on a car platform and combining, in highly variable degrees, features of a traditional sport utility SUV with features from a passenger vehicle.
OSAT Co(CoS) Process Flow

1. Wafer with TSV u-pad/bump, Probe
2. Carrier Mount Thin & TSV Reveal UBM & C4-bump
3. Carrier De-mount to Film frame
4. Dice
5. Interposer-on-Substrate
6. Package
Virtex-7 2000T: Homogeneous Stacked Silicon Interconnect (SSI) technology

- Virtex-7 2000T – 2 million logic cells
  - ~2,000 BGA balls
  - ~20,000 C4 bumps
  - ~200,000 ubumps
  - ~6.8B transistors
- 4-layer metal Si interposer with TSV
- 4 FPGA sub-die in package
- >10,000 inter-die connections
- Shipping today
Heterogeneous Integration
What happened to System on a Chip?

<table>
<thead>
<tr>
<th></th>
<th>Logic</th>
<th>Memory</th>
<th>Analog</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global Revenue 2011</td>
<td>$150B</td>
<td>$68B</td>
<td>$45B</td>
</tr>
<tr>
<td>Moore Scaling</td>
<td>Good</td>
<td>Good</td>
<td>Poor</td>
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<tr>
<td>Technology “Vintage”</td>
<td>2012</td>
<td>2012</td>
<td>2000</td>
</tr>
<tr>
<td>Transistor Characteristics</td>
<td>High performance/ Low leakage</td>
<td>Low leakage/ moderate performance</td>
<td>Stable with good voltage headroom</td>
</tr>
<tr>
<td>Metallization</td>
<td>&gt;9 layers</td>
<td>&lt;5 layers</td>
<td>&lt;6 layers</td>
</tr>
<tr>
<td>Differentiators</td>
<td>High density logic</td>
<td>Charge storage</td>
<td>Passives, Optical</td>
</tr>
</tbody>
</table>
What’s the problem with multiple packages?

➤ The packaging chasm:
  - Two orders difference in package trace/width vs silicon metallization
  - I/O also isn’t scaling due to bump pitch and chip to chip loading issues
  - Leads to increased area, power and complexity (SERDES)

To scale in X dimension
Virtex-7 HT: Heterogeneous SerDes

**Top View**
- 28G SerDes
- Fabric Interface
- Passive Interposer
- TSVs

**Cross Section**
- Yield optimized
- Noise isolation
- 28G process optimized for performance
- FPGA process optimized for power

- 2.8Tb/s ~3X Monolithic
- 16 x 28G Transceivers
- 72 x 13G Transceivers
- 650 GPIO

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Virtex-7 H580T – Dual FPGA Slice with 8x28Gb/s Serial Transceivers
Interposer Routing & DCAP

- Wire coupling, no shielding
- Wire coupling, with shielding

SSN, no DCAP
SSN, with DCAP

Wire Length Histogram

3mm
6mm
SSI Enables Scalable FPGAs

**XC7VH290T**
- GTZ-IC
- FPGA
- GTH
- GTH

**XC7VH580T**
- GTZ-IC
- FPGA
- GTH
- GTH

**XC7VH870T**
- GTZ-IC
- FPGA
- GTH
- GTH

**Network**
- 2 x 100G

**GTZ (28G)**
- 8

**GTH (13G)**
- 24

**Logic Cells**
- 284K

**Logic Cells**
- 580K

**Logic Cells**
- 876K

**1 x 400G or 4 x 100G**
- 16

- 72

- 876K

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High Bandwidth Integrated Memory

- Higher memory bandwidth at lower power: 1Tbps – 2Tbps
- ~1Gb/s per interposer wire
- Simple extension of existing work

Diagram:
- MAC
- Bridging FPGA
- Packet Processing/Traffic Manager
- Fabric Interface
- TCAM
- DDR3
- Bridging FPGA
- Control Plane CPU

Wired Comms Line Card

Implement in FPGA
Implement in ASIC/ASSP

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3D: The next frontier

Who’s on top?

- High performance chip on top for thermal and TSV process availability
- Bottom die supports power TSV’s for top die (Swiss cheese) in older technology (TSV friendly)
- Floor-planning critical:
  - Thermal concerns (stacked thermal flux)
  - TSV keep out zones in bottom die to avoid stress induced performance impact
Challenges

Cost
- Wafer backside processing is complicated
- “Device quality” wafers used for interposers
- KGD methodologies still emerging

Scalability
- Micro-bump scaling is limited
- Super-sized interposers (>30mm x 30mm).
- Improve TSV aspect ratio

Design Support
- Multi-die analysis without Multi-mode Multi-corner explosion
- Thermal modeling based on vertical hotspots
Summary

- Economic and technology forces are aligned to enable 3-D stacking

- The “end game” will see three distinct technologies: Logic, Memory, Analog

- Heterogeneous integration is already here
Thank You

Questions?
400Gb/s Line Card Application

- Up to 16 x 28 Gb/s GTZ Transceivers
- Up to 72 x 13.1 Gb/s GTH Transceivers

Diagram showing components:
- Virtex-7 HT
- Network Processor
- Fabric Interface
- Packet Queues and Lookup Memory (SRAM, TCAM, DRAM)
- 4 x 100G Optical Interface
- CFP2/CFP4 Optical Module
- Switch Fabric
- Up to 72 x 13.1 Gb/s GTH Transceivers
- Up to 16 x 28 Gb/s GTZ Transceivers