ST Strategy on 3D Integration LSI

Alexis Farcy, Nicolas Hotellier, Jean Michailos

3D Interconnects
Front-End Manufacturing & Process R&D, Digital Sector
STMicroelectronics

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• ST's competitiveness moving to 3D

• Via Middle Technology
  • Front side and Back side Process
  • Key process steps and challenges

• Electrical characterizations
  • Via Middle impact on electrical parameters & yield
  • Reliability assessment

• Driving Applications
  • Analog / Digital partitioning
  • Memory on application processor
  • Further developments axes

• Conclusion & Perspectives
ST's competitiveness moving to 3D

- Our industry is looking for a **complementary technology** to the traditional 2D SoC or SiP design approach continuing to:
  - **Improve performances**
    (enlarge bandwidth, enhance speed, reduce power consumption)
  - **Enlarge integration**
    (reuse of existing IP, heterogeneous ICs, mixed technologies)
  - **Form Factor**
    (Shrink feature sizes, Product partitioning)
  - **Lower cost**
    (Reduce metal layer, Increase yield, Faster time to Market)

- 3D Interconnects provides another path with relatively **smaller capital investments**.
3D Integration environment

ST’s strength

3D Integration environment

ASSY FLOW

PHYSICAL DESIGN KIT

3D INTEGRATION PLATFORM

LIBRARIES

TECHNO

CAD FLOW

ST's strength

3D integration environment
TSV Wafer Level Camera
A first step in 2.5D integration

VGA module size evolution: from 2002 to 2011

Permanent Glass Handler

Pixel Array
CMOS: 70µm

Glue

TSV feature
• Via last
• Diameter 70µm
• Thickness 70µm

⇒ Form factor as main driver
- Surface gain: 33%
- Thickness gain: 50%
⇒ Mass production in 12”
Via Middle Technology
- Front side and Back side Process
- Key process steps and challenges
Face to Back Via middle TSV integration

1. Standard front end + middle end process
2. Via patterning
3. Via isolation & metallisation
4. CMP
5. BEOL process
6. Cu post process
7. Isolation + RDL + passivation
8. Grinding & TSV recess
9. Carrier bonding
10. Cu pillar
Front-side process major challenges

- **TSV etching**
  - Deep silicon etching (10 to 6μm CD / 80 to 60μm depth)
  - Depth & uniformity control
  - Depth non-uniformity control < 0.7%
  - Smooth sidewall
  - Controlled profile (89~90°)

- **TSV sidewall isolation**
  - Electrical properties, step coverage & cost of ownership

- **Cu diffusion barrier integrity**
  - Material choice, step coverage, barrier efficiency

- **TSV Cu filling**
  - Key challenges → no void + thermo-mechanical stability
  - Cu bath chemistry influence on TSV thermo-mechanical behaviour
  - Process cost of ownership (process duration divided by 4 compared to project beginning)
    - Bottom-up filling strategy
    - Minimum overburden
Front-side process major challenges

- Integration of TSV structures must be transparent with respect to devices parameters and product yield
- ST’s priority: provide an innovative TSV integration scheme
  - Limited impact on standard technology process flow
  - “Portable” to Advanced Technology nodes and FDSOI

• 10µm x 85µm TSV
• 6µm x 55µm TSV
Back-side process major challenges

- **Back-side process** mostly based on CMOS image sensors experience

- **Major novelty linked to carrier temporary bonding & thin wafer de-bonding**
  - Key enabler for process reliability & cost of ownership
  - Multiple solutions available
    - extensive benchmarking done
    - solution validated down to 50µm thick wafers
Via Middle integration on 28nm construction analysis

- Layers integrity validated
- 6*55 µm Cu filling validated
- Minimised impact on BEOL integration
Electrical characterizations
- Via Middle impact on electrical parameters & yield
- Reliability assessment
TSV process impact on product yield

**C065 technology**
Product yield

- **Without TSV**
- **With TSV**

⇒ C065 TSV product yield @ WWS
⇒ No impact of TSV process demonstrated

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**C028-FDSOI technology**
1Mb SRAM yield

- **Without TSV**
- **With TSV**

⇒ C028-FDSOI TSV lots in-line with baseline
Reliability assessment (1/2)

- **Electromigration**
  - Electromigration stress at TSV / M1 interface performed at package level
  - Diffusion and void nucleation at Cu / SiCN capping interface

![SEM (TSV/M1 interface) after electromigration test](image)

125°C - 6.48mA

Time to failure distribution

- Lifetime specification: 10 years
- Lifetime: > 1000 years

- Standard metal interconnects failure mode
- TSV middle lifetime > 1000 years

3D interconnects are not a limiting factor
Reliability assessment (2/2)

- **Kelvin TSV Thermal Cycling**
  - Thermal cycles (-65 C / 120 C / 500 cycles)
  - Both isolated and dense (40µm pitch) Kelvin TSV structures

- **Wide IO daisy chain Thermal Cycling**
  - Thermal cycles (-55 C / 125 C)

  - No extrinsic failure
  - No significant resistance shift

  ![Graphs showing initial TSV electrical resistance and resistance shift after thermal cycling.](image)

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*Continuity test at package level*
Driving applications
- Analog / Digital partitioning
- Memory on application processor
- Further developments axes
Analog / Digital partitioning

- **Analog bottom die with TSV’s**
  - Mature technology node
- **Digital top die**
  - Advanced technology node
- **Interests**
  - Yield on logic die → **cost**
  - IP reuse on Analog die → **time to market**

- **3D Design partitioning, CAD flow validation**
- **ESD protection validation**
- **Similar performances compared to single die product**
- **1000 Thermal Mechanical Cycle (TMC) positive read out**
Memory on Application processor
Breakthrough in power efficiency

- System on Chip co-designed by ST-E / ST / LETI
- SoC key figures
  - 73 mm²
  - 1250 TSV’s & top / bottom interconnections
  - ~1000 flip chip Cu pillars (bottom / BGA)

⇒ Full functionality demonstrated on first assembly lot
⇒ High final test yield
⇒ Performances in-line with JEDEC Wide IO specifications
### 3D Package Assembly

#### Process Flow

- **Top Wafer backgrinding**
- **Top Wafer sawing**
- **Bottom / BGA Assy. - TC or MR**
- **Top / Bottom Assy. - TC**
- **Molding**
- **Ball Attach**
- **Singulation**

#### Components

- **Bottom die**
  - 6.7x5.4mm²
  - Bond pitch 140µm

- **Top die**
  - 8.1x7.9mm²
  - Bond pitch 50µm

- **BGA**
  - 12x12mm²
  - 4L, finishing NiAu
Further development axes

### Passive & Active Interposers
- **Passive interposer**
  - High density interconnects
  - FE/BE compatibility with ULK
  - Smart interposer concept
- **Active interposer**
  - Power management
  - 3D partitioning (Analog/Digital)

### Photonics
- **Photonics / Electronics partitioning**
  - Dedicated photonics on Si
  - Stacked digital die with advanced node for electronics
  - Cost/performance
- **TSV implementation in photonic die**

### 3D Network On Chip
- **Fast asynchronous Network On Chip**
  - High data rate memory interface
  - Network extension to host processing units
- **3D power distribution**
- **IO peripherals in interposer**
Conclusions & perspectives

- 3D design enablers available and demonstrated
  - 2.5D and 3D CAD flows demonstrated
  - I/Os and models available for 3D interconnects

- 3D TSV technology available
  - High yield demonstrated even on 28nm FD-SOI
  - Back-side process & assembly flow available
  - TSV extensive characterisation performed (RF Modeling, impact on MOS, Thermal)

- Multiple opportunities for 2.5 / 3D adoption
  - Passive / Active interposer → high performance / power
  - Memory on Logic → high bandwidth / low consumption
  - Analog / Digital partitioning → time to market / cost
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Thank you for your attention