EV Group

Recent Advances in Thin Wafer Processing and Chip Stacking

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European 3D TSV Summit
Thin wafer processing – Temporary bonding and debonding

Adhesive Uniformity

Edge Alignment

Cost of Ownership

Process Integration

Thin Wafer Handling Post Debond

Device Wafer Front End Processing (Lithography, etching, etc.)

Device Wafer

Release Layer Carrier Wafer

Temporary Bonding

Device Wafer bonded on Carrier Wafer

Back Thinning and further Processing

Device Wafer (thin) on Carrier Wafer

Debonding

Cleaning

Unloading

AC2W Advanced Chip to Wafer Bonding

Device Wafer
Lessons learned - Wafer Edge Alignment
Wafer Edge Alignment Aspects

- Yield: Edge die yield
- Cost: Arcing in plasma chambers
- Cost: Alignment key capture range of steppers
- Cost: Carrier re-usability
  - Avoids metal deposition on carrier
  - Avoids edge seal failures for wet processes

Wafer Edge Alignment Options

1) Mechanical Center-to-Center Alignment: ≤ 30µm (3σ)
2) Optical Alignment: ≤ 10µm (3σ)
### Post-bond TTV Achievements

<table>
<thead>
<tr>
<th>Topography</th>
<th>Interconnect</th>
<th>Application</th>
<th>Adhesive T</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 10µm</td>
<td>Bonding Pads</td>
<td>Die to Die Various</td>
<td>20µm</td>
</tr>
<tr>
<td>~30 to 40µm</td>
<td>Microbumps, Cu-pillars</td>
<td>Die to Die</td>
<td>40-50µm</td>
</tr>
<tr>
<td>~80 to 90µm</td>
<td>Bumps</td>
<td>Die to Substrate Interposer to Substrate</td>
<td>90-100µm</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Bondline</th>
<th>TTV today*</th>
<th>Q1 2013</th>
<th>Q2 2013</th>
<th>Bump last !</th>
</tr>
</thead>
<tbody>
<tr>
<td>20µm</td>
<td>2 µm</td>
<td>1 µm</td>
<td>1 µm</td>
<td>1) TTV, 2) Cost</td>
</tr>
<tr>
<td>50µm</td>
<td>3 µm</td>
<td>2.5 µm</td>
<td>2 µm</td>
<td></td>
</tr>
<tr>
<td>100µm</td>
<td>4.5 µm</td>
<td>4 µm</td>
<td>3 µm</td>
<td></td>
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</tbody>
</table>

* Data achieved with selected adhesives

With 3 mm standard edge exclusion zone.
Lessons learned – Yield management: TTV

Inline TTV inspection
- 100% production inspection
- 80s per 300mm wafer
- Full wafer scan
- 282,000 data points per wafer
Thinned Wafer Post Debond
How to Handle Stress Induced Bow and Warp

Handle it:
- Equipment: Keep thinned wafer flat post debond

Avoid it:
- Mount on film frame before debonding
- Technology: Use permanent bonding / stack at wafer level
- Process: Eliminate stress + Avoid edge defects
How to Handle Stress Induced Bow and Warp

Handle it:
- Equipment: Keep thinned wafer flat post debond
  + Debond and Cleaning Flexibility, + Freedom to Choose Side on Film Frame
  - Min. Die Thickness Limitation 30 ~ 50µm, - Lower Edge Defect Tolerance

Avoid it:
- Mount on film frame before debonding
  + Supports Very Thin Dies (<30µm), + High Tolerance to Edge Defects
  + Insensitive to Stress induced Bow and Warp
  ~ Tape Compatibility (Debond Temperature, Cleaning Solvents)
Comparison of Two Approaches

Thermal Slide-off Release

1. Waferstack
2. Debond Process slide off
3. Cleaning Device Wafer
4. Film Frame Mounting
5. Device Wafer on Film Frame

EVG® ZoneBOND® Process Flow

1. EZR® Edge Zone Release Module
2. Film Frame mounted Wafer Stack
3. EZD® Edge Zone Debond Module
4. Cleaning Module
5. Thinned Wafer on Film Frame
Thermoplastic adhesives

**Main benefits:**
1. Cleanliness

**Max. temperature:** stress dependent

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**Mechanical debonding at room temperature**

**Main benefits:**
1. Room temperature process

**Inherent conflict:**
Wafer stress resembles peel off debonding process

1. Adhesion tailored for debonding
   -\implies\ unwanted delamination

2. Adhesion stronger
   -\implies\ reduced debondability

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**Solution:** ZoneBOND®

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**Today:** Variety of 10-20 temporary adhesives from multiple suppliers
Adhesives for EVG® ZoneBOND® Process Flow

Applications Windows - ZoneBOND ® Adhesives

- DRAM
- Logic
- Si based Power Devices

Bonding Temperature

Maximum Process Temperature Capability
CoO Improvement – New Equipment Introduction

**EVG850 TB**
- 4 Process Modules
- 2 FOUP Load Ports

**EVG850TB XT**
- 9 Process Modules
- 4 FOUP Loading Ports and optional local FOUP storage
Equipment induced CoO has been reduced by >50% with the introduction of the EVG850 XT Frame platform.
Equipment induced CoO vs. Materials Cost

Total CoO reduction is lower unless materials cost is reduced also

→ Open supply chain model
CoO Improvement – New Equipment Introduction

Thinner adhesives enable lower CoO

Thinner adhesives also mean:
• Better TTV → More stable TSV manufacturing process
AC2W Integrated System
Pick-and-place bonder + permanent bonder

**Datacon 8800 Bonder**
- Chip-to-wafer bonding
- High placement accuracy
- High throughput up to 10,000 uph
- Different tacking methods

**EVG540C2W Bonder**
- Permanent bonding on wafer scale
- Programmable position of force
- Compliant Layer for different chip thickness
- About 2-3 Wfr/Hour (for SOLID process)
EVG540C2W Alignment accuracy

Alignment Shift From Collective Bonding After Implementing Tooling and Process Improvements

- Collective bonding shift improved to <2 µm (ave. shift = 0.8 µm)
- No damage to tooling

Misalignment vector map
300mm wafer
1 unit = 1 µm

FIB-SEM Sectional Image