Advances in TSV technologies from the MEMS Perspective

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Chief Technologist, co-founder and VP of R&D

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Silex – The Worlds Largest Pure-Play MEMS Foundry

• **Most Widely Recognized Pure-Play Foundry**
  – No internal product focus
  – Concentrating on MEMS manufacturing capabilities
  – Ideal manufacturing partners to fabless and fab-lite customers

• **Leaders in MEMS foundry services**
  – Independent, full production 6” and 8” Fabs
  – Leadership in turning Idea to prototype, prototype to production
  – Over 300 man-years of MEMS engineering expertise
  – Over 130 employees

• **Broad Customer Base**
  – Over 60 international customers
  – Global sales presence
  – Over 350 MEMS projects successfully executed
  – In 2011-12 worked with 12 of world’s top 30 MEMS companies
Silex has been a leader in enabling innovative MEMS products.

Examples of MEMS devices manufactured at Silex over the years:

- Pressure sensors for measuring blood pressure in coronary arteries
- Microphones for mobile telephones
- Mirrors for optical switching
- Lab-on-chip for DNA analysis

Accelerometers
Gyros
Pressure Sensors
Cantilevers
Touch Membranes
Flow Sensors
Filter Structures
CMOS Interposers
Needles
μBatteries
IR Sensors

Cell/DNA Analysis
Microphones
RF Switches
Lab-on-Chips
Print Heads
Drug Delivery Devices
μMirrors
Optical Benches
Oscillators
Silex’ start was based on its technical capabilities in micro manufacturing devices for in-situ blood pressure sensing.

The company’s rapid growth has been due to its unique skill set and ability to address the micro machining needs for the exploding Sensory Revolution.
MEMS TSV Solutions from SILEX
Sil-Via® and Met-Via®
TSV solutions for the “other” markets

So much focus is put on the high density, state of art FPGA interposer solutions, it is easy to lose sight of the spectrum of mainstream uses for TSV technologies

- TSVs for MEMS Solutions
  - Either through the sealing cap or through the bulk substrate
  - TSV density much lower (1 to 10 TSV/mm²)
  - MEMS die sizes much smaller (mm² vs cm²), i.e. 6” and 8” substrates OK
  - Allow for compact MEMS-ASIC packaging, either wirebond or flip chip
  - Today over 50% of Silex engagements use some type of TSV

- TSVs for LED Interposers
  - 2 to 4 TSVs per interposer
  - TSITM Through Silicon Insulation – chaining of Sil-Via® TSV to achieve electrically isolated die area

- TSVs for MEMS – ASIC interposers
  - Can eliminate organic substrate altogether (all-silicon package)

- TSVs as high density alternative to TMV
  - For Package on Package or FOWLP

- TSVs directly into CMOS: the next frontier
  - Either TSV first or TSV last depending on technology match
  - Because CMOS and TSV need to be integrated, these are custom projects
2006: Silex brings the Sil-Via® all silicon TSV to Market

- Sil-Via® rigid interposer developed in 2003 in response to market need (full wafer thickness TSV)
- First implementation in MEMS microphone interposer substrate – produced for leading cellphone manufacturer
- Volume production started in 2006 ramping to 2,000 6” wafers / month
- Over 6 years in volume production
- Over 50 thousand wafers processed to date
- Over 100 product implementations
Sil-Via® Construction:
single crystal via, high reliability construction

An insulating material fills the via trench.

Via post is formed out of the low-resistivity substrate.

Substrate is single crystal, highly doped silicon.
Sil-Via® TSV combined with poly Vias allowing TSVs and silicon lateral routing

Mirror Design Dual /single axis comb drive:
Alt 1 - Recess etch FS (oxidized comb aniso etch)
Alt 2 - Recess etch BS
Alt 3 – Bonded extra wafer for spacer

R&D program through EU funded EUROSTARS consortium "High Res Sensing" 2011-13
Sil-Via® - TSV for Customer Integration

Examples of products manufactured at Silex:

- Accelerometers*
- Cantilevers
- Cell Analysis
- Drug Delivery
- Electrodes
- Filter structures
- Flow sensors*
- Gyros*
- IC Interposers*
- Lab-on-chips*
- Microphones*
- Mirrors*
- Needles
- Optical Membranes
- Optical Benches*
- Pressure sensors*
- Print heads*
- RF switches
- Resonators*
- Touch Membrane
- µBatteries*
- IR Sensors

* Sil-Via® TSV implemented
2010: Met-Via® Baseline Process Released

- Development began for TSV through-wafer cap as complement to Sil-Via substrate TSV

- XiVIA™ based Met-Cap® Implementation
  - XiVIA™ locking construction ensures high via reliability
  - Integration with getter
  - Hollow via plating allows Tc conformability
  - Hermetic metal bond seal preserves cavity vacuum in case of via crack

*XiVIA™ technology licensed from ÅAC Microtec*
# Sil-Via® vs Met-Via®

<table>
<thead>
<tr>
<th></th>
<th>Sil-Via® (highly doped Si)</th>
<th>Met-Via® (Cu plated via)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Years in Production</strong></td>
<td>&gt;6 years</td>
<td>Approximately 1 year,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MEMS Capping</td>
</tr>
<tr>
<td><strong>Via size</strong></td>
<td>100 µm standard, can go</td>
<td>300 µm is standard,</td>
</tr>
<tr>
<td></td>
<td>down to 50 µm diameter</td>
<td>200 µm available,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>90 (50) µm for 2013</td>
</tr>
<tr>
<td><strong>Wafer Thickness</strong></td>
<td>430 µm is standard, can</td>
<td>300 to 400 µm</td>
</tr>
<tr>
<td></td>
<td>go down to 350 µm</td>
<td></td>
</tr>
<tr>
<td><strong>Reliability</strong></td>
<td>Zero field failures in</td>
<td>85°/85%RH and UHAST</td>
</tr>
<tr>
<td></td>
<td>6 year history</td>
<td>complete; will go through</td>
</tr>
<tr>
<td></td>
<td></td>
<td>full mil/aero testing</td>
</tr>
<tr>
<td><strong>Resistivity</strong></td>
<td>Depends on geometry</td>
<td>&lt;20 mΩ per via</td>
</tr>
<tr>
<td></td>
<td>Typically &lt;1 Ω per via</td>
<td></td>
</tr>
<tr>
<td><strong>Thermal</strong></td>
<td>Perfect matching</td>
<td>Hollow via construction</td>
</tr>
<tr>
<td></td>
<td></td>
<td>buffers Tc differentials</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>Roughly equivalent to SOI</td>
<td>Dependent on via density,</td>
</tr>
<tr>
<td></td>
<td>wafer preparation</td>
<td>RDL requirements</td>
</tr>
<tr>
<td><strong>Availability</strong></td>
<td>6” and 8” wafers</td>
<td>6” (&gt; Met-Via 200)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>and 8” wafers</td>
</tr>
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</table>
Continuous Via Density with All Silex TSVs

- Some via technologies cannot support edge-to-edge via density at the same pitch
- Both Silex’s Sil-Via® TSV and Met-Via® TSVs support edge-to-edge via density at any via diameter
- This is critical for high power, multi-via configurations, as well as shielded via structures for RF (Met-Via only)

Actual Sil-Via® TSV 3D interposer manufactured for a customer, with edge-to-edge via density, High density TSV (200 µm pitch) and Zero-Crosstalk™ features for digital / analogue GND separation

2 layer frontside RDL, 1 layer backside RDL, 400 µm full wafer TSV
Why Rigid Interposers?

• Ability to create TSVs through full wafer thickness means the interposer can be the package
• Rigid interposers best take advantage of existing wafer processing
  – No exotic thin wafer handling
  – Substantial experience in reliable wafer handling at 300-400um
• Eliminating organic substrates improves heat transfer, thermal matching of die to package
• Silicon substrate can be “functionalized”
  – Passive, active elements
  – Through-wafer isolation of entire real estate blocks
Met-Via® Void-Free Underfill for Enhanced Interposer Reliability

Met-Via cavity can be filled void-free with conventional underflow materials with CTE in 7-12 ppm/C range

Image courtesy Fraunhofer-IZM
Above is metalized test samples from Silex Met-Via Interposer (TSV: 250 µm diam and 600 -1500 µm pitch)
Using 305 µm thick substrates (3.2 x 5.6 mm Interposer die size with 3 x 6 TSVs)
The hollow features of Met-Via® TSVs can be filled void-free with conventional underflow materials with CTE in 7-12 ppm/C range.
Proven to work with FgH-IZMs compression molding process

Image courtesy FgH-IZM (CAJAL4EU):
Areas of Recent Development
Test structure showing both Met-Via 90 and Met-Via 50 Daisy chain structures

90 µm via diameter
240 µm pitch
(16 TSV / mm²)

50 µm via diameter
150 µm pitch
(36 TSV / mm²)
Backside of wafer showing Met-Via 90 collar after Cu via plating (8x8 TSV array)

Silicon removed to visualize copper TSV and BS collar structures

Collar has diameter of 190 µm and spacing of 50 µm
Met-Via® after removed silicon visualizing Daisy chains for TSV testing
Seed layer deposition of high AR full wafer thickness vias is the current area of R&D focus.
> 1000 dies out of 1200 (on 8” wafers) shows via resistance below 20 mOhm
28°C temp increase means 1,720 +/- 650 (1 sigma) µohm increase,
Nominal Via resistance = 14 mOhm => TCR = 0.44 % / deg C
Capacitance to substrate and metal ground: 24 pF for 350 µm Via diameter in 380 µm thick substrates.

The artifact along wafer edge is due to overplated BS via collars shortening the sealing ring.

Every 2nd row has BS routing (Daisy TSV chains).
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</thead>
<tbody>
<tr>
<td>Met-Via 200+</td>
<td>12-24</td>
<td>350-400</td>
<td>355</td>
<td>380</td>
<td>500</td>
<td>&lt; 3</td>
</tr>
<tr>
<td>Met-Via 90</td>
<td>10-20</td>
<td>90</td>
<td>280</td>
<td>305</td>
<td>240</td>
<td>16</td>
</tr>
<tr>
<td>Met-Via 50</td>
<td>8-16</td>
<td>50</td>
<td>280</td>
<td>305</td>
<td>150</td>
<td>36</td>
</tr>
</tbody>
</table>

![Met-Via Diagram](image)

- **a**: Si Oxide (Optional low-k)  
- **b**: Barrier  
- **c**: Si  
- **d**: Backside Via Depth  
- **p**: Minimum Via Pitch  
- **t**: Wafer Thickness
SEM of Met-Via® 50 full wafer via etch (305µm)

Done at 150 µm pitch (currently scheduled for 2H 2013 availability)

DRI etched XiVIA™ feature variants

Met-Via® uses XiVia™ technology licensed from ÅAC Microtec.
Functional Capping can provide higher value than CMOS-MEMS Packaging alone.

High levels of functionality can be integrated into the interposer or CMOS wafer cap, creating new categories of heterogeneous devices.
Met-Via® 3D Inductors

Mag core inductors using Met-Via for winding

Magnetic core (Fe Ni Co alloy)

Met-Via

High Resistivity Silicon
The Future: Silex TSV Technologies can be applied to CMOS wafers for **True Heterogenous Integration**

- MEMS / CMOS on separated wafers that are bonded together
- Increased I/O density with reduced foot print (die cost)
- TSV integration of both MEMS and CMOS*
- Large inertial mass in mono-Si => better resonance performance
- Rigid wafer for ease of packaging handling
- Long term high vacuum reliability

*CMOS TSV integration needs process integration at the CMOS process level. Contact Silex to initiate a feasibility study on this emerging technology.*
Acknowledgments

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Thank you for your time.

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