3D Component Packaging in Organic Substrate

Mark Beesley
Beyond 300mm, Grenoble – April 2012
A range of topics discussing substrate panelisation and drivers from a series producer of Embedded Component Substrates
„Large and larger format“ packaging concepts

**Moulded Component**
Single-sided fanout

**Embedded Component**
Double-sided fanout

Minimum Semiconductor footprint through DESIGN RULE

Minimum SYSTEM footprint through STACKING
Embedding uses the space within an organic substrate for active and passive components.

Focus < 100 embedded connections
Roadmap < 400 embedded connections

AT&S is amongst the leading chip embedding providers – others in Europe; Japan; Korea; Taiwan.
ECP® Advantages

- Footprint reduction (Miniaturisation)
- Integration (Ease of Use)
- Reliability
- Performance
Why SoC? Why WLP? Why Embedded Die?

Rapid Product Lifecycle kills SoC for smartphone

- Standard PCB
- High end Semiconductor on Interposer

Discrete component packages. Supply chain flexibility but PCB interconnect density at maximum and complex BoM management

OEM Decision on Engine concept

Scenario #1
Integrated packaging + Anylayer = Overall form factor reduction

Scenario #2
Integrated packaging + Standard PCB = Reduced cost; reduced ramp risk

3D Component Packaging in Organic Substrate | Mark Beesley, AT&S
## Embedding: Positioning and market segmentation

### Market Segmentation

<table>
<thead>
<tr>
<th>Device</th>
<th>Market 2012 [Bn. Units]</th>
<th>Applications</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt; 400 Pins</td>
<td>18.8(^1)</td>
<td>• Application processor</td>
<td>• Substrate</td>
</tr>
<tr>
<td>– 400 Pins</td>
<td>14.5(^2)</td>
<td>• Baseband processor, Memory</td>
<td>• Hybrid (FOWLP, BGA,...)</td>
</tr>
<tr>
<td>&lt; 100 Pins</td>
<td></td>
<td>• RF, Audio, Video, MEMS, Sensor, Power Mgmt.</td>
<td>• Embedded die – FOCUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Resistor, capacitor, diode</td>
<td>• Wafer Level Package (WLP)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Embedded and SMT discrete</td>
</tr>
</tbody>
</table>

### Target-market characteristic
- Large Markets
- Trend for Miniaturization
- Fastest growing

### Target markets
- Prio 1: Smartphones
- Prio 2: Medical Devices
- Prio 3: Automotive

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The overall embedding market will count for approx. 500 Mio. US$ in 2015.

Source: Yole (2010)
Smartphone/Tablet Projections

Smartphone/Tablet unit Sales (mio units)

Source: Bank of America / Merril Lynch
GSF Shanghai 2012

Ramp of non-Apple/Samsung driven by China and 100-dollar-smartphone

<table>
<thead>
<tr>
<th>Year</th>
<th>Non Apple/Samsung</th>
<th>Apple + Samsung</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008</td>
<td>135</td>
<td>15</td>
</tr>
<tr>
<td>2009</td>
<td>142</td>
<td>31</td>
</tr>
<tr>
<td>2010</td>
<td>232</td>
<td>88</td>
</tr>
<tr>
<td>2011 (E)</td>
<td>305</td>
<td>229</td>
</tr>
<tr>
<td>2012 (E)</td>
<td>405</td>
<td>346</td>
</tr>
<tr>
<td>2013 (E)</td>
<td>542</td>
<td>431</td>
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</table>
Position in the value chain

**Market drivers**

<table>
<thead>
<tr>
<th>#</th>
<th>Market driver</th>
<th>Driven by</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Roadmaps</td>
<td>Moore’s Law, Semicon, OEM</td>
<td>Boundaries are the same for everyone</td>
</tr>
<tr>
<td>2</td>
<td>Time to market</td>
<td>OEMs</td>
<td>Depends on market segment</td>
</tr>
<tr>
<td>3</td>
<td>Product vision</td>
<td>OEMs</td>
<td>Product strategy, Costs, …</td>
</tr>
</tbody>
</table>

**OEM’s Value chain**

1. Roadmaps
2. Time to market
3. Product vision

- Semicon (24+ months)
- Pkg Design (18 months)
- Substrate (15 months)
- Pkg Ass’y (12 months)
- Test (6 months)
- PCB (3 months)
- EMS (4 weeks)
- Distribution (Ramp)

**Product Lifecycle**

**Embedded Substrate** – Disruptive technology from PCB

- OEM advantage
- Embedded PCB

Timeline
USP: Embedded packaging = merger of worlds

Embedded Component

- PCB
- Pick & Place
- Epoxy
- Embedded Package

+ Large format substrate + High speed assembly + Mass production die adhesion = Value add
Semi-additive technology – single board processing

- Stacked copper filled via
- Roadmap 10µm line
- Handling of ultra-thin panels
- Full traceability of process data
- Single piece flow for improved
  - Flexibility
  - Risk management
Component Assembly – SMT World

- High speed component placement
- Large production formats
- Fully flexible equipment
- Accuracy to 10µm true position

- Ability to integrate different component types in one package

- Highly competitive against alternative methods …
As complexity evolves – yield must be maintained at close to 100% due to device impact on cost of scrap

<table>
<thead>
<tr>
<th>Design Rule</th>
<th>When</th>
<th>Volume</th>
<th>Line / space (µm)</th>
<th>Component pad (µm)</th>
<th>Minimum pitch (µm)</th>
<th>Comp to Comp (µm)</th>
<th>ECP® Core thickness over Cu (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>NOW</td>
<td>Series</td>
<td>50 / 50</td>
<td>200</td>
<td>250</td>
<td>200</td>
<td>250</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre-series</td>
<td>25 / 25</td>
<td>150</td>
<td>175</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>V2</td>
<td>Industrialisation</td>
<td>Series</td>
<td>25 / 25</td>
<td>150</td>
<td>175</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre-series</td>
<td>20 / 20</td>
<td>130</td>
<td>150</td>
<td>200</td>
<td>160</td>
</tr>
<tr>
<td>V2.1</td>
<td>Development</td>
<td>Series</td>
<td>20 / 20</td>
<td>130</td>
<td>150</td>
<td>100</td>
<td>160</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre-series</td>
<td>15 / 15</td>
<td>110</td>
<td>125</td>
<td>100</td>
<td>130</td>
</tr>
<tr>
<td>V3</td>
<td>Research</td>
<td>Series</td>
<td>15 / 15</td>
<td>110</td>
<td>125</td>
<td>100</td>
<td>130</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre-series</td>
<td>10 / 10</td>
<td>90</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>V4</td>
<td>Research</td>
<td>Series</td>
<td>10 / 10</td>
<td>90</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pre-series</td>
<td>&lt; 10 / 10</td>
<td>&lt; 75</td>
<td>&lt; 85</td>
<td>&lt; 75</td>
<td>&lt; 75</td>
</tr>
</tbody>
</table>
Supply Chain

Wafer → Wafer Level Processing → Embedded Component → Package Assembly → Test

- Array Distribution
- WLP simplification
- Format optimisation
- Design optimisation
- Step up of formats
- Large format package assembly
- Step testing
Largest EU funded project focussed on INDUSTRIALISATION – AT&S consortium leader; 11 partners – driving Embedded Component technology
Show me the bunny! (suit)
A tongue-in-cheek comparison of Laminate embedding with „conventional“ packaging
Class 10k at AT&S vs. Class 10 at OSAT
1 SiPlace X2 chip shooter has capacity of 20 die placers
Pick and Place vs. Die Placer

1 SiPlace X4 chip shooter equivalent to 4 X2 chip shooters
1 X4 chip shooter equivalent to 80 die placers ...
1 laser drilling station equivalent to 100 wirebonders …
PCB Panel sizes

42“x48“ full laminate sheet

Yields 4 x 21“x24“ @ 100% efficiency

36“x48“ full laminate sheet

Yields 4 x 18“x24“ @ 100% efficiency
18 “ x 24 “

1 panel equivalent to 3.8 reconstructed 300-mm wafers…
1 Next Gen panel equivalent to 4.5 reconstructed 300-mm wafers!
Embedded component uses large production formats compared to other packaging techniques.

Base materials are typically glass reinforced epoxy resins (FR4) as used in high density PCB manufacturing, or BT resins as used in IC Substrate.

Panel size

- **Panel Pkg Gen 2**
  - 21” x 24” panel
  - ~ 504sqin

- **Panel Pkg**
  - 18” x 24” panel
  - ~ 432sqin

- **Panel Pkg**
  - 18” wafer
  - ~ 254sqin

- **8” wafer**
  - ~ 113sqin

- **12” wafer**
  - ~ 50sqin

- **6” wafer**
  - ~ 28sqin

- **8” strip**
  - ~ 24sqin

- **18” wafer**
  - ~ 254sqin

Shown approximately to scale

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<table>
<thead>
<tr>
<th>Application</th>
<th>Package Size</th>
<th>X,Y Reduction</th>
<th>Package concept</th>
<th>Embedded Component advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Convertor</td>
<td>7mm²</td>
<td>40%</td>
<td></td>
<td>Smallest footprint 600mA DC DC convertor on the Market</td>
</tr>
<tr>
<td>Charge Management</td>
<td>20mm²</td>
<td>40%</td>
<td></td>
<td>Stacked silicon package for advanced Li-ion battery charge management</td>
</tr>
<tr>
<td>High Def Media</td>
<td>20mm²</td>
<td>30%</td>
<td></td>
<td>Integrated module – discrete passives stacked on eWLP</td>
</tr>
<tr>
<td>MEMS integration</td>
<td>5mm²</td>
<td>&gt; 50%</td>
<td></td>
<td>Superior performance MEMS applications with smallest form factor</td>
</tr>
<tr>
<td>Mobile TV</td>
<td>20mm²</td>
<td>50%</td>
<td></td>
<td>Single device solution for mobile tuner</td>
</tr>
<tr>
<td>Identification</td>
<td>60mm²</td>
<td>New feature</td>
<td></td>
<td>Integrated biometric sensing</td>
</tr>
<tr>
<td>Sensorics</td>
<td>60mm²</td>
<td>50%</td>
<td></td>
<td>Die flipped in package to direct active sensor to object – position; temperature</td>
</tr>
<tr>
<td>Wireless</td>
<td>20mm²</td>
<td>40%</td>
<td></td>
<td>Stacked package for smallest footprint solution</td>
</tr>
</tbody>
</table>
Embedded Component = Dramatic Package form factor reduction - up to 50% - for SiP < 400 embedded connections

Other benefits - performance; reliability; integration

Capacity ramping, leveraging existing technologies (WLP; SMT; PCB etc)

Design automation available from mainstream providers

Supply chain is optimising – double digit million embedded SiPs in the field

AT&S ramping up the world’s leading chip embedding technology, ECP® ...
About AT&S

- Worldwide Sales Network with offices in Europe, Asia and America
- Seven high tech production facilities – world leader in innovation and high end interconnect technology
- More than 7,500 employees, around 670Mio USD turnover in 2010/11
- Dedicated Production facility for Embedded Component Packaging in Leoben, Austria
Thank you for your attention!

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