Packaging Challenges for High Performance Mixed Signal Products

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NXP Semiconductors: HPMS solutions


These innovations are used in a wide range of automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing applications.

A global semiconductor company with operations in more than 25 countries, 28000 people, > 3000 engineers
High Performance Mixed Signal

- The world is analog in nature
- HPMS refers to advantages gained by processing a mix of analog and digital signals
- Effective handling of real world signals
- It requires optimized fab processes as well as packaging technologies
- Resulting in the highest product performances
Innovations used in a wide range of applications

**Wireless infra**
- Wireless base stations
- Point-to-point
- CATV infrastructure
- Broadcasting

**Lighting**
- Lighting drivers (CFL, LED)
- Lighting networks
- Backlighting

**Industrial**
- Smart grid
- White goods
- Home / building automation
- Power supplies

**Mobile**
- Mobile devices
- Portable power supplies
- Personal health
- Chargers
Innovations used in a wide range of applications

- **Automotive**
  - In-vehicle networking
  - Car access & immobilizers
  - Car entertainment
  - Solid State Lighting
  - Telematics
  - Speed & Angular Sensors

- **Identification**
  - Secure identity
  - Secure transactions
  - Tagging & authentication

- **Consumer**
  - TV
  - Satellite, Cable, Terrestrial and IP set-top boxes
  - Satellite outdoor units

- **Computing**
  - Tablet PCs
  - Note- / Netbooks
  - Desktops
  - Power supplies, Monitors and peripherals
High Performance Mixed Signal Solutions

Key differentiators
- Power efficiency
- Cost efficiency
- Functional performance
- Miniaturisation
- Quality

It is combining expertise in
- Application
- Circuit design
- Process technology
- Packaging technology
Package Landscape over Time

- Package size reduces about 1.5 to 2 times slower than semiconductor technology (Moore’s law).
- The relative packaging cost is increasing; packaging costs are in HPMS applications about half the total product costs.
‘Unit Cost Perspective’ is the sum of package cost reduction and package concept evolution.

The challenges:
- **Switch to new technology in time**
- **Continuous assembly platform cost saving**
Assembly Technology Drivers

- Form Factor / Miniaturization
- Performance
- Functional Integration
- Cost Reduction

Above items seem to conflict, but by good optimization of technologies, they get aligned and strengthening each other

**Platform based approach:**
- Cost
- Flexibility
- TTM
RF Performance and Miniaturization

- Mobile business drives size reduction
- Wire bonding has limits wrt RF performance
- Going from leaded packages to leadless (wire bonded)
- Going from Wire bond to WLCSP
- Board level requirements demand larger pitch, so: fan-out
- Main challenges
  - Size: 0.7x1.1 mm → 0.4x0.6 mm
  - Volume manufacturing / cost
Supporting Manufacturing Technology

- For small dies saw lane area is very significant
  - E.g. RFID <0.2mm² die size, 8 inch wafer: 30% of wafer area is saw lane

- Stealth laser sawing enables 15 µm wide saw lanes: 25% more dies per wafer
  - Drop in PCM/OCM need to be used

Old 60/80 µm saw lane design
New 15/15 µm saw lane design
New 15/15 µm saw lane design after singulation
Power and High Frequency

- RF high-power devices: balance between cost and performance
- Ceramic packages with CPC headers towards overmolded packages base on Cu headers
- Technical challenges
  - 50um thick dice
  - Combi with wafer backside metals / solder (AuSi or AuSn)
  - CPC to Cu headers
  - Thermal performance
Cost and Miniaturization

- Diamond package
  - Size 0.8 x 0.8 x 0.35 mm
  - Smallest body size in the world for 5 IOs at 0.5 mm pitch
  - Allows easy board assembly
RF Performance and Miniaturization

- Fan-out Wafer Level Package:
  - Extension of WLCSP platform
  - WLCSP bumping infrastructure used →
    interconnects by plated/sputtered trace
    - Excellent electrical performance
  - Technology competing with FCCSP, performance driven
  - Targeted for medium pin count
  - 3D packages under development – any array patterns on the top
Performance and Miniaturization

- Substrate embedded packages
  - Alternative for fanoutWLCSP
  - Mechanically more robust package compared to WLCSP
  - Low ohmic interconnects (no wire-bonds)
  - Easy design for vertical devices
  - Easy design for modules

- Concerns
  - Business model and logistics flow
  - Liability: Follow package subcon model with singulation and final test in-house
  - No standardization yet, different suppliers use different technologies
  - Reliability in case of a-symmetrical build ups
  - Yield, especially in case of multiple die or large I/O dies
Quality, System Integration and Cost

- Automotive sensor
  - Design simplification and standardization
  - Full system integration: 3 caps, 2 ASICs, 2 MR dies
  - Build-in redundancy
  - High temperature capability
    - Molding compound development for 150-200 °C
FE/BE Interaction

- Brittle LowK material in advanced CMOS can be easily damaged by packaging steps:
  - Testing, wire-bonding (esp. Cu wire), and dicing are critical
  - Robust bond pad stacks and saw lane design needed

- Different package types exert different stress levels on the die
  - Stiff packages and packages with asymmetric build-up are most critical
WLCSP, FE-BE Interaction

WLCSP quality is a trade-off between FE-BE decoupling, BLR and costs.
WLCSP Robustness Improvement

- **FE process**
  - Planarization in wafer fab process
  - Robust passivation layer

- **Design:**
  - “Planarization in design”: use large bondpads

- **Bump construction**
  - Thick, compliant UBM
  - Stress decoupling layer(s)
  - Compliant solder ball material

- Each new FE/BE combination is to be assessed separately

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Early drop test fail for not planarized FE process
Sustainability

- **Green** RoHs: elimination of Pb in electronics per July 1st 2006
  - Implementation of Pb-free termination finishes
  - Compensation of MSL level increase due to higher Pb-free reflow temperature
  - Co-operation between Philips Semiconductors, IFX, ST and later also FSL (E3/E4)

- **Dark Green** NXP converted to halogen-free and antimony oxide-free substrates and molding compounds in 2010
  - Packages are more resistant to moisture, no dry-packing needed
  - More expensive
  - Dark green is the standard for all new developments

- RoHS and ELV directives still exempt use of Pb inside packages
  - Revision of exemptions is planned in 2014
  - Until legislation change: Pb-free is a selling feature
  - Co-operation between: NXP, FSL, IFX, Bosch, ST on lead-free D/A (DA5)
    - Effort to convince EU NOT to ban Pb-holding D/A to avoid large effort and cost
    - Find Pb-free alternative
Conclusions

- HPMS products require dedicated packaging solutions
  - Market drives to ultimate miniaturization
  - Miniaturization also is cost enabler for HPMS products
  - Flip chip or plated interconnect to realize high electrical performance
  - HPMS products requirements drive high temperature packaging performance

- HPMS solutions require even stronger co-operation between FE and BE