Packaging - Enabler for Integration in Mobile Applications

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- Summary
Intel Mobile and Communications Group

MCG (Mobile and Communications Group) is a business group of Intel Corporation.
MCG develops and markets innovative semiconductor products and solutions for
mobiles, tablets and emerging devices.
MCG products comprise:
  • Application Processors
  • Mobile platform solutions for all market segments from ultra low cost phones to
    advanced smart phones and tablets. → Basebands, Modems, PMU, 2G, 3G, LTE
  • Connectivity as Wi-Fi, BT, GPS

Trend to Mobile Devices

PCs shipped
2002: 1 bn
2007: 2 bn
Today: ~3.5 bn

PCs installed
1.5 billion installed PCs today (2 bn in 2015)

Mobile Phones
~6 bn mobile phone subscriptions worldwide at the end of 2011

IDC predictions

PC = desktop, notebook & server
Device Market Opportunity

In the 2012-16 period, there will be shipments of:

- ~9 billion Phones (of which, 4.6 billion smartphones)
- 300+ million ‘Cellular’ Tablets
- 400+ million M2M modules
- 1+ billion USB dongles and other consumer electronics with cellular connectivity

~11 Billion Unit Opportunity in 2012-2016
Mobile Evolution

- **1970**: Brick Phone
- **1980**: Candy Bar
- **1990**: Feature Phone
- **2000**: Smart Phone
- **2010**: Touch Phone

**Brick Phone**
- GSM, CDMA, TDMA, iDEN
- Small size
- SMS service

**Candy Bar**
- GSM, CDMA, TDMA, iDEN
- Small size
- SMS service

**Feature Phone**
- GPRS, HSCSD
- Data capable
- Camera & MMS
- Mass adoption

**Smart Phone**
- GPRS, HSPDA, Wi-Fi
- Emails driver
- Gadget

**Touch Phone**
- GPRS, HSPDA, EVDO, Wi-Fi, LTE
- Sensors, MEMS
- Media Platform
- All about web…
Moore’s Law Scaling can not maintain the pace of progress

In the past: scaling geometries enabled improved performance, less power, smaller size, and lower cost.

Today: scaling alone does not ensure improvement of performance, power, size and cost.

The primary mechanism to deliver “More than Moore” will come from integration of multiple circuit types through SoC and SiP.

SiP will allow the efficient use of three dimensions through innovation in packaging technology.
Mobile Application Package

Trends

- Package down-sizing
- Higher substrate utilization
- Better electrical performance

- Wafer Level BGA
  - Down-sizing potential
  - Better thermal and electrical performance
  - Cost reduction potential
  - Minimum SiP cost adder

- Flip Chip BGA
  - Performance (f2f)
  - Stacking
  - Passives embedding

- Wire Bond BGA

- Embedded Die
eWLB (embedded Wafer Level Package)

⇒ More than 1 Billion components sold
System Integration

“System integration brings together components into one system and is ensuring that the components function together as a system”

Important:

⇒ Co-Design … for the design optimization of the system

Integration by:

⇒ Side-by-side SiP
⇒ Stacking
  ⇒ Embedded Package Technologies … inherent stacking possibility
  ⇒ Package on Package (PoP) stacking … test and burn-in capability and external supply
  ⇒ 2.5D Interposer Stacking … half way to stacking
  ⇒ Die stacking (actives, passives) … the hype
⇒ Modules … high integration
Many technologies (& libraries) within one project:
- different silicon tech’s – substrate / RDL – PCB – other components
- Multiple length scales
  - cm ⇒ PCB, mm ⇒ Substrate, μm ⇒ chip, sub-μm ⇒ chip devices
- Strong interdependencies between dies, package, testing & application board
- independent optimization at different levels cannot lead to optimum system
- Global design optimization required (chips – package – board/system)
  ⇒ higher performance, reduced cost, better quality
## System Integration

### Package Technology

<table>
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<tr>
<th>Structure</th>
<th>Example</th>
<th>eWLB based example</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Side-by-Side Structure</strong></td>
<td><img src="image" alt="Diagram" /></td>
<td><img src="image" alt="Diagram" /></td>
</tr>
<tr>
<td>Wire bonded</td>
<td>Flip Chip</td>
<td></td>
</tr>
<tr>
<td><strong>Stacked Structure</strong></td>
<td><img src="image" alt="Diagram" /></td>
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<tr>
<td>With Interposer</td>
<td>Wire bonded</td>
<td>Wired Bonding and Flip Chip</td>
</tr>
<tr>
<td>PoP, Flip Chip type</td>
<td>Through Silicon Via</td>
<td></td>
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[www.itrs.net](http://www.itrs.net)
Side-by-Side SiP

- Typically wire bonding or flip-chip bonding technology has been used
- easy to realize in eWLB
  - enable pick and place for several die types
  - ensure mold filling between dies
  - control die shifts, warpage of recon wafer
- Enable higher data transfer rate between dies on module
- Short interconnect line length targeted
- Bringing dies close together is the key
- Larger package size compared to stacking

Two-die multi-chip eWLB
Embedded Die

- Inherent stacking capability as alternative to side by side. Enabler is basic PCB-technology providing vias and 2 side metallization.
- developed by a wide range of companies for several years
- high potential for integration / miniaturization
- Challenges:
  -- min chip pad pitch = 175µm (typically)
  -- supply chain: OSAT + PCB-manufacturer

- Example: DC/DC converter:
  - DC/DC converter embedded in substrate
  - Passive SMD components mounted onto substrate
  - Size benefit due to face-down mounting of converter
Stacking

Why Stacking?

- **Higher electrical Performance**
  Shorter and less interconnects, lower parasitics, higher bandwidth

- **Smaller Form Factor**
  Small lateral dimensions, low package height, higher density

- **Heterogeneous integration**
  Integration of different functional layers (RF, memory, logic, MEMS, …) based on different optimized process nodes

- **Shorter Time-to-Market**
  Capability to partitioning, reusable (die-level) building blocks

- **Lower Development, Tooling and Unit Costs**
  In high volume production

- **Die-Level Modularity Reduces Risk**
  Modularity reduces the risk of failure.
Traditional Stacking

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<th>3D-TSV Stack</th>
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<td>Flip Chip &amp; Wire Bond</td>
<td>Package on Package</td>
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<td>vertical integration</td>
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- Stacking of multiple chips into one package
- Realization of interconnects typically by flip chip or wire bond

**Advantages:**
- Reduced package height/ dimensions
- Known processes, high yield

**Disadvantages:**
- Electrical performance
- Capability for future technology nodes
PoP Stacking

Stacking of multiple (possibly different kinds of) packages onto each other

**Advantages:**
- Both packages can be tested and burned before assembly
- Interfaces standardized

**Disadvantages:**
- Dimensions
- Electrical performance

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Peripheral BGA balls interconnecting top and bottom package
BGA balls connection to motherboard (desoldered)
Top package
Bottom package

iPhone's ARM processor (Flip Chip, bottom package) & DRAM package (Wire Bond, top package)
PoP Stacking:

- eWLB standard flow with TMV connections
- Lowest package profile with but with only peripheral interconnects

eWLB based TMV PoP

Height reduction is key...

 Courtesy of STATSChipPAC
PoP Stacking: ePoP

- ePoP: embedded Package on Package
- eWLB flow with two sided redistribution (RDL)
- Multiple possibilities for connection in z-direction: TMV, TSV, pre-fabricated via bars (PCB, Si)
- Area array interconnects on ePoP package backside
- Low package height
- Good electrical performance due to short interconnects
- Large package sizes remain a challenge for board level reliability (without underfill)
### 2.5D Interposer Stacking

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#### Side-by-side placement of multiple dies possible

#### Advantages:
- Si-Interposer technology allows use of very fine pitch dies and integration of thin-film passives
- Expansion-matching

#### Trade-Off:
- Cost of Si-interposer with TSVs and multiple RDLs
- Lateral size of multi-chip-package
2.5D Interposer Stacking
Performance driven Example

Example of Performance-Driven 2.5D Integration
GPU for gaming

- The Sony PS4 (to be released for the 2013 holiday season, or in 2014) will have a GPU interposer with a 512-wide data bus and an interposer memory
- Will probably be an AMD chip
- Future gaming platforms will offer 3D imagery, which requires fast & high bandwidth computing power
- 2.5D is unanimously praised as the ideal solution for this purpose
- “GPU-RAM Bandwidth is the key factor for rendering performance” – Sept 2011 -- Teiji Yutaka, SVP Technology Platform, Sony Computer Entertainment

Interposers Expected Applications Production Roadmap

- CPUs
- APEs (smartphones)
- CMOS image sensors
- APEs (in tablets)
- GPUs
- FPGAs, networking, & storage & HDTV ASICs
- LED silicon substrates
- BAW filters, RF devices

An interposer module for (Yole’s assumption) an AMD GPU demonstrator
Courtesy of Global Foundries, 2012
**2.5D-Interposer-Stacking: eWLB Alternative**

**Possible Solution for Low End...**

**Approach FC-eWLB:**

2.5D-interposer replacement by eWLB (for redistributing the extreme fine pitch to std. Flip-Chip-pitch) and a standard Flip Chip assembly.

**Leading to a ...**

**Std. Flip Chip** approach with

- High reliability *(FC comparable)*
- Lower package height
- Lower cost
- Higher yield
- Existing packaging infrastructure *(OSATs)*
# 3D TSV-Stacking

## Advantages:
- Performance
- Dimensions

## Disadvantages:
- Cost
- Maturity

Stacking of multiple chips into each other with shortest interconnect through the chips (TSV)

### Samsung 16Gb NAND stack with TSV

Source: Internet

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## Traditional Stacking

- Flip Chip & Wire Bond

## PoP

- Package on Package

## 2.5D Interposer

- side-by-side integration

## 3D-TSV Stack

- vertical integration
3D TSV-Stacking:
Wide I/O DRAM: A first adoption possibility of TSV...

- Wide I/O DRAM offers twice the bandwidth of LPDDR2 for the same power
- 1200 standardized interconnects to the memory chip
- Usage in high performance smartphones first
- Likely the first TSV application to come with Logic

Source: S. Dumas, Mobile Memory Forum, June 2011
# 3D TSV Stacking

Applications Status, Drivers and Barriers

<table>
<thead>
<tr>
<th>Application</th>
<th>Driver</th>
<th>Status</th>
<th>Barrier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image Sensors</td>
<td>Performance, form factor</td>
<td>Production</td>
<td>None</td>
</tr>
<tr>
<td>CPUs &amp; memory</td>
<td>Performance</td>
<td>16nm silicon and beyond</td>
<td>Cost, process, yield, infrastructure</td>
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<td>Performance</td>
<td>2014</td>
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<tr>
<td>FPGAs</td>
<td>Performance</td>
<td>2014</td>
<td>Cost, process, yield, infrastructure</td>
</tr>
<tr>
<td>Wide I/O memory with Logic</td>
<td>Performance (bandwidth, lower power consumption)</td>
<td>2012-2013</td>
<td>Cost, process, yield, KGD, infrastructure</td>
</tr>
<tr>
<td>Memory (stacked)</td>
<td>Performance, form factor (z)</td>
<td>(2012) 2013</td>
<td>Cost, process, yield, assembly</td>
</tr>
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</table>

(Source: TechSearch International, Inc., 2011)

⇒ TSV Applications in production with backside vias for Image sensors, MEMS, LED
⇒ 3D IC Research and prototypes in memory, wireless applications (Wide I/O), high-speed logic (processors, FPGAs)
Summary

- Packaging is one key to solve the challenges of System Level Integration.
- Side by Side SiPs can be realized as extension of existing technologies.
- Stacking requires new technologies but is the strongest enabler for integration.
- Many stacking technologies are available – Few applications of stacking made it to commercial success.
- More stacking to come with realization of TSVs when cost, supply chain and yield issues will be solved.
- Until then, other solutions may step in… Fan-Out Wafer Level Packaging is offering a broad range of possibilities for System Integration and will therefore be one packaging technology of the future.
Thank You for Your Attention

Mobile and Communications Group