LATEST INSIGHTS IN MATERIAL AND PROCESS TECHNOLOGIES FOR INTERPOSER AND 3D STACKING

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Dr. Rainer Knippelmeyer, CTO and VP of R&D, GM Product Line Bonder
## SUSS PRODUCTS & SEGMENTS

<table>
<thead>
<tr>
<th>Segments</th>
<th>Photomask Equipment</th>
<th>Lithography</th>
<th>Substrate Bonder</th>
</tr>
</thead>
<tbody>
<tr>
<td>Products</td>
<td>MaskTrack Pro</td>
<td>Exposure Systems</td>
<td>Coater/Developer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Coating Developing</td>
<td>Wafer Bonder</td>
</tr>
</tbody>
</table>

### Process Steps
- Photomask Cleaning
- Laser Ablation (UV projection)
- Stepper, Scanner (proximity exposure)
- Mask Aligner (proximity exposure)
- Coating Developing
- Bond Alignment Permanent Bonding Temporary Bonding

### Markets
- Mask Manufacturing
- Advanced Packaging
- 3D Integration
- MEMS
- LED

Latest Insights in Material and Process Technologies for Interposer and 3D Stacking
CONCENTRATE ON THIN WAFER HANDLING FOR 3DIC & INTERPOSERS

Latest Insights in Material and Process Technologies for Interposer and 3D Stacking
What is the status of room temperature debonding processes & materials?

Initial R&D

Line R&D (Integration)

Volume Ramp-up

HVM

Process & Material Requirements

- Basic requirements
- Basic process Compatibility
- Initial Cost of Ownership

Specific Process Compatibility Voids, CMP, Test, Solvent comp.

Cost of Ownership

Technical Roadmap (Thinner Wafer, more bumps)

PROMISE

YIELD

IMPROVEMENT

Cost of Ownership

Process Latitude

Repeatability

Latest Insights in Material and Process Technologies for Interposer and 3D Stacking
## 2.5D / 3D-TSV PROCESS COMPATIBILITY MATRIX AND SUSS STRATEGIC PROCESS FOCUS

<table>
<thead>
<tr>
<th>DEBOND METHOD / MATERIAL</th>
<th>SOLVENT RELEASE</th>
<th>THERMAL SLIDE</th>
<th>LASER RELEASE</th>
<th>Room Temperature Bond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple Carrier (low CoO)</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>No thermal stress on solder</td>
<td>↑</td>
<td>↓</td>
<td>→</td>
<td>↑</td>
</tr>
<tr>
<td>High throughput capable</td>
<td>↓</td>
<td>↓</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>Compatible to Si - Carrier</td>
<td>↑</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
</tr>
<tr>
<td>No (laser) energy on active device</td>
<td>↑</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
</tr>
</tbody>
</table>
GENERAL ROOM TEMPERATURE DEBOND PROCESS

Temporary Bond

1. Device Wafer
2. Carrier Wafer
3. Add & Prepare Release or Zoned Layer(s)
4. Spin Coat & Prepare Adhesive(s)
5. Flip Wafer
6. Bond

Debond

1. Thinned Device Wafer
2. Carrier Wafer
3. Attach to Dicing Frame
4. Mechanical Debond at Room Temperature
5. Flip Wafer
6. Clean Device Wafer
SUSS OPEN EQUIPMENT PLATFORM AND SUPPORTED MATERIALS

Latest Insights in Material and Process Technologies for Interposer and 3D Stacking

WaferBOND™

DOW CORNING

The miracles of science*

ZoneBOND®

WSS “laser free”

Material Supplier

Electronic Materials

3M

Dow

ThinMaterials

**Note:** The image contains logos and text related to various materials and equipment used in semiconductor manufacturing. The text provides insights into material and process technologies for interposer and 3D stacking.
STEP1: WORKING WITH MATERIAL SUPPLIERS TO OVERCOME PROCESS CHALLENGES

- Voids
- TTV (Total Thickness Variation)
- Coating of high viscosity adhesives
- Adhesive Conformity and strength to topography
- Mechanical stability of adhesives for backside processing (grinding)
- Thermal stability
- Chemical stability
- Particles

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OVERVIEW ON SELECTED TEMPORARY BONDING MATERIALS FOR USE WITH GLASS AND SILICON CARRIERS

Mechanical Room Temperature Release Materials:

<table>
<thead>
<tr>
<th>THERMOSET</th>
<th>THERMOPLASTIC</th>
<th>PHOTOSET</th>
</tr>
</thead>
<tbody>
<tr>
<td>ThinMaterials</td>
<td>DOW CORNING</td>
<td>brewer science ZoneBOND®</td>
</tr>
</tbody>
</table>

Material made by WACKER
Distribution by NISSAN CHEMICAL INDUSTRIES, LTD.

Thermal Slide:

<table>
<thead>
<tr>
<th>THERMOPLASTIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>brewer science WaferBOND™</td>
</tr>
</tbody>
</table>

Laser Release:

<table>
<thead>
<tr>
<th>PHOTOSET</th>
<th>THERMOPLASTIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>3M WSS (Wafer Support System)</td>
<td>Dupont “The miracles of science”</td>
</tr>
</tbody>
</table>
STEP2: SUCCESSFUL DEBONDING & INTEGRATION FOR VARIOUS TEMPORARY BONDING MATERIALS

THIN WAFER DEBONDING

IMEC and SUSS successfully demonstrated thin wafer (50um/300mm) debonding with various temporary bond materials
STEP 3: PROCESS OPTIMIZATION FOR PRODUCTION EXAMPLE TTV OPTIMIZATION - INFLUENCING FACTORS

Material

Thermoset

Thermoplastic

Main influencing factors

- Adhesive Coating
- Adhesive Curing
- Leveling Processes
- Bond Process
- Post Bond Curing
- Release layer coating
- Release layer treatment

Thermoset:
- ✔️
- ✔️

Thermoplastic:
- ✔️
- ✔️
- ✔️
C4 bumps (70µm), ~ 2M bumps / wafer
+ 120µm adhesive thickness
+ Stack TTV < 4µm
### Examples for Post Grinding TTV for Different Adhesives at IMEC

<table>
<thead>
<tr>
<th>Temp. Bond Adhesive</th>
<th>Adhesive Thickness</th>
<th>TTV on 50µm Si</th>
<th>TTV [%] as a function of Adh. Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>55µm</td>
<td>3µm</td>
<td>5.5%</td>
</tr>
<tr>
<td>B</td>
<td>45µm</td>
<td>4µm</td>
<td>8.9%</td>
</tr>
<tr>
<td>C</td>
<td>50µm</td>
<td>2µm</td>
<td>4.0%</td>
</tr>
<tr>
<td>D</td>
<td>60µm</td>
<td>5µm</td>
<td>8.3%</td>
</tr>
</tbody>
</table>

**Diagram:**
- **Device**  
- **Carrier**  
- **Thinned Device Wafer**  
- **50µm Si Wafer**  
- **TTV**
STEP 4: REPEATIBILITY MACHINE / MATERIAL COMBINATION

Centering Arm

Notch Finder

LF300 bond chamber

Notch Shift Measurement (300-300mm)

Spec

Notch alignment results on 300mm wafer pair

Wafer number
| 1 | Introduction: Room Temperature Debonding |
| 2 | Prepare Processes & Materials for high volume manufacturing |
| 3 | Material & Process Survey |
| 4 | Next steps |
### Production Readiness
Categorized:
1: Qualified /used for high volume manufacturing
2: Integration tests in line at institute
3: Qualified by SUSS internal tests

### Cost of Ownership
Calculated:
- Equipment cost
- Process times & cycles
- Other consumables: e.g. Cost of Tape (Cost of materials)

### Performance
Weighted:
- Process Latitude (Survivability / Debondability)
- Achievable min. wafer thickness (TTV)

### Temperature
Max. temperature for post processing
Readiness level

- Qualified/Used for High Volume Manufacturing
- Integration tests at Institute
- Qualified with SUSS test criterias

Cost of Ownership (normalized to 1 for best process)

Performance (TTV / Process Latitude)
- 50%: Si TTV 1µm & all bump sizes / layers more or less plug and play

Max. Temperature
- 500°C
- 400°C
- 250°C
- 200°C

Readiness level - Cost of Ownership Matrix (Jan 13)
DO TEMPORARY BOND PROCESSES MEET THE INDUSTRY STATUS?

Initial R&D

Line R&D (Integration)

Volume Ramp-up

HVM

Industry

PROMISE

- Basic requirements
- Basic process compatibility
- Initial Cost of Ownership

YIELD

- Specific Process Compatibility
  Voids, CMP, Test, Solvent;
- Process Latitude
- Repeatability

(COST) IMPROVEMENT

- Cost of Ownership improvement
- Technical Roadmap
  (Thinner Wafer, more bumps)

Latest Insights in Material and Process Technologies for Interposer and 3D Stacking
HOW TO FURTHER IMPROVE COST OF OWNERSHIP / PROCESS LATITUDE

Cost of Materials:
- Material Usage
- Choice of Materials

Process Times
- Minimization of steps & timings

Optimization of Total Thickness Variations
- Bump density and size
- Thickness after Thinning

Extend room temperature debonding
CLEANING OPTIMIZATION - INFLUENCING FACTORS

Process Steps

Solvent Dispense → Spin Off → Rinse → Dry

Influencing Parameters

- Nozzle
- Flow Rate
- Time / Spin Speed / Puddle
- Number of cycles

- Nozzle
- Flow Rate
- Time
- Spin Speed

Solvent Compatibility

- Chemical #1
- Chemical #2
- Chemical #3
- Chemical #4

- Solves Adhesive
- Tape Frame
- Wafer
## Cleaning Optimization - Experimental Results

<table>
<thead>
<tr>
<th>Solvent</th>
<th>Glue thickness</th>
<th>Cleaning time</th>
<th>Consumption of the solvent</th>
</tr>
</thead>
<tbody>
<tr>
<td>Origin POR</td>
<td>110 µm</td>
<td>100%</td>
<td>100%</td>
</tr>
<tr>
<td>Improved POR</td>
<td>110 µm</td>
<td>72%</td>
<td>66%</td>
</tr>
</tbody>
</table>

Comparison of the cleaning time and solvent consumption.

### Solvent Price per liter

<table>
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<th>Solvent</th>
<th>Price per liter</th>
<th>Consumption of the solvent</th>
</tr>
</thead>
<tbody>
<tr>
<td>Origin POR</td>
<td>100%</td>
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<td>30%</td>
<td>66%</td>
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</table>

Comparison of the solvent consumption and the costs.
EXAMPLE FOR ROADMAP WORK ON VERY THIN WAFERS AT ITRI

300mm 50µm thickness with TSV wafer

5µm Ultra Thin Wafer

SUSS XBS300
Qualifying new materials

Optimizing new materials

Enhancement of debonding concept

Time line
Thank you!