



Thursday, May 17, 2012 (day three)

Session 15 - 3D/Through Silicon Via (TSV) (in parallel with Session 14)

Chairs: Hamid Khorram, Nikon Precision; James Lu, RPI

Very large Scale Integration motivates 3D integrated circuit architectures. This session presents complexities of Through Silicon Via techniques supporting 3D designs.

9:05

15.1

TSV RF de-embedding Method and Modeling for 3DIC

Hsiao-Tsung Yen, Yu-ling Lin, Clark Hu, S.B. Jan, Chi-Chun Hsieh, M.F. Chen, Chin-Wei Kuo, Sean Chen, Min-Chie Jeng, Taiwan Semiconductor Manufacturing Company, Ltd.

9:30

15.2

Evaluation of Fabrication Process for a Novel Chip-to-wafer (C2W) 3D Integration Approach Using an Alignment Template

Dingyou Zhang, James Jian-Qiang Lu, Rensselaer Polytechnic Institute (student)

9:55

15.3

New Method of WLCSP for Process Optimization and Reliability Prediction

Chin-Yu Ku, Wei-Chi Huang, Young-Chang Lien, Ming-Chih Yew, Po-Yao Lin, Hsiu-Mei Yu, Taiwan Semiconductor Manufacturing Company, Ltd.

10:20 Break

10:35

15.4

New Polymerizing Chemistries for Through-Silicon Via Etching (3D/TSV) (student)

William Nicoll, Eric Eisenbraun, University at Albany; Christian Dussarrat, Curtis Anderson, Rahul Gupta, Air Liquide

11:00

15.5

Decoupling Capacitor Modeling and Characterization for Power Supply Noise in 3D Systems

Kenneth Rose, James Jian-Qiang Lu, Rensselaer Polytechnic Institute; Zheng Xu, IBM Microelectronics; Xiaoxiong Gu, Michael Scheuermann, Bucknell C. Webb, John Knickerbocker, IBM T.J. Watson Research Center

11:20 Keynote: Risto Puhakka, President, VLSI Research - IC Market Trends and Forecast

12:20 Closing Remarks