

The 23rd Annual SEMI Advanced Semiconductor Manufacturing Conference – ASMC 2012

May 15-17, 2012 – Saratoga Hilton, Saratoga Springs, NY

27-Feb-12

Monday, May 14, 2012

4:00-5:30 Workforce Development Workshop (to be confirmed)

6:30-7:30 Registration

Tuesday, May 15, 2012

7:30-8:30 Registration

8:30 Welcome to the Conference: Conference Chairs (Jennifer Braggin, Entegris; Larry Pulvirent, GLOBALFOUNDRIES), ASMC 2012 Best Paper and Best Student Paper Awards

8:45 Keynote: Customer Perspective

Session 1 - Yield Enhancement (in parallel with Session 2)

Chairs: Gary Green, Green Consulting; Christopher Hess, PDF Solutions

Defect inspection, yield analysis and optimization are integral components in the development and manufacture of semiconductor devices. This session reviews optimizing and maximizing product yield and intelligently isolating faults

9:50

1.1

Identifying Systematic Critical Features Using Silicon Diagnosis Data

Chris Schuermyer, Mentor Graphics, Shobhit Malik, Thomas Herrmann, GLOBALFOUNDRIES

10:20

1.2

Using Selective Voltage Binning to Maximize Yield

Susan Lichtensteiger, Jeanne Bickford, IBM

10:45 Break

11:00

1.3

Analytic modeling of AC response to FET-level elements for CLY optimization

Gauri Karve, Ron Logan, Brian Greene, Jonathan Winslow, IBM Systems and Technology

11:25

1.4

Optimizing Product Yield Using Manufacturing Defect Weights

Jeanne Bickford, Jason Hibbeler, Sven Peyer, Vasanth Kumar, IBM; Dirk Mueller, University of Bonn

11:50

1.5

Improving Yield Learning by Electrical Fault Inspection

Jeff Block, Ron Mousaffi, Ted Lundquist, DCG Systems, Inc.

12:15 Networking Lunch

Session 2 - Factory Optimization I

Chairs: Philippe Campion, STMicroelectronics; Prashant Aji, KLA-Tencor; Stefan Radloff, Intel Corporation

Semiconductor equipment and manufacturing is increasingly complex and driven by strict economic constraints. It is vital for IC production to improve efficiency, control costs, and be good environmental stewards. This session discusses new approaches to factory optimization based on data analysis and simulation.

9:50

2.1

Automatically Optimize PM Control System for Maximum Productivity

Wei-Hao Wang, Hsi-Lo Lo, Cheng-Chung Pan, Yu-Ting Chang, Shih-Hsiung Chiou, Rexchip Electronics

10:20

2.2 Innovative approach to identify location of AMC source in cleanroom by inverse Computational Fluid Dynamics modeling

James J.J. Hwang, Kevin Chou, C.M. Yang, John Lin, Arthur Chuang, TSMC; J.M. Tsao, C.F. Chen, S.C. Hu, ITUT

10:45 Break

11:00

2.3

Managing Variability within Wafertest Production by Combining Lean and Six Sigma

Dietrich Eberts, Sophia Keil, Kristina Wilhelm, Oliver Buhmann, Infineon

11:25

2.4 Potential of use of Condition Based Monitoring in Semiconductor Equipment

Michael Cholette, Alexander Bleakie, Dragan Djurdjanovic, University of Texas; John Rasberry, Novellus (student paper)

11:50

2.5 MSC-Clustering and Forward Stepwise Regression for virtual metrology in highly correlated input spaces

PKS Prakash, P. Hung, S. F. McLoone, Callan Institute, The Irish Centre for Manufacturing Research, NUI Maynooth; A. Schirru, University of Pavia (student paper)

12:15 Networking Lunch

Session 3 - Defect Inspection

Chairs: Kazunori Nemoto, Hitachi Hi-Tech; Oliver Patterson, IBM; Dieter Rathei, D R Yield
Defect inspection, yield analysis and optimization are integral components in the development and manufacture of semiconductor devices. Defect inspection takes place in several areas of the fab, ranging from initial inspection of ultra thin films to final inspection of scribed die. This session will review several innovative techniques to detect and reduce defects in varied processes in semiconductor manufacturing.

1:30

3.1

Post Cu CMP Cleaning Process Evaluation for 32nm and 22nm Technology Nodes
Wei-Tsu Tseng, Donald Canaperi, Adam Ticknor, Leo Tai, James MacDougal, Laertis Economikos, Jennifer Muncy, Xiaomeng Chen, IBM Semiconductor R&D Center; John Zhang, STMicroelectronics, Qiang Fang, Jianping Zheng, GLOBALFOUNDRIES

1:55

3.2

Bevel Rie Application to Reduce Defectivity in Copper BEOL Processing
Christine Bunke, Kenneth Bandy, Thomas Houghton, IBM; Grace Fang, George Stojakovic, Lam Research

2:20

3.3

Defect Inspection Challenges and Solutions for Ultra-Thin SOI
C. Moulin, R. Brun, W. Schwarzenbach, C. Girard, C. Maleville I, SOITEC; W. Shen, V. Aristov, D. Kavaldjiev, G. Bast, G. Simpson, A. Azordegan, KLA-Tencor

2:45

3.4

Automated Optical Inspection for Die Prep
Xue Mei, Nital Patel, Baris Bicen, Simranjit Khalsa, Intel Corporation

3:10 Break

Session 4 - Advanced Metrology I

Chairs: Dick James, Chipworks; Alok Vaid, GLOBALFOUNDRIES
Advanced semiconductor manufacturing demands advanced metrology techniques. This session details some new reflectometry, ellipsometry, scatterometry, X-ray and thermal wave use cases.

1:30

4.1

Optical Metrology of Thickness and Indium Content of Epitaxial In_xGa_{1-x}As Layers on Si substrates

Niamh Waldron, Tommaso Orzali, Matty Caymax, Naoto Horiguchi, Youseung, imec; Jin TaeHyun Park, Zhiming Jiang, SangHyun Han, KLA-Tencor Corporation

1:55

4.2

Measurement Strategy for Dielectric Ultra-Thin Film Characterization by Vacuum Ultra-Violet Reflectometry

Georg Roeder, Martin Schellenberger, Lothar Pfitzner, Fraunhofer Institute for Integrated Systems and Device Technology (IISB); Thomas Gumprecht, Erlangen Graduate School in Advanced Optical Technology (SAOT) and IISB

2:20

4.3

DRAM Storage Cell Metrology by MBIR Technique

Leif Jonny Höglund, Semilab; Chung-Yuan Lee, Inotera Memories; Chao-Sung Lai Chang Gung University

2:45

4.4 (2585) Optimal Wafer Site Selection using Forward Selection Component Analysis
PKS Prakash, B. Honari, S.F. McLoone, NUI Maynooth; A. Johnston, Seagate Technology

3:10 Break

Session 5 - Emerging Technologies and Innovative Devices

Chairs: Eric Eisenbraun, CNSE; Jacek Tyminski, Nikon Precision

Innovative integrated circuit functionalities continue to be integrated in semiconductor manufacture. This session presents analysis of the effects of enabling technologies, and innovative integrated circuit designs.

3:30

5.1

CMOS-integrated Geometrically Tunable Optical Filters

Damiana Lerose, Daniel Gaebler, X-Fab Semiconductor Foundries AG; Stephan Junger, Fraunhofer-Institut for Integrated Circuits IIS

3:55

5.2

Modeling, design and optimization of a low level vibration piezoelectric energy harvester

Yang Xu, Zhili Hao, Old Dominion University (student)

4:20

5.3

Detection, binning and analysis of defects in a Gan-on-Si process for High Brightness Light Emitting Diodes

Sandip Halder, Andy Miller, Haris Osman, Barun Dutta, IMEC

4:45

5.4

Device characteristics research according to the array EEPROM cell's active pattern difference
Sang-bae Yi, Sun-hyun Kim, Sung-hoon You, Samsung Electronics Co. Ltd; Young-sik Choi, Yonghan Noh, Sungkyunkwan University

Session 6 - Advanced Metrology II

Chairs: Pat Gabella, The Gabella Group; David Huang, Pall Microelectronics; Thanas Boudri, Texas Instruments

Advanced semiconductor manufacturing demands advanced metrology techniques. This session details some new reflectometry, ellipsometry, scatterometry, X-ray and thermal wave use cases.

3:30

6.1

Scatterometry Measurement for SiGe AEI Sigma-Shaped Gate Structures of 28nm Technology

Autumn Yeh, Pao-Chung Lin, Yu-Wen Wang, Chin-Cheng Chien, United Microelectronics Corporation; Ching-Hung Bert Lin, Zhi-Qing James Xu, Chao-Yu Harvey Cheng, Sungchul Yoo, Jason Lin, KLA-Tencor

3:55

6.2

In-line Metrology Capability for Epitaxial Multi-stack SiGe Layers

D. Le Cunff, S. Couvrat and F. Abbate, STMicroelectronics

4:20

6.3

Laser Micro-Scale Thermal Wave Characterization of Heat Transport Processes in Modern Semiconductor Structures and Devices

A.L. Glazov, K.L. Muratkov, Ioffe Physical-Technical Institute of RAS; V.A. Kozlov, FID Technology Ltd

4:45

6.4

Development of CMP Pad Using an Unpatterned Surface Inspection System

C.Y. Cheng, S.N. Peng, S.C. Chen, Wei-Chung Yu, Dow Chemical; Larry Yang, Debbie Hu, Steve Lin, KLA-Tencor

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The 23rd Annual SEMI Advanced Semiconductor Manufacturing Conference - ASMC 2012 - Tuesday, May 15, 2012 (day one)

5:00-7:00 Session 7 - Interactive Session and Reception: This popular session provides an ideal opportunity for interaction between authors and conference attendees. During this session, participants may engage authors in in-depth discussion of a wide range of issues impacting semiconductor manufacturing, from wide range of manufacturing and technology enhancements.

Chairs: Jennifer Bragg, Entegris; Russell Dover, Brion; Dave Gross, GLOBALFOUNDRIES; Rob Pearson, Rochester Institute of Technology; Darryl Peters, Confluense; Viraj Pandit, Novellus; Thuy Tran-Quinn, IBM

Growing the Representation of Women in Leadership: A Business Imperative – IBM Microelectronics' MINDSET Initiative
M. Cretekos, K. Hall, C. Dunbar, L. Beilstein, R. Leduc, M. Cole, K. Kelly, D. Hall, S. McClure, IBM

Trench geometry and resist profiles from modeling of polarized optical spectra
Franz Heider, Christian Kayser, Hans G Millonig, Samrat A. SundaraneelInfineon Technologies; Jeffrey W Roberts, n&k Technologies

A Failure Model of Heating Filaments in Epitaxial Growth Tools
Keung Hui, Jason Mou, TSMC

Influences of Etcher Chamber Condition on Critical-Dimension Shift in Advanced Floating Gate Etching Process
Sheng-Yuan Chang, Yu-Chung Chen, An Chyi Wei, Hong-Ji Lee, Nan-Tzu Lian, Tahone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co., Ltd.,

The Analysis of device performance on a different STI liner scheme
Sun Jong Wang, Yong Han Roh, Sungkyunkwan University; Sung Hun Kim, Sung Gun Kang, Jun Sup Lee, Samsung Electronics (student)

The study of leakage current performance improvement in high voltage technology
M.H.Chen, C.T.Ni, R.H.Liu, Y.L.Chen, TSMC

Advanced Metrology and Gas Purifier Yield Improvement
Abneesh Srivastava, Thomas Gaffney, Entegris, Inc.

Analysis of an Effect of Perturbations in SWHM and Illuminating Optical Scheme Parameters on an Aerial Image
Vadim I. Rakhovsky, M.V. Borisov, D.A.Chelyubeev, V.V. Chernik, A.A. Gavrikov, D. Yu Knyazkov, P.A. Mikheev, A.S. Shamaev, NANOTECH SWHL

IMPROVE Simulation Tool - Integrating Heterogeneous Simulation Modules for Semiconductor Manufacturing Processes
Nuno Almeida, João Pires, David Sora, Critical Manufacturing

Predictive Maintenance for Ion Implanter
Gian Antonio Susto, Alessandro Beghi, University of Padova; Andrea Schirru, Simone Pampuri, Giuseppe De Nicolao; University of Pavia

Measuring Hydrochloric Acid and Ammonium Hydroxide Permeation in Bulk Chemical Distribution
Sung In Moon, Mark Caulfield, Chuck Extrand, Entegris, Inc.

Sub-s Luminescence Lifetime Measurements and Imaging for Characterization and Quality Control of Wafers
V. Buschmann, F. Koberling, R. Erdmann, U. Ortmann, PicoQuant GmbH; S. Fore, PicoQuant North America; A. Knigge Leibniz-Institut für Höchstfrequenztechnik, M. Roczen, Institut für Silizium Photovoltaic

Detecting Arcing Events in Semiconductor Equipment
Scott Singlevich, Kommisetti Subrahmanyam, Applied Materials

Overcoming The Limitation of Al Metal Line Patterning Technology Without Cu Damascene
Sung-Hi Lee, Sungkyunkwan University; SoYoung Kim, Ill-Hwan Jeoun, Tae-wook Kim, Hong-Kook Kim, Samsung Electronics Co. Ltd,

RTO process monitoring with inline non-contact technique
Nicolas Pic, Guillaume Pellegrin, Jérôme Colin, Arnaud Belfy, Emmanuel Paire, Catherine Grosjean, Patrice Laurens, STMicroelectronics

Properties of Isolation Liner and Electrical Characteristics of High Aspect Ratio TSV in 3D Stacking Technology
DeokYoung Jung, Yong Han Ro, Sungkyunkwan University; Kwang-Jin Moon, Byung-Lyul Park, Gilheyun Choi, Ho-Kyu Kang, Chilhee Chung, Samsung Electronics Co. Ltd,

Efficient Mask Protection with Advanced Stocker System
Franz Zaugg, Tec-Sem AG

Engineering Process Improvement Planning for Wafer Fabrication
Sukgon Kim, Northern Illinois University; Reha Uzsoy, North Carolina State University

Enabling Collaborative Solutions across the Semiconductor Manufacturing Ecosystem
Charles M. Weber, Jiting Yang; Patricia Gabella, The Gabella Group

Carbonized Silicon Surface Curing for Etch-Back Process
Sungjin Jang, In-cheol Kim, Kyu-yeo Lee, Soo-cheol Lee, In-soo Cho, Samsung Electronics Co. Ltd., Byoung-deog Choi, Sungkyunkwan University

Maintenance Pooling to Maximize Fab Uptime and Throughput
Mike Czerniak, Alan Ifould, Michael Mooney, Edwards; Shane Butler, NUI Maynooth

Green Manufacturing with integrated Equipment & Facilities Control
Jochen Kinauer, AIS Automation Dresden GmbH

Rules of Automation for 200mm Semiconductor Manufacturing Environment
Harald Heinrich, Johannes Sturm, Infineon Technologies; Arthur Deutschländer, FH Stralsund

Leveraging Advanced Process Control (APC) Technology in Developing Predictive Maintenance (PdM) Systems
James Moyne, Nick Ward, Parris Hawkins, Applied Materials

Automated TEM Metrology in Characterization of Si Devices
Michael Strauss, Arda Genc, FEI

Real-time, Continuous Large Particle Monitoring for CMP Slurry Quality Control
Andy Kim, Koh Murai, P.E Mega Fluid Systems; Michael Parkin, Rashid Mavliev, Vantage Technology

A Comparison of Data Mining Methods for Yield Modeling, Chamber Matching and Virtual Metrology Applications
A. Deepak Sharma, James Moyne and Helen Armer, Applied Materials

A Memory Volume Diagnostics Methodology to Facilitate Production Yield Learning With Embedded Memories
Ruth Farrugia, Stephane LeComte, Tammy Dong Lei Zheng, ST-Ericsson; Florent Garait, Christophe Giroud, Eric Faehn, STMicroelectronics; Christophe Suzor, Sagar A. Kekare, Synopsys

Improved Sustainability of an Existing Fab Operation through Reduced Energy Consumption
Don Yeoman, M+W Group US; Ron Rogerson, Spansion, Inc.

The 23rd Annual SEMI Advanced Semiconductor Manufacturing Conference - ASMC 2012

Wednesday, May 16, 2012 (day two)

8:00-8:30 Registration

8:30-9:30 Keynote: R&D Perspective

Session 8 - Factory Optimization

Chairs: Sumita Basu, Intel Corporation; Paul Werbaneth,

Semiconductor equipment and manufacturing is increasingly complex and driven by strict economic constraints. It is vital for IC production to improve efficiency, control costs, and be good environmental stewards. This session covers novel solutions for environmental and material handling challenges.

9:35

8.1

Assessing the Impact of the 450mm Wafer Size Transition on Manufacturing Facility Automated Material Handling Systems

Larry Hennessy, CH2M HILL Inc.

10:00

8.2

Operator-Free Exception Measurement Logistics for a Highly Automated 200mm Semiconductor Manufacturing Environment

Andrea Bannert, Frank Heinlein, Matthias Adam, Infineon Technologies Dresden GmbH; Kay Manja, Systema GmbH

10:25 Break

10:45

8.3

Improving Eco-Efficiency via elimination of greenhouse gases from semiconductor dry cleaning processes

Chang Hyun Oh, Seung Jong Ko, and Yun Yeong Jeong, Hynix Semiconductor Inc.

11:10

8.4

Green Mode: Equipment Interface to Optimize Semiconductor SubFab Utility Consumption

Adrienne Pierce, Edwards Vacuum; Val Parks, GLOBALFOUNDRIES

11:35

8.5

Industry Approach to the Conflict Minerals legislation

Jared Connors, Intel Corporation

12:00 Boxed Lunch

Session 9 - Advanced Process Control (in parallel with Session 8)

Chairs: Agnès Roussy, EMSE; Raymond van Roijen, IBM

The demand for high quality and yield is a constant driver for advanced process development and control techniques. This session covers innovation in process controls and shows how predictive maintenance and virtual metrology will impact manufacturing.

9:35

9.1

Tribological, Thermal, and Kinetic Attributes of 300 Vs. 450 mm Chemical Mechanical Planarization Processes

Ara Philipossian, Yun Zhuang, Siannie Theng, Yasa Sampurno, Araca, Inc.; Yubo Jiao, Xiaoyan Liao, Changhong Wu, University of Arizona; Michael Goldstein, Intel Corporation (student paper)

10:00

9.2

A Comprehensive Approach to Process Control

R. Van Roijen, C. Sinn, W. Afoh, E. Hwang, J. Scarano, S. Rangarajan, J.J. Brown, W. Brennan, S. Conti, R. Keyser, IBM

10:25 Break

10:45

9.3

An Integrated Advanced Process Control on RTP Gate Oxide Thickness and Feed-forward Implant Compensation in Mass Production

Zhang Jian, Ling Syau Yun, Liu Shi Xiang, LEI Ming, Lim Ming Chou, K. Suresh, Tan Miow Chin, Vish Srinivasan, Peter Benyon, GLOBALFOUNDRIES Singapore Pte. Ltd

11:10

9.4

Framework for Integration of Virtual Metrology and Predictive Maintenance

G. Roeder, A. Mattes, M. Pfeffer, M. Schellenberger, L. Pfitzner, Fraunhofer Institute for Integrated Systems and Device Technology; A. Knapp, H. Muhlberger, University of Augsburg; A. Kyek, B. Lenz, M. Frisch, Infineon Technologies AG; J. Bichlmeier, camLine GmbH; G. Leditzky, E. Ling, austriamicrosystems AG; S. Zoia, G. Fazio, Micron

11:35

9.5

Optimal Tuning of Epitaxy Pyrometers

Gian Antonio Susto, Alessandro Beghi, University of Padova; Andrea Schirru, Simone Pampuri, Giuseppe De Nicolao, University of Pavia (student paper)

12:00 Boxed Lunch

Session 10 - Equipment and Materials Productivity

Chairs: Scott Lantz, Intel Corporation; Christopher Long, IBM Research

The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity. Optimizing equipment performance will help improve fab metrics, minimize wafer costs and maximize competitiveness. Papers in this session will review ideas and successes to help optimize equipment utilization, improve predictive modeling of fab operations, and tool performance.

12:30

10.1

Experimental Investigation and Manufacturing Solution of the Rapid Thermal Process Induced Overlay Residues

Weihua Tong, Xuli Liu, Lei Huang, K. Suresh, Miowchin Tan, Vish Srinivasan, Peter Benyon, Sung Kim, Olivier Vatel, GLOBALFOUNDRIES

12:55

10.2

TiN Metal Hardmask Etch Residues Removal for Cu Dual Damascene Device with TiN Corner Rounding Scheme

Hua Cui, EKC Technology, DuPont Electronic Technologies

1:20

10.3 Humidity Rise after Purge in Micro-Environments

Chuck Extrand, Entegris, Inc.

1:45 Break

2:05

10.4

A Novel Approach to Optical Wafer Pre-Alignment Using Innovative Ranging Edge Detectors

Thomas Jerman, Bright Red Systems GmbH; Walter Leitgeb, Infineon Technologies AG

2:30

10.5

Lithography Challenges and Solutions for MEMS/LED applications

Hamid R. Khorram, Nikon Precision

Session 11 - Advanced Patterning and Design for Manufacturability

Chairs: Holly Magoon, Nikon Precision; Mike McIntyre, GLOBALFOUNDRIES

IC production today requires innovative lithography design and manufacturing techniques. Papers in this informative session include collaborative efforts between chip makers and equipment suppliers discussing leading-edge solutions for advanced lithography techniques such as double patterning. Recent developments in Design for Manufacturability will also be highlighted.

12:30

11.1 (2692) Enhanced Process Control of Pitch Split Double Patterning by use of CD-SEM critical dimension uniformity and local overlay metrics

Scott Halle, Matthew Colburn, Chiew-seng Koay, Shyng-Tsong Chen, IBM; Shoji Hotta, Takeshi Kato, Hitachi High-Technologies Corporation, Atsuko Yamaguchi, Hitachi Ltd.,

12:55

11.2 (2683) Design Based Classification for Process Window Defect Characterization of BEOL ADI Layers

YoungSu Kim, Young Hun Kwon, Ki Ho Kim and Tae Woong Hwang, Samsung Electronics Co., Ltd.; Raghav Babulnath, Colin Yu, Paresh Desai, KLA-Tencor Corporation

1:20

11.3 (2716) Optimizing scanner performance using computational methods - practical implementation for HVM fab

Hua Cao, Chris Lu, Aaron Chu, Keyao Zhu, Chien Ming Wang, Wenjin Huang, Youping Zhang, Song Pang, Paul Chang, Gary Zhang, Jason Shields, Brion Technologies – ASML

1:45 Break

2:05

11.4 (2542) A Self-aligned Double Patterning Technology Using TiN as the Sidewall Spacer

Yuan-Chieh Chiu, Shu-Sheng Yu, Fang-Hao Hsu, Hong-Ji Lee, Nan-Tzu Lian, Tahone Yang, Kuang-Chao Chen and Chih-Yuan Lu, Macronix International Co., Ltd.

2:30

11.5

Session 12 - Equipment and Materials Productivity (in parallel with Session 13)

Chairs: Johann Massoner, Infineon; Naomi Yoshida, Applied Materials

The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity. Optimizing equipment performance will help improve fab metrics, minimize wafer costs and maximize competitiveness. Papers in this session will review ideas and successes to help optimize equipment utilization, improve predictive modeling of fab operations, and tool performance.

2:55

12.1

Enhancements in Resizing Single Crystalline Silicon Wafers up to 450 mm by using Thermal Laser Separation

M. Koitzsch, D. Lewke, M. Schellenberger, L. Pfitzner, H. Ryssel, Fraunhofer Institute of Integrated Systems and Device Technology (IISB); H.-U. Zühlke, JENOPTIK Automatisierungstechnik GmbH

3:20

12.2

Modifying Mask-Blank Manufacturing to Incorporate Cleaning and Deposition Experimentation
Milton Godwin, Anne Rudack, SEMATECH

3:45

12.3

High-k/Metal Gates in Leading Edge Silicon Devices
Dick James, Chipworks

4:10 Break

4:30-5:30 Panel Discussion: Competing for R&D Dollar: Funding the Future

As advances in materials and process technology continue, the semiconductor manufacturing industry is faced with difficult challenges concerning costs. In order to stay on the productivity curve, companies must address several critical technology issues. However, with limited R&D dollars, it is unclear how wafer size transition, next node scaling, new transistor technology, and 3D IC will be funded. A limited number of companies will pursue 450mm, but many more are looking at 3D ICs. Add to this the challenge of EUV. Where will IC companies put their investment? What about their suppliers? Should the focus be on 450mm conversion or advanced process technologies? Who will ultimately pay the price? Where does the ROI end? A panel of industry experts addresses these and other related productivity and technology challenges facing the global chip-making community.

6:00-7:00 Networking Reception – Canfield Casino, Saratoga Springs, NY

Reception Sponsors:



Session 13 - Equipment Performance

Chairs: Jan Rothe, GLOBALFOUNDRIES; Brett Williams, ON Semiconductor

The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity. Optimizing equipment performance will help improve fab metrics, minimize wafer costs and maximize competitiveness. Papers in this session will review ideas and successes to help optimize equipment utilization, improve predictive modeling of fab operations, and tool performance.

2:55

13.1

The Hidden Productivity: How to Get More Out of Your Tool
Adar Kalir and Andy Sharon, Intel Corporation

3:20

13.2

Efficient FDC based on Hierarchical Tool Condition Monitoring Scheme (student) Jakey Blue, Agnès Roussy, EMSE-CMP; Alexis Thieullen, ST Microelectronics and LSIS-University Aix-Marseille

3:45

13.3

Predictive Sampling Approach to Dynamically Optimize Defect Density
Control Operations

M. Pfeffer, R. Oechsner, L. Pfitzner, Fraunhofer Institute for Integrated Systems and Device Technology (IISB); S. Eckert, A. Hartmann, H. Gold, G. Biebl, J. Kaspar, Infineon Technologies

4:10 Break

The 23rd Annual SEMI Advanced Semiconductor Manufacturing Conference ASMC 2012

Thursday, May 17, 2012 (day three)

7:30-8:00 Registration

8:00-9:00 Tutorial: Advanced Device Design

Session 14 - Defect Inspection II

Chairs: Jeff Barnum, KLA-Tencor; Bill Miller, IBM Microelectronics

Defect inspection, yield analysis and optimization are integral components in the development and manufacture of semiconductor devices. This session will feature papers on e-beam inspection used for defect inspection of advanced technologies and improving defect inspection efficiency.

9:05

14.1

E-Beam Inspection for Combination Use of Defect Detection and CDU

Measurement

Carol Boye, Theodorus Standaert, IBM Integration; Fei Wang, Chris Lei, Shih-tsung Chen, Jack Jau, Derek Tomlinson, Hermes Microvision Inc.

9:30

14.2

Lithography Inspection Methodology Employing a Complementary Strategy of Advanced Darkfield and High Sensitivity Brightfield Inspection Tools

Jyn Hao Syu, Chen Chiz Lin, P Y Chiang, Nagus Chen, United Microelectronics Corporation; Henry Yang, Eros Huang, Harvey Cheng, Mahatma Lin, Kan Chen, Jun Lang, KLA-Tencor

9:55

14.3

Patterned Wafer Lithography Inspection using Unpatterned Wafer Inspection Tool

Dongchul Ihm, Sungchae Choi, Hyeol Lee, Byoung-ho Lee, Samsung Electronics Co., Ltd.; KeunSu Kim, Stephan Kang, Yong Gao, Seong Yoo, KLA-Tencor

10:20 Break

10:35

14.4

Use of 22 nm SEM Non Visual Defect Data at Litho as a Process Quality Indicator

Carol Boye, Christopher J. Penny, Joe Connors, Donna Boyles, IBM; Rajesh Ghaskadvi, KLA-Tencor

11:00

14.5

E-Beam Inspection for Detection of Sub-Design Rule Physical Defects

Oliver D. Patterson, Julie Lee, IBM; KC Chai, GLOBALFOUNDRIES; Chris Lei, Hermes Microvision Inc.

11:20 Keynote: IC Market Analysis/Forecast

12:20 Closing Remarks

Session 15 - 3D/Through Silicon Via (TSV)

Chairs: Hamid Khorram, Nikon Precision; James Lu, RPI

Very large Scale Integration motivates 3D integrated circuit architectures. This session presents complexities of Through Silicon Via techniques supporting 3D designs.

9:05

15.1

TSV RF de-embedding method and modeling for 3DIC

Hsiao-Tsung Yen, Yu-ling Lin, Clark Hu, S.B. Jan, Chi-Chun Hsieh, M.F. Chen, Chin-Wei Kuo, Sean Chen, Min-Chie Jeng, Taiwan Semiconductor Manufacturing Company, Ltd.

9:30

15.2

Evaluation of Fabrication Process for a Novel Chip-to-wafer (C2W) 3D Integration Approach Using an Alignment Template

Dingyou Zhang, James Jian-Qiang Lu, Rensselaer Polytechnic Institute (student paper)

9:55

15.3

New Method of WLCSP for Process Optimization and Reliability Prediction

Chin-Yu Ku, Wei-Chi Huang, Young-Chang Lien, Ming-Chih Yew, Po-Yao Lin, Hsiu-Mei Yu, Taiwan Semiconductor Manufacturing Company, Ltd.

10:20 Break

10:35

15.4

New Polymerizing Chemistries for Through-Silicon Via Etching (3D/TSV)

William Nicoll, Eric Eisenbraun, University at Albany; Curtis Anderson, Rahul Gupta, Christian Dussarrat, Air Liquide (Student paper)

11:00

15.5

Decoupling Capacitor Modeling and Characterization for Power Supply Noise in 3D Systems

Zheng Xu, Kenneth Rose, James Jian-Qiang Lu, Rensselaer Polytechnic Institute; Xiaoxiong Gu, Michael Scheuermann, Bucknell Webb, John Knickerbocker, IBM T.J. Watson Research Center

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