Thin Die Stacking for Wide I/O Memory-On-Logic

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Corporate Technology Development and IP Director

The Power of $[x]$
Outline

- EV Group at a Glance
- Motivation for Wide I/O Memory
- Package Setup and Exemplary Process Flow
- Temporary Bonding
- Stacking of Thin Dies
- Summary and Conclusions
EV Group at a Glance

EV Group (EVG) is a global supplier of
- Wafer Bonders
- Aligners
- Coaters / Developers
- Temporary Bonders / Debonders (Laminator)
- Cleaners
- Inspection Systems

EV Group (EVG) is a global supplier to
- Advanced Packaging, 3D Interconnect
- MEMS (MicroElectroMechanical Systems)
- SOI (Silicon-On-Insulator)
- Compound Semiconductor and Silicon based Power Devices
- Nanotechnology

EV Group holds the dominant share of the market for wafer bonding equipment (especially SOI bonding) and is a leader in lithography for advanced packaging and nanotechnology.
Motivation for wide I/O Memory

Comparison between PoP and TSV based Wide I/O Memory Package

Source: Samsung
Motivation for wide I/O Memory

Driver: Mobile Applications

Source: Samsung
Package Setup

Source: Micron

Source: EVG
Package Setup

DRAM Layers

Wafer Level Overmolding

Underfill

Base Wafer (Logic)

Temporary Adhesive

Temporary Carrier

Fine Pitch Interconnect

Source: EVG
Exemplary Process Flow Memory Cube

Base Wafer BEOL → Temporary Bonding → Thinning and Via Reveal

Chip to Wafer Stacking → Bond Pad Formation → Bond Pad Formation

Chip to Wafer Stacking → Overmolding

Source: EVG
Stacked Memory – New Processes Required

Temporary Bonding / Debonding

Chip-to-Wafer Stacking

Interconnect Structure:

~15 μm
~10 μm
~5 μm

40 μm

~80 μm

Inspection
# Adhesive Thickness Requirements

**Interconnect Structure:**
- ~15 µm
- ~10 µm
- ~5 µm

<table>
<thead>
<tr>
<th>Topography</th>
<th>Interconnect</th>
<th>Application</th>
<th>Adhesive T</th>
<th>Adhesive T</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 10µm</td>
<td>Bonding Pads</td>
<td>Die to Die Various</td>
<td></td>
<td>20µm</td>
</tr>
<tr>
<td>~30 to 40µm</td>
<td>Microbumps, Cu-pillars</td>
<td>Die to Die</td>
<td></td>
<td>40-50µm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Die to Interposer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>~80 to 90µm</td>
<td>Bumps</td>
<td>Die to Substrate</td>
<td></td>
<td>90-100µm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Interposer to Substrate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TB / DB Process Concepts Supported by EVG Equipment

- Solvent Debeonding (Perforated Carriers)
- Double Side Adhesive Tapes
- Slide Off Debonding
- ZoneBOND™ Debonding
- Mechanical Peel-Off Debonding
- UV Release Debonding

Historical Technology
Mainstream Market
Niche Market Application
The surface of the carrier substrate is chemically treated in Center Zone so that the adhesive does not adhere strongly to the carrier. Therefore, only low separation force is required for carrier separation once the polymeric edge adhesive has been removed by solvent dissolution or other means. No treatment of Edge Zone, therefore, strong adhesion to carrier at perimeter.
Edge Zone Release Approach

**Edge Zone Release (EZR®)**

Release adhesives at the stack edge

**Edge Zone Debond (EZD®)**

Separation at the carrier; No vertical force to device wafer

Mechanical separation of the carrier wafer
Adhesives for TB /DB

Applications Windows - ZoneBond® Adhesives

- DRAM
- Logic
- Si based Power Devices

Bonding Temperature vs. Maximum Process Temperature Capability

Adhesive Optimization
**Post-bond TTV**

TTV of the bondline is a critical performance parameter of the TB / DB solution. Below table lists the current performance of the combination of EVG coating and bonding technology and the roadmap for further improvement.

<table>
<thead>
<tr>
<th>Bondline</th>
<th>TTV today</th>
<th>Q4 2012</th>
<th>Q2 2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>20µm</td>
<td>2 µm</td>
<td>1 µm</td>
<td>1 µm</td>
</tr>
<tr>
<td>50µm</td>
<td>3 µm</td>
<td>2.5 µm</td>
<td>2 µm</td>
</tr>
<tr>
<td>100µm</td>
<td>4.5 µm</td>
<td>4 µm</td>
<td>3 µm</td>
</tr>
</tbody>
</table>

*With 3 mm standard edge exclusion zone!*
Metrology Module – Working Principle

- Sensor 1: Infrared Based Sensor (IR interferometer)
- Sensor 2: White Light Interferometer
- Sensors scan across the wafer stack
EVG850 - New high T-Put System launched

- 9 process modules
- True continuous mode of operation with local FOUP storage system
- Integrated metrology with scan times < 80 sec / wafer
- Up to >40 uph throughput
Stacking of Thin Dies

Technology – Development Focus Areas

• C2W Bonding
  • Pre-applied underfills
  • Solder bonding, Cu-Sn bonding

• W2W Bonding
  • High Throughput / Low Temp Cu Bonding
  • Hybrid Bonding (Oxide & metal at the same time)
  • Plasma activated bonding

Equipment – Latest Developments

• C2W Platform improvements
  • Improved alignment accuracy

• W2W Alignment Accuracy
  • 0.5 µm, 3 sigma SmartView alignment accuracy

• Oxide Removal & Management
  • Pre-processing modules development and qualification

• Alignment accuracy inspection
## Chip-to-Wafer + Wafer-to-Wafer Bonding

<table>
<thead>
<tr>
<th></th>
<th>Wafer-to-Wafer</th>
<th>Chip-to-Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Wafer size</strong></td>
<td>Common size</td>
<td>Dissimilar wafer size</td>
</tr>
<tr>
<td></td>
<td>Wafer and Die</td>
<td>Dissimilar die size</td>
</tr>
<tr>
<td><strong>Economy / Throughput</strong></td>
<td>Wafer scale throughput</td>
<td>Die scale throughput</td>
</tr>
<tr>
<td><strong>System compatibility</strong></td>
<td>Wafer handling</td>
<td>Wafer and die handling</td>
</tr>
<tr>
<td><strong>Yields</strong></td>
<td>Lower than lowest yield wafer</td>
<td>Select known good die (KGD)</td>
</tr>
<tr>
<td><strong>Alignment</strong></td>
<td>&lt; 0.5 µm global alignment</td>
<td>~ 5 µm &gt; 5000dph</td>
</tr>
<tr>
<td></td>
<td></td>
<td>~ 3 µm &lt; 3000dph</td>
</tr>
<tr>
<td><strong>Fabrication site</strong></td>
<td>Fab or packaging</td>
<td>Packaging</td>
</tr>
</tbody>
</table>
# Chip-to-Wafer + Wafer-to-Wafer Bonding

<table>
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<tr>
<th></th>
<th>Wafer-to-Wafer</th>
<th>Chip-to-Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Wafer size</strong></td>
<td>All design details of both wafers must be in control</td>
<td>Best Modularity and Flexibility</td>
</tr>
<tr>
<td><strong>Economy / Throughput</strong></td>
<td><strong>Best Throughput</strong></td>
<td>Die scale throughput</td>
</tr>
<tr>
<td><strong>System compatibility</strong></td>
<td><strong>Best Cleanliness</strong></td>
<td>Wafer and die handling</td>
</tr>
<tr>
<td><strong>Yields</strong></td>
<td><strong>High Yield or Redundant Design</strong></td>
<td>KGD = Best Yield</td>
</tr>
<tr>
<td><strong>Alignment</strong></td>
<td><strong>Best Accuracy</strong></td>
<td>~ 5 µm &gt; 5000dph</td>
</tr>
<tr>
<td></td>
<td></td>
<td>~ 3 µm &lt; 3000dph</td>
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<td><strong>Fabrication site</strong></td>
<td><strong>Best Cleanliness</strong></td>
<td>Packaging</td>
</tr>
</tbody>
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Requirements for W2W → if met: W2W
Chip-to-Wafer vs. Wafer-to-Wafer Throughput

Throughput comparison: C2W vs. W2W

Throughput enhancement for C2W: true known good die (KGD) manufacturing

Higher C2W Throughput = Less Accuracy
Reflow soldering vs. Thermo-Compression Bonding

For fine pitch interconnect and dies with TSVs, conventional reflow soldering does not work anymore because:

- Dies are very thin. Stress causes dies to bend. 
  → No mechanical contact between interconnects
- Fine pitch required reduction of solder volume. 
  → Reduced solder volume results in lower tolerance for height variations and / or bow and warp of chips

For this reason, Thermo-Compression Bonding is becoming the standard for fine-pitch interconnect
Thermal Profile for Thermo-Compression Bond

- Entire bonding cycle may take from 4 seconds to 16 seconds per chip.
- This greatly limits the throughput of the Flip Chip Bonder.
  → Thermal Process to be performed collectively for all chips at once.
Advanced Chip to Wafer Bonding

A two step process for high throughput:

Prebonding:
- Only Known Good Dies
- Prebonding of the dies on the wafer
- MEMS compatible
- At high speed
- Various methods available

Permanent Bonding:
- Temperature
- with / without Force
- Gas / Pressure / Vacuum

EASY TRANSFER
AC2W for Memory or Memory on Logic

- IME, Singapore
  - 4 layer stack with TSVs, usage of pre applied underfill
  - simultaneous permanent bonding of multiple layers

Source: IME, Poster, IME Scientific Advisory Panel, 2010
AC2W for Memory on Logic

- IMEC, Belgium
  - Hybrid CuCu bonding, use of pre-applied underfill
  - Connection of TSVs in 16.9 µm thin dies

Source:
Alignment Accuracy Results by Sematech

Alignment Shift From Collective Bonding After Implementing Tooling and Process Improvements

- Collective bonding shift improved to <2 µm (ave. shift = 0.8 µm)
- No damage to tooling

Post-bond alignment accuracy: <2µm (3σ)
Summary and Conclusions

• Next generation memory based on TSV type interconnects requires novel manufacturing techniques

• Temporary Bonding / Debonding and Advanced Chip to Wafer Bonding methods will play a key role in enabling low cost manufacturing of such novel memory devices.

• EVG provides leading edge equipment and process solutions that support the manufacture of next generation memory devices.
Thank you for your attention!

Please visit us at booth #1076

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