Exploring Silicon Interposers through System Co-Design and Co-Analysis to Maximize Performance

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Agenda

• 3D IC Co-Design Flow
• Multi-Fabric Planning for Interposers
• Interposer Extraction
  – during implementation
  – for system-level co-analysis
• Interposer System-Level Co-Analysis
3D IC Co-Design Flow
Why 3D-IC?

- **Application Requirements**: Bandwidth, Power, Reduced Area
- **Obvious Solution**: Jump to next process node, but … (20nm/14nm/10nm)
  - Yield?
  - Shrinking Analog to smaller geometries increases variability and leakage!
  - Reuse of IP built on older nodes?
  - COST?
- **What is the alternative?** Move into vertical stacking – 3D-ICs
  - Neither alternative is easy due to technical and manufacturing challenges
Cadence and 3D-IC
Cadence 3D-IC solution (8 test chips, 1 production chip) since 2007

- **3D-IC Challenges with a heterogeneous stack**
  - **Integrated methodology amongst Custom, Digital and Package**
    - Optimize TSV/bump location, bump alignment across dies
    - DFT/Test for 3D
    - Interposer routing / 3D routing for minimized IR drop
    - Parasitic extraction for the stack
    - Thermal management
  - **Ecosystem**
    - Hand offs, models, rules, constraints, etc.

**Custom, Digital, and Package Need to Understand 3D Constructs**
Modeling and database infrastructure to support TSVs, micro bumps, and backside metals

**Seamless Digital, Custom, and Package Co-Design**
Cadence: the leader in custom with Virtuoso® technology
Cadence: SiP solution spanning digital, custom, and package for the last 6 years
Cadence: the leader in mixed-signal solutions using OpenAccess

**Ecosystem Partnership and Real Experiences/Proofpoints**
Cadence: working on 3D-IC with ecosystem partners since 2007
Completed 8 test chips / 1 production chip (spanning short, medium, long term)
Several ongoing projects
Cadence Silicon-Proven 3D-IC Solution

Plan ➔ implement ➔ test ➔ verify

More than 5 years of real test chip and real partner experience in 3D-IC

Complete and integrated 3D-IC solution: spans IP, custom, digital, and package

Seamless integration of digital, custom, and package domains
# Silicon Interposer System Design Flow

## STEP 1: Top Die Implementation
- Bump Assignment
- RDL Routing
- Wafer level DFT/BIST

## STEP 2: Interposer Implementation
- Bump Alignment – Adjust TSV/Bump assignment
- Interposer Routing

## STEP 3: Interposer Analysis
- RC Extraction
- DRC/LVS

## STEP 4: Stacked System
- Interdie DRC/LVS
- IR Drop Analysis
- SI/PI analysis
- Package level DFT/BIST

![Silicon Interposer Method](image)
Multi-Fabric Planning for Interposers
The Complexity of Optimizing Four Fabrics vs. Three Fabrics

- Chip-Package-Board vs. Chip-Interposer-Package-Board
  - one extra fabric doubles the system interconnect complexity
    - Intra interposer connectivity
    - Inter interposer connectivity
The Problem

• An un-optimized design is costly and performs poorly
  – Unnecessary crossovers add vias
    – **performance**: vias add self and mutual parasitics for signals, noise coupling for power
  – Unnecessary vias blocks routing channels
    – **cost**: blocked routing leads to additional package and board layers

• The problem is:
  – Chip-interposer and interposer-package connectivity adversely impacts the performance and add cost to the overall system when chip and package are not considered

• The goal is:
  – Optimize connectivity and routing feasibility when considering fixed and variable designs throughout the system
  – Hand off the interposer plan to an IC tool for detailed implementation
Key Requirements for System Planning

- **Multi-Fabric capability**
  - Simultaneously manage and interact with multiple designs across die, package, interposer, and board

- **Hierarchy management**
  - Define and manage relationships between designs

- **Net management and mapping**
  - Map nets to adjacent fabrics to establish the connectivity
  - Produce top-level system net list

- **Connection planning and optimization**
  - Define and optimize connections between substrates
  - Supporting top-down, bottom-up, or middle-out
  - Propagate net changes and evaluate impacts
  - Net lists exported in Verilog, ASCII, or DEF formats
Key Requirements for System Planning

• **Design Abstraction**
  – Apply abstraction by using best available data then refine and optimize as detailed content become available

• **Bump pattern development**
  – Asymmetrical multiple pitch patterns
  – Export appropriate bump views to IC and package tools

• **RDL auto-routing and editing**
  – Validate routeability and quality of bump pad placement

• **Interposer instantiation**
  – Generate initial design containing bumps on top/bottom and connectivity
  – Export to IC P&R tool for detailed implementation and final routing
A Typical Silicon Interposer System

<table>
<thead>
<tr>
<th>Device</th>
<th>Data Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>BGA</td>
<td>BGA.txt from Cadence APD</td>
</tr>
<tr>
<td>Si Interposer</td>
<td>Created on-the-fly</td>
</tr>
<tr>
<td>Die Slice 1</td>
<td>LEF / OrbitIO IOview</td>
</tr>
<tr>
<td>Die Slice 2</td>
<td>ASCII data</td>
</tr>
</tbody>
</table>

Multi-Fabric Planning View
Planning-Driven, Analysis-Augmented Interposer Implementation

Problem:
• Lack of optimization between the Silicon Interposer and adjacent fabrics adds cost to the overall system and reduces system performance

Solution: Interposer planning
• A comprehensive system view and pin assignment optimization function will reduce the number of signal crossovers in the overall system
• System route feasibility and system SI and PI analysis validates that the Interposer will meet design specifications

Result:
• A system optimized Silicon Interposer plan that can be handed off to IC implementation tools for final manufacturing prep
Interposer Extraction
Chip PDN models can vary from 2-node to N-nodes, where N is the number of die pads.

There can be 1 to M current sources, where M may be much larger than N.
3D IC Power Model Extraction

μ-Bump Ports

TSV Equivalent Circuit Model

Stimulus Current Profiles

Power Grid Circuit Model

[μ-]Bump Ports

Final output netlist is in SPICE format
Die Power Model Extraction

• Die Power Model includes
  – Spatially-distributed power grid model (R, L, C, K)
  – TSV models (if present)
  – Device parasitic models (effective C and leakage)
  – Stimulus current profiles
  – Model of user defined resolution
    • potentially very high resolution - each bump could have a distinct circuit terminal
  – Reduced-order Model of concise circuit size
    • compressed from the model of the entire multi-layer power-ground grid

• Application
  – System-level power analysis using Cadence/Sigrity or third party tools
• To XcitePI … a 3DIC is no different than a 2DIC

• Pin based circuit model

• L and C matrices for mutual coupling
2D Die IO Model Extraction
Enabling Chip-Power-Aware SSO Analysis

Apply IO driver models on these ports

IO Device ports

Connect to package pins through these ports

Final output netlist is in SPICE format
2.5D Silicon Interposer Model Extraction

Connect to chip die pads through these ports

Chip stack-up and routing (top)

TSVs

Chip stack-up and routing (bottom)

Connect to package pins through these ports

μ-Bump Ports

Bump Ports

Final output netlist is in SPICE format
Die IO Model Extraction

• Die IO Model includes
  – Distributed IO power grid and IO signal net models (R, L, C, K)
    • RDL and Silicon Interposers may be included in extraction
  – Considers all parasitics
    • self parasitics for both signals and power
    • mutual parasitics within and between signals and power
  – Model of user defined resolution
    • potentially very high resolution - each bump could have a distinct circuit terminal
  – Reduced-order Model of concise circuit size
    • compressed from the model of the entire multi-layer power-ground grid

• Application
  – System-level signal integrity analysis using Cadence/Sigrity or third party tools, including power-aware SSO simulation
Extraction During Implementation
Electrical Performance Assessment

- Quickly check IO P/G robustness and signal electrical performance to identify potential design defects.
Interposer System-Level Co-Analysis
A Silicon Interposer Test Case

- Two chips on interposer wafer
  - 40LP logic die
  - 40LP memory die
  - 65LP interposer die
- MIMcaps in interposer PDN
- Interposer high-freq constraint-driven routing for wide-IO interface
Chip and Interposer Model Extraction with XcitePI

Circuit import from LEF/DEF

Memory Die

Logic Die

Interposer
Interposer Electrical Performance Assessment by XcitePI

<table>
<thead>
<tr>
<th>Bump name</th>
<th>Net</th>
<th>R(Ohm)</th>
<th>L(nH)</th>
<th>C(µF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bump2016_U_Qbus_To_LOG[91]</td>
<td>U_Qbus_To_LOG[91]</td>
<td>325.871</td>
<td>3.41489</td>
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<td>Bump2014_U_Qbus_To_LOG[90]</td>
<td>U_Qbus_To_LOG[90]</td>
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<td>2.06095</td>
<td>0.873107</td>
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<tr>
<td>Bump2012_U_Qbus_To_LOG[89]</td>
<td>U_Qbus_To_LOG[89]</td>
<td>315.501</td>
<td>3.30021</td>
<td>0.452756</td>
</tr>
<tr>
<td>Bump2010_U_Qbus_To_LOG[88]</td>
<td>U_Qbus_To_LOG[88]</td>
<td>320.054</td>
<td>3.40535</td>
<td>0.490629</td>
</tr>
<tr>
<td>Bump2008_U_Qbus_To_LOG[87]</td>
<td>U_Qbus_To_LOG[87]</td>
<td>320.386</td>
<td>3.39847</td>
<td>0.501783</td>
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<tr>
<td>Bump2006_U_Qbus_To_LOG[86]</td>
<td>U_Qbus_To_LOG[86]</td>
<td>320.188</td>
<td>3.29856</td>
<td>0.469831</td>
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<tr>
<td>Bump2004_U_Qbus_To_LOG[85]</td>
<td>U_Qbus_To_LOG[85]</td>
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<td>3.40876</td>
<td>0.442901</td>
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<tr>
<td>Bump2002_U_Qbus_To_LOG[84]</td>
<td>U_Qbus_To_LOG[84]</td>
<td>318.139</td>
<td>3.36948</td>
<td>0.538333</td>
</tr>
</tbody>
</table>

Impedance seen by memory looking into interposer

Impedance seen by logic looking into interposer
Corresponding Package and Board

Package Stack-up

Board Stack-up
Package/Board Model Extraction with PowerSI

Models with MCP Headers

Package S-parameter

PCB S-parameter

```
.SUBCKT pkg
  +
  DIE_3763
  +
  DIE_3762
  +
  BGA_H13
  +
  BGA_M13
+.

.SUBCKT pcb
  +
  BGA_H13
  +
  BGA_M13
  +
  J1_A48
  +
  J1_A41
+.

.MODEL Spara S
  +
  BNPFILE = "pkg.bnp"
  +
  DIE_3763
  +
  DIE_3762
  +
  BGA_H13
  +
  BGA_M13
  +
  MNAME = Spara
+.

.ENDS
```
IBIS v5.0 Power-Aware Model Generation with T2B

Transistor Model

IBIS v5.0
Power-Aware Model
Complete System SSO Co-Analysis with SystemSI

- Power supplied by VRM on board.
- Non-ideal power effects are included throughout the entire system.
SSO System Co-Analysis Results

- 100mV noise with only 8-bits randomly switched.
- Non-ideal PDN has significantly greater noise and more timing jitter.
Another Silicon Interposer Test Case

- 3 chips on interposer
  - logic/memory/PLL

- Mixed-technology
  - 65LP/40LP/28HP

- Logic and Memory share PDN on the interposer

- MIMcaps in the interposer PDN
Co-Analysis Flow for Emissions

Frequency Domain Results through FFT

Transient Co-Analysis of Chip-Interposer-Package System

Far-field Radiation

Near-field Radiation
Far-field Radiation Results

Emissions are reduced by \( \approx 10 \text{dB} \) at the peaks near 500MHz and 1GHz after adding 10 100pF MIMcaps in the interposer PDN.
Near Field Radiation Analysis

1GHz (without mimcap)

- E near field strength observed above top layer (5mm) of the package

1GHz (with mimcap)
Summary
Summary

- 3D IC design tools are available and becoming more full-featured
  - electrical extraction tools are less affected by 3D nature

- Multi-fabric planning tools enable lower-cost and higher-performance interposer designs
  - despite increased complexity of inter-fabric connectivity

- Electrical analysis for 2.5D and 3D IC is readily available
  - electrical performance assessment should be applied during implementation for early feedback
  - model extraction supports system-level co-analysis

- Full system co-analysis supports power, signal and emissions design
  - non-ideal PDN effects may be included throughout the entire system
  - MICcap effects for interposers are easily included