Monday, May 14, 2012
3:30-5:30 Workforce Development Workshop (Saratoga 1)
6:30-7:30 Registration (Hilton Hotel Lobby)

Tuesday, May 15, 2012
7:30-8:30 Registration (level 2 – Saratoga City Center)
8:30 Welcome to the Conference: Conference Chairs (Jennifer Braggin, Entegris; Larry Pulvirent, GLOBALFOUNDRIES); ASMC 2011 Best Paper and Best Student Paper Awards (M2B)
8:45 Keynote: Michael Campbell, Sr. Vice President, of Engineering, Qualcomm: Mobile Wireless Driving the Semi Industry: A Semi Customer’s View (Sponsored by CNW)

Session 1 - Yield Enhancement (Meeting Room 2B)
Chairs: Gary Green, Green Consulting; Christopher Hess, PDF Solutions
Defect inspection, yield analysis and optimization are integral components in the development and manufacture of semiconductor devices. This session reviews optimizing and maximizing product yield and intelligently isolating faults.

9:50
1.1 Identifying Systematic Critical Features Using Silicon Diagnosis Data
Chris Schuermyer, Mentor Graphics; Shobhit Malik, Thomas Herrmann, GLOBALFOUNDRIES

10:20
1.2 Using Selective Voltage Binning to Maximize Yield
Susan Lichtensteiger, Jeanne Paulette Bickford, IBM Systems and Technology Group

10:45 Break (Sponsored by ATMI)

11:00
1.3 Analytic Modeling of AC Response to FET-level Elements for CLY Optimization
Gauri Karve, Ron Logan, Brian Greene, Jonathan Winslow, IBM Systems and Technology Group

11:25
1.4 Optimizing Product Yield Using Manufacturing Defect Weights
Jeanne Paulette Bickford, Jason D. Hibbeler, Sven Peyer, Vasanth S. Kumar, IBM STG; Dirk Mueller, University of Bonn

11:50
1.5 Improving Yield Learning by Electrical Fault Inspection
Jeffrey A. Block, Paul Sakamoto, Ted Lundquist, DCG Systems, Inc.

12:15 Networking Lunch (Meeting Room 1A)

Session 2 - Factory Optimization I (Meeting Room 2A)
Chairs: Prashant Aji, KLA-Tencor; Stefan Radloff, Intel Corporation
Semiconductor equipment and manufacturing is increasingly complex and driven by strict economic constraints. It is vital for IC production to improve efficiency, control costs, and be good environmental stewards. This session discusses new approaches to factory optimization based on data analysis and simulation.

9:50
2.1 Innovative Approach to Identify Location of AMC Source in Cleanroom by Inverse Computational Fluid Dynamics Modeling

10:20
2.2 Managing Variability within Wafertest Production by Combining Lean and Six Sigma
Dietrich Eberts, Kristina Wilhelm, Infineon Technologies; Sophia Keil, Rainer Lasch, Dresden University of Technology; Oliver Buhmann, University of Applied Sciences

10:45 Break (Sponsored by ATMI)

11:00
2.3 Potentials of Condition Based Monitoring in Semiconductor Equipment (student)
Michael E. Cholette, Dragan Djurdjanovic, University of Texas at Austin; John Rasberry, Novellus Systems

11:25
2.4 MSC-Clustering and Forward Stepwise Regression for Virtual Metrology in Highly Correlated Input Spaces (student)
PKS Prakash, Peter Hung, Seán McLoone, National University of Ireland Maynooth; Andrea Schirru, University of Pavia

11:50
2.5 Rules of Automation for 200mm Semiconductor Manufacturing Environment
Harald Heinrich, Johannes Sturm, Infineon Technologies; Arthur Deutschländer, University of Applied Science Straslund

12:15 Networking Lunch (Meeting Room 1A)
Session 3 - Defect Inspection [Meeting Room 2B]

Chairs: Kazunori Nemoto, Hitachi Hi-Tech; Oliver Patterson, IBM; Dieter Rathei, D R Yield

Defect inspection, yield analysis and optimization are integral components in the development and manufacture of semiconductor devices. Defect inspection takes place in several areas of the fab, ranging from initial inspection of ultra thin films to final inspection of scribed die. This session will review several innovative techniques to detect and reduce defects in varied processes in semiconductor manufacturing.

1:30

3.1 Post Cu CMP Cleaning Process Evaluation for 32nm and 22nm Technology Nodes
Wei-Tsu Tseng, Donald Canaperi, Adam Ticknor, Vamsi Devarapalli, Leo Tai, Laertis Economikos Christine Bunke, Matthew Angyal, James MacDougal, Jennifer Muncy, Xiaomeng Chen, IBM Semiconductor R&D Center; John Zhang, STMicroelectronics, Qiang Fang, Jianping Zheng, GLOBALFOUNDRIES

1:55

3.2 Bevel RIE Application to Reduce Defectivity in Copper BEOL Processing
Christine Bunke, Thomas Houghton, Kenneth Bandy, IBM; George Stojakovic, Grace Fang, Lam Research Corporation

2:20

3.3 Defect Inspection Challenges and Solutions for Ultra-Thin SOI
Roland Brun, Cecile Moulin, Walter Schwarzenbach, SOITEC; Gerhard Bast, Victor Aristov, Alexander Belyaev, KLA-Tencor Corporation

2:45

3.4 Automated Optical Inspection for Die Prep
Xue Mei, Nital S. Patel, Baris Bicen, Simranjit Khalsa, Intel Corporation

3:10 Break [Sponsored by ATMI]

Session 4 - Advanced Metrology I (Meeting Room 2A) [sponsored by FEI Company]

Chairs: Dick James, Chipworks; Alok Vaid, GLOBALFOUNDRIES

Advanced semiconductor manufacturing demands advanced metrology techniques. This session details some new reflectometry, ellipsometry, scatterometry, X-ray and thermal wave use cases.

1:30

4.1 Optical Metrology of Thickness and Indium Composition of Epitaxial InxGa1-xAs layers on Si Substrates
Niamh Waldron, Tommaso Orzali, Matty Caymax, Naoto Horiguchi, imec; Youseung Jin, TaeHyun Park, Zhiming Jiang, SangHyun Han, KLA–Tencor Corporation

1:55

4.2 Measurement Strategy for Dielectric Ultra-Thin Film Characterization by Vacuum Ultra-Violet Reflectometry
Georg Roeder, Martin Schellenberger, Lothar Pfitzner, Fraunhofer Institute for Integrated Systems and Device Technology (IISB); Thomas Gumprecht, Erlangen Graduate School in Advanced Optical Technology (SAOT) and IISB

2:20

4.3 Automated TEM Metrology in Characterization of Si Devices
M. Strauss, A. Genc, G. Dutrow, D.N. Horspool, L.A. Dworkin, FEI Company

2:45

4.4 Optimal Wafer Site Selection using Forward Selection Component Analysis
PKS Prakash, B. Honari, S.F. McLoone, National University of Ireland Maynooth; A. Johnston, Seagate Technology

3:10 Break [Sponsored by ATMI]
Session 5 - Emerging Technologies and Innovative Devices (Meeting Room 2B)

Chairs: Eric Eisenbraun, CNSE; Jacek Tyminski, Nikon Precision

Innovative integrated circuit functionalities continue to be integrated in semiconductor manufacture. This session presents analysis of the effects of enabling technologies, and innovative integrated circuit designs.

3:30
5.1 CMOS-integrated Geometrically Tunable Optical Filters
Damiana Lerose, Daniel Gäbler, X-FAB Semiconductor Foundries AG; Stephan Junger, Fraunhofer Institut for Integrated Circuits IIS

3:55
5.2 Detecting Arcing Events in Semiconductor Manufacturing Equipment
Scott Singlevich, Kommisetti V R Subrahmanyam, Applied Materials, Inc.

4:20
5.3 Detection, Binning and Analysis of Defects in a GaN-on-Si Process for High Brightness Light Emitting Diodes
Sandip Halder, Andy Miller, Haris Osman, Barun Dutta, imec; Christopher Jones, Antonio Mani, Syd McCance, Frank Burkeen, KLA-Tencor Corporation

Session 6 - Advanced Metrology II (Meeting Room 2A)

Chairs: Pat Gabella, The Gabella Group; Thanas Budri, Texas Instruments

Advanced semiconductor manufacturing demands advanced metrology techniques. This session details some new reflectometry, ellipsometry, scatterometry, X-ray and thermal wave use cases.

3:30
6.1 Scatterometry Measurement for SiGe AEI Sigma-Shaped Gate Structures of 28nm Technology
Yu-Wen Wang, Autumn Yeh, Pao-Chung Lin, Chin-Cheng Chien, United Microelectronics Corporation; Lanny Mihardja, Ching-Hung Bert Lin, Zhi-Qing James Xu, Chao-Yu Harvey Cheng, Sungchul Yoo, Jason Lin, Catherine Perry-Sullivan, KLA-Tencor Corporation

3:55
6.2 In-line Metrology Capability for Epitaxial Multi-stack SiGe Layers
Delphine Le Cunff, S. Couvrat, F. Abbate, STMicroelectronics

4:20
6.3 Laser Micro-Scale Thermal Wave Characterization of Heat Transport Processes in Modern Semiconductor Structures and Devices

4:45
6.4 Development of CMP Pad Using an Unpatterned Surface Inspection System

ASMC 2012 Corporate sponsors:
Session 7 - Interactive Session and Reception: This popular session provides an ideal opportunity for interaction between authors and conference attendees. During this session, participants may engage authors in in-depth discussion of a wide range of issues impacting semiconductor manufacturing, from wide range of manufacturing and technology enhancements.

Chairs: Jennifer Braggin, Entegris; Russell Dover, Brion; Dave Gross, GLOBALFOUNDRIES; Rob Pearson, Rochester Institute of Technology; Darryl Peters, Confluense; Viraj Pandit, Novellus; Thuy Tran-Quinn, IBM

7.1 Growing the Representation of Women in Leadership: A Business Imperative – IBM Microelectronics’ MINDSET initiative

7.2 Trench geometry and resist profiles from modeling of polarized optical spectra
Franz Heider, Christian Kayser, Hans G Millonig, Samrat A. Sundaraneedi; Infineon Technologies; Jeffrey W Roberts, n&k Technology

7.3 A Failure Model of Heating Filaments in Epitaxial Growth Tools
Keung Hui, Jason Mou, Taiwan Semiconductor Manufacturing Corporation

7.4 Influences of Etcher Chamber Condition on Critical-Dimension Shifts in Advanced Floating Gate Etching Process
Sheng-Yuan Chang, Yu-Chung Chen, An Chyi Wei, Hong-Ji Lee, Nan-Tzu Lian, Tathone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co., Ltd.,

7.5 The Analysis of Device Performance on a Different STI Liner Scheme (student)
Sun Jong Wang, Yonghan Rho, Sungkyunkwan University; Jun Sup Lee, Sung Hun Kim, Sung Gun Kang, Samsung Electronics

7.6 The Study of Leakage Current Performance Improvement in High Voltage Technology

7.7 Advanced Metrology and Gas Purifier Yield Improvement
Abneesh Srivastava, Entegris, Inc.

7.8 Analysis of an Effect of Perturbations in SWHM and Illuminating Optical Scheme Parameters on an Aerial Image
M.V. Borisov, D.A.Chelyubeev, V.V. Chernik, A.A. Gavrikov, D. Yu Knyazkov, P.A. Mikheev, V. I. Rakovsky, A.S. Shamaev, NANOTECH SWHL

7.9 IMPROVE Simulation Tool - Integrating Heterogeneous Simulation Modules for Semiconductor Manufacturing Processes
Nuno Almeida, João Pires, David Sora, Critical Manufacturing

7.10 A Predictive Maintenance System based on Regularization Methods for Ion-Implantation
Gian Antonio Susto, Alessandro Beghi, University of Padova; Andrea Schirru, Simone Pampuri, University of Pavia

7.11 Measuring Hydrochloric Acid and Ammonium Hydroxide Permeation in Bulk Chemical Distribution
Sung In Moon, Mark Caulfield, C.W. Extrand, Entegris, Inc.

7.12 Wafer Characterization via Sub-Nanosecond Time Correlated Single Photon and Quality Control of Counting

7.13 RTO process monitoring with inline non-contact technique
Nicolas Pic, Emmanuel Paire, Arnaud Belfy, Catherine Grosjean, Guillaume Pellegrin, Patrice Laurens, STMicroelectronics

7.14 Properties of Isolation Liner and Electrical Characteristics of High Aspect Ratio TSV in 3D Stacking Technology
DeokYoung Jung, Yong Han Ro, Sungkyunkwan University; Kwang-Jin Moon, Byung-Lyul Park, Gilheyun Choi, Ho-Kyu Kang, Chilhee Chung, Samsung Electronics Co. Ltd.

7.15 Modeling and Analysis of Integrated Planning of Production and Engineering Production Improvement
Sukgon Kim, Northern Illinois University; Reha Uzsoy, North Carolina State University

7.16 Enabling Collaborative Solutions across the Semiconductor Manufacturing Ecosystem (student)
Charles M. Weber, Jiting Yang; Portland State University; Patricia Gabella, The Gabella Group

7.17 Carbonized Surface Curing for Etch-Back Process
Sunjin Jang, In-cheol Kim, Kyu-yeo Lee, Soo-cheol Lee, In-soo Cho, Samsung Electronics Co. Ltd.; Byoung-deog Choi, Sungkyunkwan University

7.18 Maintenance Pooling to Maximize Fab Uptime and Throughput
Mike Czerniak, Alan Ifould, Michael Mooney, Edwards Ltd.; Shane Butler, National University of Ireland Maynooth

7.19 Leveraging Advanced Process Control (APC) Technology in Developing Predictive Maintenance (PdM) Systems
James Moynie, Nick Ward, Parris Hawkins, Applied Materials, Inc.

7.20 Real-time, Continuous Large Particle Monitoring for CMP Slurry Quality Control
Andy Kim, Koh Murai, P.E Mega Fluid Systems; Michael Parkin, Rashid Mavliev, Vantage Technology

7.21 A Comparison of Data Mining Methods for Yield Modeling, Chamber Matching and Virtual Metrology Applications
Deepak Sharma, Helen Armer, James Moynie, Applied Materials, Inc.

7.22 Improved Sustainability of an Existing Fab Operation through Reduced Energy Consumption
Don Yeaman, M+W Group US; Ron Rogerson, Spansion, Inc.
Session 8 - Factory Optimization (Meeting Room 2B) – (Sponsored by CH2M HILL)
Chairs: Sumita Basu, Intel Corporation; Paul Werbaneth, Semiconductor equipment and manufacturing is increasingly complex and driven by strict economic constraints. It is vital for IC production to improve efficiency, control costs, and be good environmental stewards. This session covers novel solutions for environmental and material handling challenges.

9:35
8.1 Assessing the Impact of the 450mm Wafer Size Transition on Manufacturing Facility Automated Material Handling Systems
Larry Hennessy, CH2M HILL

8.2 Operator-Free Exception Measurement Logistics for a Highly Automated 200mm Semiconductor Manufacturing Environment
Andrea Bannert, Frank Heinlein, Matthias Adam, Infineon Technologies Dresden GmbH; Kay Manja, Systema GmbH

10:00
8.3 Improving Eco-Efficiency via elimination of greenhouse gases from semiconductor dry cleaning processes

10:25 Break

10:45
8.4 Green Mode: Equipment Interface to Optimize Semiconductor SubFab Utility Consumption
Adrienne Pierce, Edwards Vacuum Inc.; Val Parks, GLOBALFOUNDRIES

11:10
8.5 Industry Approach to the Conflict Minerals Legislation
Jared Connors, Intel Corporation

12:00 Boxed Lunch (Sponsored by Synopsys)

Session 9 - Advanced Process Control (Meeting Room 2A)
Chairs: Agnès Roussy, EMSE; Raymond van Roijen, IBM
The demand for high quality and yield is a constant driver for advanced process development and control techniques. This session covers innovation in process controls and shows how predictive maintenance and virtual metrology will impact manufacturing.

9:35
9.1 Tribological, Thermal, and Kinetic Attributes of 300 Vs. 450 mm Chemical Mechanical Planarization Processes (student)
Yubo Jiao, Xiaoyan Liao, Changhong Wu, University of Arizona; Yun Zhuang, Siannie Theng, Yasa Sampurno, Ara Philipossian, Araca, Inc.; Michael Goldstein, Intel Corporation

10:00
9.2 A Comprehensive Approach to Process Control

10:25 Break

10:45
9.3 An Integrated Advanced Process Control on RTP Gate Oxide Thickness and Feed-forward Implant Compensation in Mass Production
Zhang Jian, Liu Shi Xiang, Lei Ming, Ling Syau Yun, Lim Ming Chou, K. Suresh, Tan Miow Chin, Vish Srinivasan, Peter Benyon, GLOBALFOUNDRIES Singapore Pte. Ltd

11:10
9.4 Framework for Integration of Virtual Metrology and Predictive Maintenance

11:35
9.5 Optimal Tuning of Epitaxy Pyrometers (student)
Gian Antonio Susto, Alessandro Beghi, University of Padova; Andrea Schirru, Simone Pampuri, University of Pavia

12:00 Boxed Lunch (Sponsored by Synopsys)
Session 10 - Equipment and Materials Productivity (Meeting Room 2B)

Chairs: Scott Lantz, Intel Corporation; Christopher Long, IBM Research

The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity. Optimizing equipment performance will help improve fab metrics, minimize wafer costs and maximize competitiveness. Papers in this session will review ideas and successes to help optimize equipment utilization, improve predictive modeling of fab operations, and tool performance.

12:30
10.1 Experimental Investigation and Manufacturing Solution of the Rapid Thermal Process Induced Overlay Residues
Weihua Tong, Xu Li, Lei Huang, K. Suresh, Miowchin Tan, Vish Srinivasan, Peter Benyon, Sung Kim, Olivier Vatel, GLOBALFOUNDRIES

12:55
10.2 TiN Metal Hardmask Etch Residue Removal with Mask Pullback and Complete Mask Removal for Cu Dual Damascene Device
Hua Cui, EKC Technology, DuPont Electronic Technologies

1:20
10.3 Lithography Challenges and Solutions for MEMS/LED/ABS Applications
Hamid R. Kharram, Nikon Precision; Junpei Fukui, Susumu Hagiwara, Shigeo Mizoroke, Makoto Osanai, Tetsuji Onuki, Nikon Engineering; Volker Berghof, First Sensor AG

1:45 Break

2:05
10.4 A Novel Approach to Optical Wafer Pre-Alignment Using Innovative Ranging Edge Detectors
Thomas Jerman, Bright Red Systems GmbH; Walter Leitgeb, Infineon Technologies AG

2:30
10.5 Humidity Rise Purge in Micro-Environments
Sung In Moon, C.W. Extrand, Entegris, Inc.

Session 11 - Advanced Patterning and Design for Manufacturability (Meeting Room 2A)

Chairs: Holly Magoon, Nikon Precision; Mike McIntyre, GLOBALFOUNDRIES

IC production today requires innovative lithography design and manufacturing techniques. Papers in this informative session include collaborative efforts between chip makers and equipment suppliers discussing leading-edge solutions for advanced lithography techniques such as double patterning. Recent developments in Design for Manufacturability will also be highlighted.

12:30
11.1 Enhanced Process Control of Pitch Split Double Patterning by use of CD-SEM critical dimension uniformity and local overlay metrics
Scott Halle, Chiew-seng Koay, Matthew Colburn, Shyng-Tsong Chen, IBM; Shoji Hotta, Takeshi Kato, Hitachi High-Technologies Corporation, Atsuko Yamaguchi, Hitachi Ltd.,

12:55
11.2 Design Based Classification for Process Window Defect Characterization of BEOL ADI Layers
YoungSu Kim, Young Hun Kwon, Ki Ho Kim, Tae Woong Hwang, Samsung Electronics Co., Ltd.; Raghav Babulnath, Colin Yu, Paresh Desai, KLA-Tencor Corporation

1:20
11.3 A Self-aligned Double Patterning Technology Using TiN as the Sidewall Spacer
Yuan-Chieh Chiu, Shu-Sheng Yu, Fang-Hao Hsu, Hong-Ji Lee, Nan-Tzu Lian, Tahnge Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co., Ltd.

1:45 Break

2:05
Lithography Challenges – A Technology Update
Stefan Wurm, Director of Lithography, SEMATECH
The 23rd Annual SEMI Advanced Semiconductor Manufacturing Conference - ASMC 2012
Wednesday, May 16, 2012 (day two)

Session 12 - Equipment and Materials Productivity (Meeting Room 2B)
Chairs: Johann Massoner, Infineon; Naomi Yoshida, Applied Materials
The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity. Optimizing equipment performance will help improve fab metrics, minimize wafer costs and maximize competitiveness. Papers in this session will review ideas and successes to help optimize equipment utilization, improve predictive modeling of fab operations, and tool performance.

2:55
12.1 Enhancements in Resizing Single Crystalline Silicon Wafers up to 450 mm by using Thermal Laser Separation
M. Koitzsch, D. Lewke, M. Schellenberger, L. Pfitzner, H. Ryssel, Fraunhofer Institute of Integrated Systems and Device Technology (IISB); H.-U. Zühlke, JENOPTIK Automatisierungstechnik GmbH

3:20
12.2 Modifying Mask Blank Manufacturing to Incorporate Cleaning and Deposition Experimentation
Milton Godwin, Anne Rudack, SEMATECH

3:45
12.3 High-k/Metal Gates in Leading Edge Silicon Devices
Dick James, Chipworks

4:10 Break

Session 13 - Equipment Performance (Meeting Room 2A)
Chairs: Jan Rothe, GLOBALFOUNDRIES; Brett Williams, ON Semiconductor
The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity. Optimizing equipment performance will help improve fab metrics, minimize wafer costs and maximize competitiveness. Papers in this session will review ideas and successes to help optimize equipment utilization, improve predictive modeling of fab operations, and tool performance.

2:55
13.1 The Hidden Productivity: How to Get More Out of Your Equipment
Adar Kalir, Yair Nahun, Andy Sharon, Intel Corporation

3:20
13.2 Efficient FDC based on Hierarchical Tool Condition Monitoring Scheme (student)
Jakey Blue, Agnès Roussy, EMSE-CMP; Alexis Thieullen, STMicroelectronics and LSIS-University Aix-Marseille; Jacques Pinaton, STMicroelectronics

3:45
13.3 Predictive Sampling Approach to Dynamically Optimize Defect Density Control Operations
M. Pfeffer, R. Oechsner, L. Pfitzner, Fraunhofer Institute for Integrated Systems and Device Technology (IISB); S. Eckert, A. Hartmann, H. Gold, G. Biebl, J. Kaspar, Infineon Technologies

4:10 Break

4:30-5:45 Panel Discussion: Competing for R&D Dollars: Funding the Future (Meeting Room 2B)
As advances in materials and process technology continue, the semiconductor manufacturing industry is faced with difficult challenges concerning costs. In order to stay on the productivity curve, companies must address several critical technology issues. However, with limited R&D dollars, it is unclear how wafer size transition, next node scaling, new transistor technology, and 3D IC will be funded. A limited number of companies will pursue 450mm, but many more are looking at 3D ICs. Add to this the challenge of EUV. Where will IC companies put their investment? What about their suppliers? Should the focus be on 450mm conversion or advanced process technologies? Who will ultimately pay the price? Where does the ROI end? A panel of industry experts addresses these and other related productivity and technology challenges facing the global chip-making community.
Moderator: Peter Singer, Editor-in-Chief, Solid State Technology. Panelists: David Bennett, VP Alliances, GLOBALFOUNDRIES; Noreen Harned, VP Marketing, ASML; Subramanian Iyer, IBM Fellow, IBM Systems & Technology Group; Nag Patibandla, Ph.D., Sr. Director (Office of CTO), Applied Materials; Risto Puhakka, President, VLSI Research.

6:00-7:00 Networking Reception – Canfield Casino, Saratoga Springs, NY
Reception Sponsors:
Session 14 - Defect Inspection II [Meeting Room 2B]
Chair: Jeff Barnum, KLA-Tencor; Bill Miller, IBM Microelectronics
Defect inspection, yield analysis and optimization are integral components in the development and manufacture of semiconductor devices. This session will feature papers on e-beam inspection used for defect inspection of advanced technologies and improving defect inspection efficiency.

9:05
14.1 E-Beam Inspection for Combination Use of Defect Detection and CDU Measurement
Carol Boye, Theodorus Standaert, IBM Corporation; Fei Wang, Chris Lei, Shih-tsung Chen, Jack Jau, Derek Tomlinson, Hermes Microvision Inc.

9:30
14.2 Photo Cell Monitoring Inspection Methodology Employing a Complementary Strategy of Advanced Darkfield and High Sensitivity Brightfield Inspection Tools
Jyn Hao Syu, Chen Chiz Lin, P Y Chiang, Nagus Chen, United Microelectronics Corporation; Henry Yang, Eros Huang, Harvey Cheng, Mahatma Lin, Kan Chen, Jun Lang, KLA-Tencor Corporation

9:55
14.3 Use of 22 nm Litho SEM Non-Visual Defect Data as a Process Quality Indicator
Carol A. Boye, Christopher J. Penny, Joe Connors, Donna Boyles, IBM; Rajesh Ghaskadvi, Roland Hahn, KLA-Tencor Corporation

10:20 Break

10:35
14.4 E-Beam Inspection for Detection of Sub-Design Rule Physical Defects
Oliver D. Patterson, Julie Lee, IBM R&D Center; Dave Salvador, GLOBALFOUNDRIES; Chris Lei, Hermes Microvision Inc.

11:00
14.5 A Memory Volume Diagnostics Methodology to Facilitate Production Yield Learning With Embedded Memories
Ruth Farrugia, Stephane LeComte, Tammy Dong Lei Zheng, ST-Ericsson; Florent Garait, Christophe Giroud, Eric Faehn, STMicroelectronics; Christophe Suzor, Sagar A. Kekare, Synopsys, Inc.

11:20 Keynote: Risto Puhakka, President, VLSI Research: IC Market Analysis and Forecast (Meeting Room 2B)
12:20 Closing Remarks

Session 15 - 3D/Through Silicon Via (TSV) [Meeting Room 2A]
Chair: Hamid Khorraram, Nikon Precision; James Lu, RPI
Very large Scale Integration motivates 3D integrated circuit architectures. This session presents complexities of Through Silicon Via techniques supporting 3D designs.

9:05
15.1 TSV RF de-embedding Method and Modeling for 3DIC
Hsiao-Tsung Yen, Yu-ling Lin, Clark Hu, S.B. Jan, Chi-Chun Hsieh, M.F. Chen, Chin-Wei Kuo, Sean Chen, Min-Chie Jeng, Taiwan Semiconductor Manufacturing Company, Ltd.

9:30
15.2 Evaluation of Fabrication Process for a Novel Chip-to-wafer (C2W) 3D Integration Approach Using an Alignment Template
Dingyou Zhang, James Jian-Qiang Lu, Rensselaer Polytechnic Institute (student)

9:55
15.3 New Method of WLCSP for Process Optimization and Reliability Prediction
Chin-Yu Ku, Wei-Chi Huang, Young-Chang Lien, Ming-Chih Yew, Po-Yao Lin, Hsiu-Mei Yu, Taiwan Semiconductor Manufacturing Company, Ltd.

10:20 Break

10:35
15.4 New Polymerizing Chemistries for Through-Silicon Via Etching (3D/TSV) (student)
William Nicoll, Eric Eisenbraun, University at Albany; Christian Dussarrat, Curtis Anderson, Rahul Gupta, Air Liquide

11:00
15.5 Decoupling Capacitor Modeling and Characterization for Power Supply Noise in 3D Systems
Kenneth Rose, James Jian-Qiang Lu, Rensselaer Polytechnic Institute; Zheng Xu, IBM Microelectronics; Xiaoxiong Gu, Michael Scheuermann, Bucknell C. Webb, John Knickerbocker, IBM T.J. Watson Research Center

11:20 Keynote: Risto Puhakka, President, VLSI Research: IC Market Analysis and Forecast (Meeting Room 2B)
12:20 Closing Remarks

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