TRUE: A New Metric for ATE Cost Effectiveness

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Teradyne Business segments

Semiconductor Test
System-On-Chip (SOC) Test
• Leading wireless, mixed signal, microcontroller and performance analog test systems
• Largest installed base with over 9,000 systems installed at IDM and OSAT customers

Memory Test
• Highest Throughput Flash and High Speed DRAM Solutions

Wireless Products
• Unique tester architecture focused on production test of mobile devices
• Products deliver highest throughput and shortest time to market
• Serves ~$1B+ wireless product test market, growing 8% - 10% per year

Systems Test Group
Defense & Aerospace Board Test
• Defacto standard for DoD digital test
Storage Test
• Industry’s most productive 2.5” HDD Systems
Commercial Board Test
• Patented low voltage test technology delivers highest yield in-circuit board test

Annual Revenue (1)

<table>
<thead>
<tr>
<th>Year</th>
<th>Revenue</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
<td>$1,038M</td>
</tr>
<tr>
<td>2008</td>
<td>$1,048M</td>
</tr>
<tr>
<td>2009</td>
<td>$777M</td>
</tr>
<tr>
<td>2010</td>
<td>$1,566M</td>
</tr>
<tr>
<td>2011</td>
<td>$1,429M</td>
</tr>
<tr>
<td>2012</td>
<td>$1,657M</td>
</tr>
</tbody>
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(1) Revenues exclude DS which was divested in Q1’11
The 3D IC Challenge to Test

- Increased wafer sort test coverage to get to KGD quality levels to avoid excessive scrap costs for stacks
- Increased number of in process test insertions for partially completed die stacks
- Excessive test cost could preclude application of 3D-IC in cost sensitive, high volume markets
  - Memory on Logic (Application Processors)
  - Heterogeneous 3D-IC for mobile and wearable electronics
- Innovation is required to deliver a step function reduction in test cost for the 3D-IC era
**Potential Strategies to Reduce Cost of Test**

- **Reduce COT**
  - Reduce Test Cell Cost
  - Increase UPH
  - Increase Utilization
  - Reduce # of insertions

- **Increase UPH**
  - Higher Site Count
  - Reduce Test Time

- **Reduce Test Cell Cost**
  - Reduce CAPEX per site
  - BIST / BOST / Structural test

- **Increase Utilization**
  - Increase PTE
  - Concurrent Test
  - Eliminate ATE overhead
  - Adaptive Test

**Impact**

- Achieved reduction of 50% to 90% over past 5 years
  - Potential for future reductions is lower

- Impacts device AQL
  - 25% to 50% of CAPEX

- Relevant for ||8
  - 1% increase → 30% throughput above 16 sites

- Requires DFT investment
  - ~25 to 40% for CT enabled devices

- Datalog, DSP, Inst setup
  - ~10 to 20% of Test Time

- Relatively unproven
  - ~10 to 20% of Test Time

**How much is possible here?**
Equipment Utilization

“Classic” Definition of Utilization

25 Test Cells

- 5 Test Cells Idle / Down
- 2 cells waiting for Material
- 17 cells operating

68% Utilization (at this moment)
Average Utilization is integration over a time period
First Step: Optimize “dead time” in the test cell

- Setup tester, initiate test
- Testing the devices
- Datalogging
- Index Time

Optimizations
- Faster Computers
- Optimized SW

- ~80% → 90%
- Background Datalog
- Better at Wafer test
- More efficient handlers
But How Efficient is Device Test?

If each test takes 1 second, Tester Resource Utilization Efficiency ~ 35%
TRUE = Tester Resource Utilization Efficiency

• 35% TRUE for the example on previous slide
• Is that a good or bad number?
  – A low baseline number is an opportunity for significant improvement
• What does a higher number mean?
  – More fully utilizing capital investment
  – Optimizing configurations to requirements
Multi-Station
Index Parallel Testing

Ismeca NX16 Turret Handler

Typically used for low pin count analog dominant devices

“Typical” Specs
Minimum dwell time = 80-100ms
Index Time = 80ms to 200ms
Number of stations: 16 to 32
Test Stations: 1 to 4

Diagram courtesy of Ismeca Semiconductor
Throughput
275ms (test time)
3x80ms (non-test-dwell)
515ms (for 4 devices)
129ms/device = 28K UPH

Test List (275ms)
Test 1.0 Kelvin
Test 2.0 Iddq
Test 3.0 Idd/I
Test 4.0 Vth+
Test 5.0 Vth-
Test 6.0 Delta Vth
Test 7.0 Drop 10mA
Test 8.0 Drop 150mA
Test 9.0 Drop 300mA
Test 10.0 PSRR
Test 11.0 Load Reg
Test 12.0 I short

CAPEX: 1.0
COT: 1.0
TRUE: 16%

“Classic” Quad Site

Turret Handler

“Classic”
Quad Site

Throughput
80ms (test time)
0ms (non-test-dwell)
80ms (for 1 device)
45K UPH

CAPEX: 0.5x
COT: 0.31x
TRUE: 41%

69% lower COT

Index Parallel Test

Turret Handler

Low I VI
High I VI
Diff VM

Index Parallel Test

Turret Handler

Low I VI
Low I VI
High I VI
Diff VM
Applying the Index Parallel technique to wafer sort KGD

**“Classic Multisite”**
- 4 copies of resources
- Test time = ~1.2x SS

**“Index Multisite”**
- 2 copies of resources
- Test time = ~0.6x2 SS
- 2x more efficient
- 2x touchdowns

Appropriate for simple, low pin count die in heterogeneous stacks

Practical Implementation depends on ATE Architecture that supports running different test flows on a per site basis
MCU: TRUE Test Case

Serial Test Flow

- O/S 0.5s
- Scan 1.0s
- Mem 5.0s
- Func 3.0s
- DAC/ADC 2.5s

Concurrent Test Flow

- O/S
- Scan
- Mem
- Func
- DAC/ADC

Concurrent Test Flow with Unique Site Flows

- O/S
- Scan
- Mem
- Func
- DAC
- ADC

Practical Implementation depends on ATE Architecture that supports managing tests as blocks without modification

TT: 12
Capex: 1.0
COT: 1.0
TRUE: 53%

TT: 7.0
Capex: 1.0
COT: 0.58
TRUE: 83%

TT: 7.5
Capex: 0.8
COT: 0.51
TRUE: 85%
PMIC: TRUE Test Case

Test Plan

| O / S       | 0.25s |
| Low Power Tests | 1.0s |
| High Power Tests | 1.5s |
| Digital Timing Tests | 0.5s |

Per Pin Architecture

Matrix Architecture

Practical Implementation depends on ATE Architecture that supports low cost pin multifunction pin with matrix capability
TRUE On the Test Floor

25 Test Cells

5 Test Cells Idle / Down
2 cells waiting for Material
17 cells operating
  7 at 50% TRUE
  6 at 40% TRUE
  4 at 30% TRUE
68% Utilization
28% TRUE Utilization (68% x 41%)

• Testers can be enhanced to provide real time reporting of TRUE to Test Floor management software
• TRUE statistics could be used to identify low efficiency applications
  • Increase site count
  • Increase concurrency
  • Redeploy options across test floor
Using TRUE as a tool

- **IC Design**
  - Evaluate the impact of incorporating independent control and visibility for major functional blocks to enable concurrent test

- **Tester Selection**
  - Evaluate economic impact of features to support index parallel, Concurrent and unique site flow

- **Test Solution Development**
  - Identify optimal site count and tester configuration for new devices

- **Test Floor Operations**
  - Identify test solutions with offensively low TRUE for improvements (modify tester config, increase site count, optimize test program flow)

- **ATE Design**
  - Develop tools to predict TRUE for new test solutions
  - Develop tools to monitor and report TRUE to test floor management
3D-IC requires a Step Function Reduction in Test Cost

- Devices require more test to avoid excessive scrap costs
- Many paths to reduce cost of test have already been travelled. The same tricks are not enough.
- TRUE offers a method to tap the unutilized potential of installed capital
- TRUE metrics provide a tool to find problems and improve test tests on SOC, SIP and 3D-IC devices