More Than Moore’s - 3D-IC Economics and Design Enablement

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Outline

• Semiconductor Challenges – More Moore or beyond Moore?
• 3D/2.5D Advantages and Challenges
• Design enablement for 2.5D/3D realization
• Conclusion
More Moore? Or more than Moore?
It’s a bimodal world!
More Moore’s

- **Application Requirements**: Bandwidth, Power, Reduced Area
- **Obvious Solution**: Jump to next process node: 20nm/14nm/10nm
  - Yield?
  - Shrinking Analog to small geometries: Variability, Leakage …
  - Reuse of IP built on older nodes? Risk? T2M?
  - **COST**?

### Table

<table>
<thead>
<tr>
<th></th>
<th>32 / 28nm node</th>
<th>22 / 20nm node</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fab construction</strong></td>
<td>$3B</td>
<td>$4B – 7B</td>
</tr>
<tr>
<td><strong>Process R&amp;D</strong></td>
<td>$1.2B</td>
<td>$2.1B – 3B</td>
</tr>
<tr>
<td><strong>Design cost</strong></td>
<td>$50M – 90M</td>
<td>$120M – 500M</td>
</tr>
<tr>
<td><strong>Mask set</strong></td>
<td>$2M – 3M</td>
<td>$5M – 8M</td>
</tr>
<tr>
<td><strong>EDA enablement</strong></td>
<td>$400M – 500M</td>
<td>$800M – 1.2B</td>
</tr>
</tbody>
</table>

*Source: IBS, May 2011*

**Design cost:** ~$200M

Need product opportunity > $1B

*Source: IBS 2012*
3D-IC is a bridge for “More Than Moore” solutions

Source: UBM TechInsights (EETimes, October 2012, May 2011)
2.5D/3D-IC Advantages

- De-Risk SOC implementation and better T2M
  - Re-use of silicon proven Analog/MS/PHY
  - Only port the digital to advanced process nodes

- Reduce power through Wide I/O, and others alike

- Improve yield for larger die at advanced nodes

- Increase system performance while Reduce Form factor by integrating heterogeneous dies in single package
3D-IC Challenges
Challenges in business model and technology

• Business:
  – Who does what?
  – Who owns what?
  – Standardization? Who is the king?

• Design enablement (tools) and methodology
• Thermal management
• Test strategies
Thermal Challenges in Mobile Application

**THERMAL - WIDE IO VS POP**

<table>
<thead>
<tr>
<th>Thermal Simulation</th>
<th>Tj limit</th>
<th>85°C</th>
<th>95°C</th>
<th>105°C</th>
<th>125°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PoP</td>
<td></td>
<td>4</td>
<td>14</td>
<td>50</td>
<td>0.3</td>
</tr>
<tr>
<td>WideIO</td>
<td></td>
<td>0.08</td>
<td>0.21</td>
<td>0.44</td>
<td>0.28</td>
</tr>
</tbody>
</table>

- 4” smartphone mechanics, typical chipset
- Application of 10W SOC perf peak starting from 2W SOC steady state

**Observation:** POP thermal performance better than WideIO
- TSV requires silicon die to be reduced to 50-70um, which results in poor lateral heat distribution
- Thermally tightly coupled WideIO DRAM heats up much faster than in POP
- WideIO DRAM performance reduced at Tj > 85°C due to increased refresh cycle requirements

*Source: ST-Ericson*
3D DFT Challenges

• **Pre-bond test**
  – Focus on die-internal circuitry
  – Original thick or thinned-down wafer
  – Probe access at DUT
  – Probe on micro-bumps or dedicated pads

• **Mid-bond / post-bond / final tests**
  – Focus on interconnects and die-internal circuitry
  – Test access (probe or socket) at bottom die
  – Require DFT to propagate test stimuli / responses up / down through stack
  – Requirements
    – Modular test: core, die, interconnect
    – TestTurn: test up till this die
    – TestElevator: test higher-up die
3D/2.5D Design Enablement and Methodology
Short-, medium-, and long-term path to 3D-IC
EDA work starts at least 3-4 years earlier

Si Partitioning with TSV Interposer
- Market: FPGA
- Xilinx in 2010
- 2011-2012

Memory Cube with TSVs
- MARKET: Server and computing
- IBM and Micron
- 2012-2013

Logic + memory w/ 2.5D TSV Interposer
- MARKET: GPU, gaming console
- ST testchip in 2010
- 2013-2014

Wide IO + Logic with TSVs
- MARKET: Mobile, tablet, gaming processors
- ST-E / LETI WIOMING in 2011
- 2014-2015

High-performance computing
- MARKET: CPU, MCMs etc
- ST-E / LETI WIOMING in 2011
- ~ 2015

Short: Standards, ecosystem, cost
Medium
Long
So what changes with 3D-IC in EDA world?
Revamped EDA requirements

- Package silicon co-design
- New layout layers (e.g. alignments)
- New layout layer (e.g. Back-side RDL)
- New extraction features (e.g. TSV)
- Inter-processes DRC/LVS
- Cross-die, power and signal integrity
- Cross-die timing closure
- Thermal analysis and mechanical constraints
- Manufacture test

Courtesy: Qualcomm
Cadence 3D-IC Integrated Solution

Complete Implementation Platforms for flexible Entry Point and Seamless Co-design
Using OpenAccess, EDI, Virtuoso each has dedicated 3DIC functions that work together, plus co-design with Cadence SiP tools for complete End to End implementation including early stage system exploration and feasibility

Full Spectrum Analysis Capability
RC/ET DFT and ATPG for 3DIC
EPS/ETS/QRC Digital Analysis Tool
Virtuoso Based Full Spice Simulation Capacity
SiP/Sigrity based Extraction, SI, and PI System/Packetage Analysis
PowerDC Thermal Analysis

Ecosystem partnership and Real Experiences/Proof Points
Cadence has been working with ecosystem partners since 2007 on 3DIC
8 test chips completed and 1 production chip done
Several projects ongoing
3D/2.5D Solutions with flexible Implementation Cockpits

SOC entry point

Virtuoso™

Sigrity

Allegro™

EDI

PVS

QRC

ET

RC

Wide IO

Virtuoso entry point

Virtuoso

Sigrity

Allegro™

QRC

PVS

Spectre

UltraSim™

ED1

ETS

EPS

ET

Wide IO

System entry point

Allegro

Sigrity

Spectre™

UltraSim

PVS

EDI, Virtuoso

ETS

EPS

RC

Wide IO

QRC

Wide IO

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Example: 2.5D Silicon Interposer

Die3, TC2 – Logic Die. Die 1,2: Memory Dies;
Example Design and implementation flow

Die-interposer-package co-design

Logic die design for test

Logic die implementation

3rd party memory modification

Interposer design and implementation
Example Design and implementation flow

Die-interposer-package co-design

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Interposer design and implementation
Example Design and implementation flow

Die-interposer-package co-design

Interposer, die abstract import
- Package driven c4-bump assignment optimization

Logic die implementation
- Logic die design for test

Die-interposer-package co-design

xctePI IO Interconnect Model Extraction Diagram

Electrical Performance Assessment

What-if Analysis

Model Generation

SPICE Netlist

SystemSI

SSN
Example Design and implementation flow

Die-interposer-package co-design

Logic die design for test

Logic die implementation

3rd party memory modification

Interposer design and implementation
Example Design and implementation flow

Die-interposer-package co-design

Logic die design for test
- DFT insertion for interposer interconnect test.
- ATPG
- Tool involved: RC, ET,

Support IEEE 1500, IEEE 1149.1, etc
Example Design and implementation flow

Die-interposer-package co-design

Logic die design for test

Logic die implementation

3rd party memory modification

Interposer design and implementation
Example Design and implementation flow

Die-interposer-package co-design

Logic die design for test

Logic die implementation
1. P&R (Stress Aware)
2. Micro bump creation/connection
3. Physical Verification (DRC/LVS)

Tool involved
• EDI, PVS,
Example Design and implementation flow

1. Die-interposer-package co-design
2. Logic die design for test
3. Logic die implementation
4. Interposer design and implementation
5. 3rd party memory modification
Example Design and implementation flow

1. Die-interposer-package co-design
2. Logic die design for test
3. Logic die implementation
4. 3rd party memory modification

Interposer design and implementation
Example Design and implementation flow

1. Interposer P&R (Using EDI or Virtuoso)
2. TSV Placement (Sync with SiP)
3. Interposer Physical Verification (DRC/LVS)

Tool involved:
- EDI, Virtuoso, PVS
Example Analysis and signoff flow

- Inter-die DRC/LVS
- Extraction
- Timing/Power Analysis and signoff
- SSO/SSN Analysis for PI/SI signoff
- Thermal Analysis
Example Analysis and signoff flow

1. Inter-die DRC/LVS
2. Extraction
   - Timing/Power Analysis and signoff
   - SSO/SSN Analysis for PI/SI signoff
3. Thermal Analysis
Example Analysis and signoff flow

Inter-die DRC/LVS
- Micro bump alignment check (DRC)
- Inter-die connective check (LVS)

Tool involved:
- PVS
- 3rd party memory modification

DRC Check Flow Chart

- Stack die config.xml
- Inter-die DRC Deck
- Signal map file .v
- Add layout path
- Stack die configuration
- Set signal map file

Output:
- TC2_APIlayer GDS
- ddd1_module1 GDS
- ddd1_module2 GDS
- Interposer GDS
- DRC Report
- PVS
- Debug
Example Analysis and signoff flow

- Inter-die DRC/LVS
- Extraction
  - Timing/Power Analysis and signoff
  - SSO/SSN Analysis for PI/SI signoff
- Thermal Analysis
Example Analysis and signoff flow

- **Inter-die DRC/LVS**
- **Extraction**
  - Interposer Extraction by QRC
  - Interposer Extraction by Sigrity/XcitePI
  - Package Extraction by Sigrity/XtractIM
  - Tool involved: QRC, Sigrity/XcitePI, Sigrity/XtractIM
- **Thermal Analysis**

**Tool involved:** QRC, Sigrity/XcitePI, Sigrity/XtractIM
Example Analysis and signoff flow

Inter-die DRC/LVS

Extraction
- Interposer Extraction by QRC
- Interposer Extraction by Sigrity/XcитеPI
- Package Extraction by Sigrity/XtractIM

Tool involved
- QRC, Sigrity/XcитеPI, Sigrity/XtractIM

PVS2QRC Flow

ICT w/ TSV
- QRC Techgen
  - arcTechFile

IPF w/ micro-bump
- EDI
  - GDS
  - PVS LVS
  - PVS DB

QRC
- Interposer SPEF

ETS

Analysis

Timing

Analysis and signoff
Example Analysis and signoff flow

- Inter-die DRC/LVS
- Extraction
  - Timing/Power Analysis and signoff
  - SSO/SSN Analysis for PI/SI signoff
- Thermal Analysis
Example Analysis and signoff flow

**Inter-die DRC/LVS**

**Extraction**

**Timing/Power Analysis and signoff**
- Include SPEF output of TC2 and Interposer to run ETS for Timing signoff
- Include Package RLC model, TC2 and Interposer layout to run EPS for EM/IR analysis
- Provide ECO (such as Decap, power Gating, etc) to EDI
  - Tool involved: **ETS, EPS**

**SSO/SSN Analysis for PI/SI signoff**
Example Analysis and signoff flow

**Timing/Power Analysis and signoff**

- Include SPEF output of TC2 and Interposer to run ETS for Timing signoff
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- Provide ECO (such as Decap, power Gating, etc) to EDI
  - Tool involved: ETS, EPS
Example Analysis and signoff flow

- **Thermal Analysis**
- **SSO/SSN Analysis** for PI/SI signoff
- **Inter-die DRC/LVS Extraction**

**Timing/Power Analysis and signoff**

- Include SPEF output of TC2 and Interposer to run ETS for Timing signoff
- Include Package RLC model, TC2 and Interposer layout to run EPS for EM/IR analysis
- Provide ECO (such as Decap, power Gating, etc) to EDI

**Tool involved**

- ETS, EPS
Example Analysis and signoff flow

- Inter-die DRC/LVS
- Extraction
  - Timing/Power Analysis and signoff
  - SSO/SSN Analysis for PI/SI signoff
- Thermal Analysis
Example Analysis and signoff flow

Inter-die DRC/LVS

Extraction

Timing/Power Analysis and signoff

Thermal Analysis

SSO/SSN Analysis for PI/SI signoff

- Include IBIS of TC2 and DRAM, as well as the Interposer and package RLC model, to run SystemSI
- Provide Feedback to SiP/Virtuoso
- Tool involved: Sigrity/T2B, Sigrity/SSI
Example Analysis and signoff flow

**Thermal Analysis**

**XcitePI IO Interconnect Model Extraction**

Diagram:

- LEF/DEF
- GDS
- GUI

**Model Generation**

**What-if Analysis**

**Electrical Performance Assessment**

**SPICE Netlist**

**SystemSI**

**SSO/SSN Analysis for PI/SI signoff**

- Include IBIS of TC2 and DRAM, as well as the Interposer and package RLC model, to run SystemSI
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Example Analysis and signoff flow

SSO/SSN Analysis for PI/SI signoff
 Include IBIS of TC2 and DRAM, as well as the Interposer and package RLC model, to run SystemSI
 Provide Feedback to SiP/Virtuoso Tool involved Sigrity/T2B, Sigrity/SSI
Example Analysis and signoff flow

- Inter-die DRC/LVS
- Extraction
  - Timing/Power Analysis and signoff
  - SSO/SSN Analysis for PI/SI signoff

- Thermal Analysis
Example Analysis and signoff flow

Inter-die DRC/LVS

Extraction

Timing/Power Analysis and signoff

SSO/SSN Analysis for PI/SI signoff

Thermal Analysis

- Die level Power Map Generation
- Integrate PKG and Interpose Design DB
- Thermal Analysis
- Die level temperature Dependent IR Analysis

Tool involved
- PowerDC, EPS
Example Analysis and signoff flow
Summary

- 3D/2.5D is here, and will become a cost effective alternative to process scaling; but not without both technical and business model challenges;
- 3D/2.5D realization involves entire design cycle with multiple 3D featured tools working together
  - Planning
  - Implementation
  - Sign off /Electrical /Thermal Analysis
  - Manufacture Test
- 3D/2.5D Implementation requires flexible platforms for wide range of design applications; By leveraging existing state of art silicon level tools with 3D enhancement and package co-design capability, 3D realization can handle massive interconnects and analysis in more automated and efficient way that has been seen in large SOC design today,
- A holistic and integrated Silicon-Package tool flow and design infrastructure is critical in minimizing risk, and improving design cycle for volume production.