3DIC and the Hybrid Memory Cube

Dean Klein

Micron Technology, Inc.
The Need: Break Down the Memory Wall

System Memory Bandwidth (GB/s)

4 Channel
3 Channel
2 Channel
Reducing System Cost

System Memory Bandwidth (GB/s)

- 2 Channel
- 3 Channel
- 4 Channel
- LGA2011

Socket 423
Managing System Complexity

System Memory Bandwidth (GB/s)

**DDR**

- 85 page specification
- 1 page of AC timing params
- 3 speed bins

**Standardization Time:**

< 3 yrs years
Managing System Complexity

System Memory Bandwidth (GB/s)

**DDR4**
- 214 page specification
- 9 pages of AC timing params
- 12 speed bins for BOL (to 2400)
- Standardized Time: >6 years and going

**DDR**
- 85 page specification
- 1 page of AC timing params
- 3 speed bins
- Standardization Time: < 3 yrs years

Graph showing the increase in System Memory Bandwidth (GB/s) over years from 1997 to 2015 with different generations of DRAM technology.
Hybrid Memory Cube (HMC)

Fast process logic and advanced DRAM design in one optimized package

- Power Efficient
- Smaller Footprint
- Increased Bandwidth
- Reduced Latency
- Lower TCO
Enabling Technologies

Abstracted Memory Management

Memory Vaults Versus DRAM Arrays
- Significantly improved bandwidth, quality and reliability versus traditional DRAM technologies

Logic Base Controller
- Reduced memory complexity and significantly increased performance
- Allows memory to scale with CPU performance

Through-Silicon Via (TSV) Assembly

Innovative Design & Process Flow
- Incorporation of thousands of TSV sites per die reduces signal lengths and reduces power
- Enables memory scalability through parallelism

Sophisticated Package Assembly
- Higher component density and significantly improved signal integrity
HMC Architecture

Start with a clean slate

DRAM
HMC Architecture

Re-partition the DRAM and strip away the common logic
HMC Architecture

Stack multiple DRAMs
HMC Architecture

Re-insert common logic on to the Logic Base die

3DI & TSV Technology

Logic Base

Vault
HMC Architecture

Logic Base
- Multiple high-speed local buses for data movement
- Advanced memory controller functions
- DRAM control at memory rather than distant host controller
- Reduced memory controller complexity and increased efficiency

Vaults are managed to maximize overall device availability
- Optimized management of energy and refresh
- Self test, error detection, correction, and repair in the logic base layer

3DI & TSV Technology
HMC Architecture
Link Controller Interface

HMC-SR Options: 10 Gbps, 12.5 Gbps or 15 Gbps

Example:
8 or 16 Transmit Lanes

8 or 16 Receive Lanes
Host Processor Memory Management

- Manufacturing Test
  - Burn-in
  - At-speed Functional

- Manage 100+ different DRAM timing parameters

- Manage field maintenance and self test

- Manage all present and future DRAM scaling and process variation issues

Non-managed DRAM (WIO, HBM, etc.)
Host Processor Memory Management

Simple memory requests and responses. No DRAM timing to manage

Manufacturing Test
- Burn-in
- At-speed Functional

Manage field maintenance and self test

Manage 100+ different DRAM timing parameters

Manage all present and future DRAM scaling and process variation issues

Non-managed DRAM (WIO, HBM, etc.)

Functions moved to HMC for management
The Package

Up to 1.28 Tbps Memory Bandwidth!

Standard BGA Packaging Solutions: Cost Effective Packaging using existing Ecosystems
HMC Near Memory

- All links between host CPU and HMC logic layer

- Maximum bandwidth per GB capacity
  - HPC/Server – CPU/GPU
  - Graphics
  - Networking systems
  - Test equipment
HMC “Far” Memory

- Far memory
  - Some HMC links connect to host, some to other cubes
  - Scalable to meet system requirements
  - Can be in module form or soldered-down

- Future interfaces may include
  - Higher speed electrical (SERDES)
  - Optical
  - Whatever the most appropriate interface for the job!
HMC Reliability

- Built-In RAS features at a high level...

- Logic Stability (DRAM controls in logic)
- Vault Data ECC protected
- CRC Protection on Link Interface
- Reliable handshake (packet integrity verified before memory access)
- Link Retry
- Address / Command Parity for Array transactions
## RAS Feature System Comparison

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>DRAM</th>
<th>RDIMM</th>
<th>HMC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extensive Test Flow</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Data ECC</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Address/Command Parity</td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Mirroring (back-up memory)</td>
<td></td>
<td>✓</td>
<td>✓✓</td>
</tr>
<tr>
<td>Sparing (Chipkill)</td>
<td></td>
<td>✓✓</td>
<td></td>
</tr>
<tr>
<td>Lockstep (redundancy w/better ECC)</td>
<td></td>
<td>✓✓</td>
<td></td>
</tr>
<tr>
<td>CRC Coding</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Self Repair</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>BIST</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Error Status and Debug Registers</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>DIMM Isolation (flags faulty DIMM)</td>
<td></td>
<td>✓✓</td>
<td></td>
</tr>
<tr>
<td>Memory Scrubbing</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

- ✓ Supported
- ✓✓ Redundant or not needed

September 4, 2013
Technology Comparison (Extreme Performance)

• What does it take to support 1.28TB/s of performance?

• Comparison of HMC to DDR3L-1600 and DDR4-3200

**Active Signals**
- DDR3 requires ~14,300
- DDR4 requires ~7,400
- HMC only needs ~2,160, HMC is ~85% less than DDR3

**Operating Power (including CPU’s)**
- DDR3 system requires ~2.25KW
- DDR4 system requires ~1.23KW
- HMC system only needs ~350W, HMC is ~72% less than DDR4

**Board Space**
- DDR3 requires ~165,000 sq mm
- DDR4 requires ~82,500 sq mm
- HMC only needs ~8,712 sq mm, HMC is ~90% less than DDR4

Assumptions:
1DPC, (SR x4) RDIMMs, 6.2W/channel for DDR3 @ 12.8GB/s, 8.4W/channel for DDR4 @ 25.6GB/s 5W per Link for HMC @ 160GB/s, 143 pins/channel for DDR3, 148 pins for DDR4, 270 per HMC, RDIMM area equals 10mm pitch x 165mm long, HMC w/keep outs equal 1089 sq mm, CPU for RDIMMS = 65W, CPU for HMC = 95W, each CPU supports up to 4 channels.
Technology Comparison (Single Link)

• What does it take to support 60GB/s of performance?
  • Comparison of HMC to DDR3L-1600 and DDR4-3200

**Channels**
- DDR3 requires 5 channels
- DDR4 requires 3 channels
- **HMC only needs 1 Link**

**Board Area**
- DDR3 requires ~7,734 sq mm
- DDR4 requires ~3,843 sq mm
- **HMC only needs ~1,089 sq mm**

**Active Pins**
- DDR3 requires 670 pins
- DDR4 requires 345 pins
- **HMC only needs 72 pins**

**BW/pin**
- DDR3 ~90MB/pin
- DDR4 ~174MB/pin
- **HMC ~833MB/pin**

_assumptions:_ Same as previous example of 1.28TB/s Bandwidth
Packet Buffer Memory Subsystem Comparison

- Packet Buffer Requirements & Assumptions
  - 4 100GbE ports per Network Processor / Traffic Manager
  - Packet buffering on ingress or egress
  - Maintain 800Gbps effective bandwidth across all packet sizes at each packet buffer
## 400Gbps Packet Buffer Comparison

### Parameter Comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DDR4-2400 x16</th>
<th>4 HMC-15G-SR Links</th>
<th>HMC System Level Savings</th>
</tr>
</thead>
<tbody>
<tr>
<td># of Memory Devices</td>
<td>48</td>
<td>1</td>
<td>85% fewer pins</td>
</tr>
<tr>
<td>Total # of Pins</td>
<td>1848</td>
<td>276</td>
<td>41% lower power</td>
</tr>
<tr>
<td>Power: Host PHY + Memory</td>
<td>56W</td>
<td>33W</td>
<td>84% smaller memory footprint</td>
</tr>
<tr>
<td>Memory Surface Area</td>
<td>6048mm²</td>
<td>961mm²</td>
<td>75% smaller host PHY</td>
</tr>
<tr>
<td>Host PHY Silicon Surface Area$^1$</td>
<td>1.75x</td>
<td>1x</td>
<td></td>
</tr>
</tbody>
</table>

1. Relative sizes represented

---

All devices drawn to scale

---

©2012 Micron Technology, Inc.
# Broad Adoption & Momentum

**http://www.hybridmemorycube.org**

1.0 Specification released April 2013

<table>
<thead>
<tr>
<th>Over 120 Adopters!</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Accel, Ltd</strong></td>
</tr>
<tr>
<td><strong>ADATA Technology Co., LTD</strong></td>
</tr>
<tr>
<td><strong>AIRBUS</strong></td>
</tr>
<tr>
<td><strong>Altior</strong></td>
</tr>
<tr>
<td><strong>APIC Corporation</strong></td>
</tr>
<tr>
<td><strong>Aria Design</strong></td>
</tr>
<tr>
<td><strong>Arnold&amp;Richter Cine Technik</strong></td>
</tr>
<tr>
<td><strong>Atria Logic, Inc.</strong></td>
</tr>
<tr>
<td><strong>BroadPak</strong></td>
</tr>
<tr>
<td><strong>Cadence Design Systems, Inc.</strong></td>
</tr>
<tr>
<td><strong>Convey Computer Corporation</strong></td>
</tr>
<tr>
<td><strong>Cray Inc.</strong></td>
</tr>
<tr>
<td><strong>DAVE Srl</strong></td>
</tr>
<tr>
<td><strong>Design Magnitude Inc.</strong></td>
</tr>
<tr>
<td><strong>Dream Chip Technologies GmbH</strong></td>
</tr>
<tr>
<td><strong>Engineering Physics Center of MSU</strong></td>
</tr>
<tr>
<td><strong>eSilicon Corporation</strong></td>
</tr>
<tr>
<td><strong>Exablate Corporation</strong></td>
</tr>
<tr>
<td><strong>Ezchip Semiconductor</strong></td>
</tr>
<tr>
<td><strong>FormFactor Inc.</strong></td>
</tr>
</tbody>
</table>

[Over 110 Adopters to date!](http://www.hybridmemorycube.org)
A Robust Ecosystem

**OEM’s**
- Juniper Networks
- Tektronix
- Agilent
- Broadcom
- HUAWEI
- ZTE
- TILERA
- TERADYNE
- CRAY
- CONVEY computer™
- BROCADE

**Enablers**
- IBM
- Analog Devices
- ARM
- EZchip
- tabula
- achronix
- Marvell
- Altera
- Xilinx
- TELEDYNE LECROY™
- Cavium

**Tools**
- Cadence
- SiI
- Northwest Logic
- Mentor Graphics
- Inphi®
- Open-Silicon
Industry Validation

“...like adding a turbocharger to your computer”
- datacenteracceleration.com

“...wicked fast”
- gigaom.com

“...a complete paradigm shift”
- extremetech.com

“...unprecedented levels of memory performance”
- Electronic News

“...an entirely new category of memory”
- Tom’s Hardware
HMC 3DIC – The Bottom Line

- Improved costs – at a system and TCO level
- When the need exists, the ecosystem develops.
- There are no competing technologies...
HMC 3DIC – The Bottom Line

- Improved costs – at a system and TCO level
- When the need exists, the ecosystem develops.
- There are no competing technologies… There are no universal solutions