Embedded Component in Panel Production
A discussion of Market-Leading Technologies

Mark Beesley
COO Advanced Packaging, a Business Unit of AT&S AG
Miniaturized Systems

Electronic component assemblies are moving to highly integrated modules

Big challenges regarding design, technology, standardisation, supply chain, business model …
Co-design

Stone Age
Co-Design

Semicon → Package → Module → PCB → EMS → OEM

Classical Approach
Why embedding?

Trends and challenges in electronics

- More functions
- Smaller devices
- Short cycles for design-to-market
- Increased component population
- Fragile components
- Supply-chain complexity
- Increased cost of high-end IC design
- Lower power
- Increased clock frequency
- Thermal management
Why embedding?

Advantages of embedding

- More functions
- Smaller devices
- Short cycles for design-to-market
- Increased component population
- Fragile components
- Miniaturisation
- Reliability
- Ease-of-use
- Performance
- Supply chain complexity
- Increased cost of high-end IC design
- Lower power
- Increased clock frequency
- Thermal management
How is it done?

Moving components from the surface and putting them inside the PCB substrate.

1. Die Placement
2. Lamination
3. Structuring
Embedded die package unit shipment forecast

Breakdown by application area (Munits)

Yole Developpement © October 2012

<table>
<thead>
<tr>
<th>Year</th>
<th>Automotive</th>
<th>Medical</th>
<th>Consumer</th>
<th>Mobile - Wireless</th>
</tr>
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<tbody>
<tr>
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<td>0</td>
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<td>6</td>
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<td>0</td>
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<td>431</td>
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<td>2015</td>
<td>6</td>
<td>0,05</td>
<td>164</td>
<td>798</td>
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<td>2016</td>
<td>11</td>
<td>0,09</td>
<td>281</td>
<td>1,410</td>
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<td>2017</td>
<td>21</td>
<td>0,15</td>
<td>478</td>
<td>2,116</td>
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<td>2018</td>
<td>35</td>
<td>0,22</td>
<td>752</td>
<td>2,952</td>
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<td>2019</td>
<td>64</td>
<td>0,30</td>
<td>1,108</td>
<td>3,898</td>
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<td>2020</td>
<td>91</td>
<td>0,38</td>
<td>1,469</td>
<td>4,582</td>
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</table>

<table>
<thead>
<tr>
<th>Year</th>
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<tbody>
<tr>
<td>2010</td>
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<td>2011</td>
<td>91</td>
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<td>114</td>
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<td>2013</td>
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<td>2014</td>
<td>525</td>
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<td>2015</td>
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<td>2016</td>
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<td>2018</td>
<td>3,739</td>
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<td>2019</td>
<td>5,069</td>
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<td>2020</td>
<td>6,142</td>
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</tbody>
</table>

Device count (Munits)
AT&S consortium leader

Largest EU funded project focussed on INDUSTRIALISATION
11 partners driving Embedded Component Packaging technology
Agenda

Market and Status

Value Proposition

Process & Capabilities

Application Examples

Standardization

Summary
Miniaturation

- Example: MEMS μPhone

**Standard solution**
- ASIC + MEMS side by side
- Footprint: 8.4 mm²

**ECP®-enabled solution**
- ASIC embedded + MEMS on surface
- Footprint: 4 mm²

**Footprint reduction** - 52%
Reliability

**Mechanical stress: Drop test** [JEDEC JESD22-B111, 1000 drops @ 1500g / 0.5ms]

**Standard solution**
- Daisy chain of passive components on top of an 8 layer substrate

  ▪ Components / Cu tracks take full weight of impact

**ECP®-enabled solution**
- Daisy chain of passive components within an 8 layer substrate

  ▪ Embedded components and laser-via interconnects are tightly surrounded with protective FR4

---

Drops passed

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard solution</td>
<td>304</td>
</tr>
<tr>
<td>ECP®-enabled solution</td>
<td>1000</td>
</tr>
</tbody>
</table>
Reliability

- **Thermal stress: TCT** [1000 cycles @ -55 / 150 °C]

**Standard solution**

Daisy chain of passive components on top of an 8 layer substrate

TCT cycles passed 1000

**ECP®-enabled solution**

Daisy chain of passive components within an 8 layer substrate

Daisy chain on chip within a 4 layer substrate

SMD vs ECP®: Comparable performance!
Performance

Example: EMI-shielded module

**Standard solution**

- Solder joints
  (*less conductivity & more parasitics*)
- Long path to other components
  (*side-by-side components*)
- No shielding
  (*external shielding necessary, increase of cost and z-dimension*)

**ECP®-enabled solution**

- Cu-plated µVias
  (*better conductivity & less parasitics*)
- Short path to other components
  (*stacked components*)
- Intrinsic shielding
  (*shielding by ground layers and edge plating / via stitching*)

**EMI with ECP® - 20dB**
Ease-of-use

- Example: Mobile TV tuner

<table>
<thead>
<tr>
<th>Standard solution</th>
<th>ECP®-enabled solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Components on PCB: 5</td>
<td>Components on PCB: 1</td>
</tr>
<tr>
<td>Solder pads on PCB: 44</td>
<td>Solder pads on PCB: 28</td>
</tr>
<tr>
<td>Footprint on PCB: 29 mm²</td>
<td>Footprint on PCB: 16 mm²</td>
</tr>
</tbody>
</table>

- Components in BOM - 80%
- Solder pads - 36%
- Footprint - 45%
Application focus

ECP


Integrated Electronics Packaging solutions from AT&S
## Ramping applications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Application</th>
<th>X,Y Reduction</th>
<th>Embedded Component advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power</strong></td>
<td>Voltage Convertor</td>
<td>40%</td>
<td>Smallest footprint – integrated module – fully tested solution</td>
</tr>
<tr>
<td></td>
<td>Charge Management</td>
<td>40%</td>
<td>Stacked package for advanced Li-ion battery charge management</td>
</tr>
<tr>
<td><strong>Media &amp; Wireless</strong></td>
<td>Media Codec</td>
<td>30%</td>
<td>Integrated module – discrete passives stacked on eWLP</td>
</tr>
<tr>
<td></td>
<td>Mobile TV</td>
<td>50%</td>
<td>Single device solution for mobile TV tuner</td>
</tr>
<tr>
<td></td>
<td>NFC module</td>
<td>40%</td>
<td>Stacked package for smallest footprint solution</td>
</tr>
<tr>
<td><strong>MEMS &amp; Sensor</strong></td>
<td>MEMS μphone</td>
<td>50%</td>
<td>Superior performance MEMS μphone / pressure sensor with smallest form factor</td>
</tr>
<tr>
<td></td>
<td>Identification</td>
<td>New feature</td>
<td>Integrated biometric sensing</td>
</tr>
<tr>
<td></td>
<td>Position sensor</td>
<td>50%</td>
<td>High accuracy Hall effect sensor – advanced micro joystick application</td>
</tr>
<tr>
<td><strong>Shielding</strong></td>
<td>Sensitive devices</td>
<td>50%</td>
<td>Implementation of shielding using the laminate package instead of metal can</td>
</tr>
</tbody>
</table>
Agenda

Market and Status

Value Proposition

Process & Capabilities

Application Examples

Standardization

Summary
## Design guidelines

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Series</th>
<th>Proto</th>
<th>Demonstrator</th>
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</thead>
<tbody>
<tr>
<td><strong>Stack Up</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Build up</td>
<td>Single ECP® core with sequential build up</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>ECP® core thickness (over Cu)</td>
<td>250</td>
<td>220</td>
<td>200</td>
</tr>
<tr>
<td>Number of layers</td>
<td>2 – 6</td>
<td>2 – 8</td>
<td>-</td>
</tr>
<tr>
<td>Line / space</td>
<td>40/40 μm</td>
<td>25 / 25μm</td>
<td>-</td>
</tr>
<tr>
<td>Laser via land size (build up)</td>
<td>min 175μm</td>
<td>min 150μm</td>
<td>-</td>
</tr>
<tr>
<td>PTH diameter (Core &lt; 400μm thickness)</td>
<td>150 μm</td>
<td>100μm</td>
<td>-</td>
</tr>
<tr>
<td>Copper filled through hole</td>
<td>-</td>
<td>Yes *</td>
<td>-</td>
</tr>
<tr>
<td><strong>Component</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Embedded component types</td>
<td>Active + passive components per module</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Bump metallization</td>
<td>Copper (minimum 4μm)</td>
<td>TiNiAg, NiAu, NiPd, Sn,…</td>
<td>-</td>
</tr>
<tr>
<td>Embedded active component size</td>
<td>0,4mm &lt; X, Y &lt; 8,0mm*</td>
<td>4mm &lt; X, Y &lt; 12,0mm</td>
<td></td>
</tr>
<tr>
<td>Embedded passive size</td>
<td>0402/0201</td>
<td></td>
<td>01005</td>
</tr>
<tr>
<td>Organic Re-passivaion material</td>
<td>Compatible with current process**</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Component pad size / pitch</td>
<td>200μm / 250μm</td>
<td>150μm / 175μm</td>
<td>-</td>
</tr>
<tr>
<td>Component connection</td>
<td>No back-side connection</td>
<td>Back-side connection on 0402</td>
<td>0201</td>
</tr>
<tr>
<td>Component material</td>
<td>Si</td>
<td>GaAs*</td>
<td>LiTaO</td>
</tr>
</tbody>
</table>

* Design related limited use

** Compatibility of specific material needs to be verified before production
Production facility

- **Rapid Prototyping** thanks to NPI team
- **Dedicated ECP® design center** in Germany
- **Supply chain management**
- **Prototype lead time 1-3 month** thanks to Product and NPI Management
- **Dedicated production facility** in Leoben, Austria
- **Production area 100-% ESD-protected**


<table>
<thead>
<tr>
<th>Total Manufacturing</th>
<th>Clean room Class 100K</th>
<th>Clean room Class 10K</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.000 m²</td>
<td>1.200 m²</td>
<td>200 m²</td>
</tr>
</tbody>
</table>

“We create more than 60 new prototypes per year with lead times of 1-3 months.

Clean products through excellence in design for manufacturing!”
Volume production experience

“We are audited and approved to the highest standards. ECP® is ready for your requirements today”

- **Units shipped:** > 100 Mio
- **AT&S Yield:** > 99.5%
- **Field returns:** 0
Component requirements

**Wafer-based embeddables**

- Pad finish needing Cu plating to contact with microvias (existing process for WLP components)
- Pad pitch adaptation to organic-substrate design rules through RDL
- Wafer thinning to 100-150µm

**Passive discrete embeddables**

- Use of thin components with copper terminations
- Availability of capacitors and resistors
- Other discretes (inductors) also in development
- Component thickness of 100µm – 220µm
- Case sizes of 0201, 0402 and above
### Versatile Integration

**Smart use of Embedded Component Technology**

<table>
<thead>
<tr>
<th>Tech</th>
<th>Diagram</th>
<th>Description</th>
<th>Applications</th>
</tr>
</thead>
</table>
| 1 ECP® | ![Diagram](image1) | - Wafer-level fan-in/out  
- Substrate-level routing  
- Integration of discrete passives  
- AT&S Production | - Mobile Power (mid integration)  
- MEMS & Sensor substrates  
- Media & Wireless |
| 2 SESUB® | ![Diagram](image2) | - Substrate-level fan-in/out  
- Substrate-level routing  
- No discrete passives  
- TDK Production | - Audio  
- Power Management (high integrated PMIC)  
- RF |
| 3 NextGen | ![Diagram](image3) | Roadmap project | Next generation highly integrated module packages |
| 4 EmPower | ![Diagram](image4) | - Dedicated power semicon package  
- Integration of high-current and logic | Discrete power semicon components  
- Integrated Industrial power modules |
# ECP® - Embedded Active Components

**Smart use of AT&S Embedded Component Technology**

<table>
<thead>
<tr>
<th>ECP Solution #1</th>
<th>ECP Solution #2</th>
<th>ECP Solution #3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fanned-in die + Passives</strong></td>
<td><strong>High density die + Passives</strong></td>
<td><strong>High density die + Passives</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Substrate thin-ness</th>
<th>300µm</th>
<th>450µm</th>
<th>300µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passives integrated</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>Die shrinkage</td>
<td>LOW</td>
<td>MID</td>
<td>HIGH</td>
</tr>
<tr>
<td>Package Cost</td>
<td>↓</td>
<td>↔</td>
<td>→*</td>
</tr>
</tbody>
</table>

**Select when …**
- Modified SMT components can be used
- Die shrink gives cost advantage
- Die shrink gives significant cost advantage or thin-ness is crucial

* includes cost of moulded package
Embedded packaging = merger of worlds

**ECP**
- **PCB**
  - Large format substrate
- **Pick & Place**
  - High speed assembly
- **Epoxy**
  - Mass production die adhesion
- **Embedded Package**
- **Value add**

**SESUB**
- **IC Substrate**
  - Mid-Large format substrate
- **Die Placer**
  - High accuracy assembly
- **Moulding**
  - Mass production die encapsulation
- **Embedded Package**
- **Value add**
Design automation

Released for mainline PCB-design platforms

- Mentor Expedition – high-profile launch at DAC 2012 in San Francisco

- Cadence Allegro 16.5 (and above) with direct support of PCB layout with embedded components

- BENEFITS – design automation, integrated design rules, thermal modelling, other simulation benefits

  • Contact AT&S to line up information from your system provider
Supply chain

Incoming Wafer
Cu-Bumping or RDL
Wafer Thinning
Wafer Dicing
Chip Tape & Reel

Passives

ECP®- Technology

SMT assembly
Overmolding
Testing
Solderballing
Singulation and Packaging

Semicon or foundry
AT&S

Customer or outsourced
Agenda

Market and Status

Value Proposition

Process & Capabilities

Application Examples

Standardization

Summary
Product Families

SiB
System in Board

- PCB technology
- Bigger size
- Higher layer count
- Many components
- Mostly passives

SiP
System in Package

- Package technology
- Small sized modules
- Low layer count
- Few components
- Mostly actives
Use case 1: System in Package
Example: Value add of ECP® for power management

600mA DC-DC step-down converter

- **Application:** Local voltage management module using a high efficiency switching regulator optimized for low-power battery-operated portable applications.

- **Components:** 1 x IC (switching regulator)
  1 x Inductor
  2 x Capacitors

- **Standard solution:**
  All 4 components get soldered onto the PCB
  → The IC is packaged

- **ECP® enabled solution:**
  - **Miniaturation:** 50% footprint reduction
  - **Performance:** less package loss
  - **Ease-of-use:** just 1 component on PCB (vs. 4)
    just 8 solder joints on PCB (vs. 12)
Use case II: System in Board
Example: Value add of ECP® for SSD

**Std. 2.5” SSD mainboard**
- PCB area: 65 x 90mm (9sqinch)
- Capacity: 480GB

**2.5” SSD mainboard with ECP®**
- PCB area: 65 x 90mm (9sqinch)
- ~200 embedded components
- Capacity: 720GB

50% MORE MEMORY
Other Application examples

MEMS μPhone

Mobile TV tuner

3D Integration
User authentication

Authentication

PMIC

2.5DC Cavity integration
Agenda

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Summary
Alliance of Market Leaders
AT&S and TDK

Standardization of Embedded Component Substrates

March 11, 2013
AT&S and TDK – Committed to the Ramp Up and Production of embedded component substrates and modules in high volume

- Modules
- Robust patent portfolio & turnkey provider in the field of component embedding
- Multiple patents related to embedding technology on hand
- Full flow from Design to Final Product including back-end capability readiness (Assembling, moulding, testing)

- Substrates
- A head start of 6-9 month in the field of cavity embedding processes
- Process knowhow & process parameters / specifications
- DFM and NPI capabilities
- Excellent Prototype performance
- Transferable mass volume experience
Value Proposition

Second source availability
Secured volume ramp up
Access to next generation embedding standards
Best-in-class Process knowhow transfer
Freedom to Operate - robust combined IP portfolio

Strong alliance = safe and controlled Embedding technology access
Need for Standardization

1. Integrated products using substrate embedding technology are selling since 2009
   → Volume is currently dominated by simple structures (DC/DC converter modules, MEMS, fan-out packages etc.)
   → More complex module structures for mobile power, connectivity etc. are in volume production, and gaining momentum

2. Main drivers for the usage of embedding substrates are high miniaturization (x, y and z) and improved system performance

3. The adoption of embedded substrate technology is rapidly expanding in different applications (media, wireless, MEMS, etc)

4. There are a few “players“ offering substrate embedding, but with different flavours of technologies, different capabilities, different business models …

5. TDK and AT&S have formed an alliance with the clear intention and capability to drive standardization of embedded component substrates
# Embedded Substrate Standards

<table>
<thead>
<tr>
<th>Standard</th>
<th>ECP</th>
<th>SESUB</th>
<th>Next Generation Embedding Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technical Specification</strong></td>
<td>Low-medium complexity</td>
<td>High complexity</td>
<td>Target = Minimum further 20% x, y, z reduction based on technology</td>
</tr>
<tr>
<td>Different component heights</td>
<td>Same component height</td>
<td>- Combination</td>
<td></td>
</tr>
<tr>
<td>Low-medium I/O count</td>
<td>High I/O count</td>
<td>- Optimization</td>
<td></td>
</tr>
<tr>
<td>High current &gt;10A</td>
<td>High current &gt; 8A</td>
<td>- Upgrade</td>
<td></td>
</tr>
<tr>
<td>IC pitch &gt; 200µm</td>
<td>IC pitch &lt; 80µm</td>
<td>Embedding Technology by AT&amp;S and TDK</td>
<td></td>
</tr>
<tr>
<td>&gt; 2 layers</td>
<td>4-6 Layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thick Cu- layer &gt;18µm</td>
<td>Thin Cu- layer &lt;12µm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Key Applications | Mobile Power (low-mid integration); MEMS & Sensor substrates; Media & Wireless | Audio; Power Management (high integrated PMIC); RF | Next generation integration concept |

| Commercial | Suitable cost-point to address substrate requirements | Suitable cost-point to address module requirements | Targeted cost structure for high integrated modules |
Roadmap

1. IP cross-license agreement (AT&S and TDK)  COMPLETE
2. Definition of standards for embedded substrates (AT&S and TDK)  COMPLETE
3. Volume ramp up of ECP at AT&S
   Volume ramp up of SESUB at TDK  AVAILABLE

**Dual source is a requirement = Business Trigger**

4. Volume ramp up of ECP at TDK  + 6 months
   Volume ramp up of SESUB at AT&S  + 6 months

**Next generation standard is a requirement = Roadmap Trigger**

5. Innovation and Development of Next Generation embedding technology  + 12 months

6. Technology Transfer and Commercial package to enable future embedded technology providers (pooling) and expand the standard  As needed
Summing up

Leading chip-embedding technologies from AT&S

Key benefits
– Miniaturization
– Reliability
– Performance
– Integration

Embedded Component is in volume production
– Production-ready – multiple sources
– High yield (>99.5%)
– NPI for rapid prototyping and supply-chain management

Large number of projects with industry leaders
– Mobile devices
– Industrial
– Automotive
Global set-up with access to key markets

International presence and key technology production overview

**Headquarters: Leoben-Hinterberg**
- Target region: global
- Key technologies: HDI, special products, prototypes, quick turnaround business, rigid-flex PCBs

**Plant: Chongqing (under construction)**
- Key production capability after completion: IC substrates

**Plant: Ansan**
- Target region: Korea, Europe
- Key technologies: flexible and rigid-flex PCBs

**Plant: Shanghai**
- Target region: global
- Key technologies: HDI volume business

**Plant: Fehring**
- Target region: Europe
- Key technologies: double-sided, flexible, semi-flexible, rigid-flex PCBs

**Plant: Nanjanqud**
- Target region: Europe, India
- Key technologies: double-sided and multilayer PCBs