History says

Low pin

High pin & Integration
As Multi-function

City phone / PCS

Feature Phone

Smart Phone

pager

SOIC

QFP

PBGA

Package-on-Package

WLCSP
Cell Phone Trend

1990’s
- TQFP
- SSOP
- SOIC
- uBGA

2000’s
- TQFP
- BGA
- uBGA
- TQFP

2010’s
- BGA
- SCSP
- WLCSP
- fCSP
## Packages per Mobile phones grade

<table>
<thead>
<tr>
<th>Function</th>
<th>High-end smartphone</th>
<th># pkg</th>
<th>Mid-end smartphone</th>
<th># pkg</th>
<th>Feature phone</th>
<th># pkg</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Processors</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AP</td>
<td>fcCSP[e-die TMV]</td>
<td>1</td>
<td>Integrated AP+BB(+DDR) (Hybrid SCSP= bottom die FC + top die WB)</td>
<td>1</td>
<td>Baseband (+SDR) (SCSP)</td>
<td>1</td>
</tr>
<tr>
<td>Baseband</td>
<td>SCSP</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DRAM</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPDDR</td>
<td>SCSP</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>NAND</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flash</td>
<td>SCSP, 32GB</td>
<td>1</td>
<td>Flash (SCSP, 2GB)</td>
<td>1</td>
<td>Flash (SCSP, 128MB)</td>
<td>1</td>
</tr>
<tr>
<td><strong>PMIC</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 PMICs</td>
<td>3 WLCSP, MLF</td>
<td>4</td>
<td>1 PMIC (WLCSP)</td>
<td>1</td>
<td>1 PMIC (CABGA)</td>
<td>1</td>
</tr>
<tr>
<td><strong>Power Amp</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 PA</td>
<td>1 LGA, 3 MLF</td>
<td>4</td>
<td>2 PA (LGA, MLF)</td>
<td>2</td>
<td>2 PA (2 LGA)</td>
<td>2</td>
</tr>
<tr>
<td><strong>MEMS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 MEMS</td>
<td></td>
<td>6</td>
<td>2 MEMS</td>
<td>2</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td><strong>Audio IC</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 kinds</td>
<td>WLCSP, CABGA</td>
<td>2</td>
<td>1 Audio codec (WLCSP)</td>
<td>1</td>
<td>1 Audio codec (WLCSP)</td>
<td>1</td>
</tr>
<tr>
<td><strong>Others</strong></td>
<td>RF, WLAN, Control IC, DMB, NFC/HDMI, Filter</td>
<td>15</td>
<td>RF, WLAN, Control IC, Filter</td>
<td>7</td>
<td>RF</td>
<td>1</td>
</tr>
</tbody>
</table>

*Amkor Proprietary Business Information*
Electronics in Everything – The Light Bulb

- For 70+ years the common light bulb contained no electronics
- Then in the 1970’s, CFL bulbs included a small power converter.
- Today the LED bulb contains a power supply, driver circuits, dimmers, etc.
- Soon bulbs will contain WiFi or Bluetooth radios and microcontrollers for remote operation.
X-ray Image of the L-Prize Winning LED Lamp

Source: IEEE Spectrum, March 2012

Philips Lighting

Power discrete market is important.
<table>
<thead>
<tr>
<th>One layer Substrate (RtMLF/ tsCSP2)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RtMLF (1L)</strong></td>
</tr>
<tr>
<td>Resin filled</td>
</tr>
<tr>
<td><strong>PPG with Carrier</strong>*</td>
</tr>
<tr>
<td>PPG without Carrier***</td>
</tr>
<tr>
<td>(* back-etching required)</td>
</tr>
</tbody>
</table>

(* back-etching required)
Thinner TMV (total stack of 1 mm)

- Thinner POR TMV
  - Thinner core, Cu, SR, mold
- WLFO TMV
- EDS TMV
- Coreless TMV

Partner ship with technology leading substrate company (SEMCO, IBIDEN....) having differentiated yield and technology?
Possum and CoC Structures
Solder bumps => Cu pillar bumps
Mass Reflow => TCNCP
Memory => high band width
Subs design rule => finer

Wire Bond
Back-to-Back FlipStack®
Flip Chip

TCNCP Cu Pillar
MR Cu Pillar
MR Solderball

LTE/Apps (28 nm and below)
18/18 L/S
500+ memory bumps

Bump Pitch(um)
150 130 55/110 45/90 40/80 25/50

3G and below
3G and below
Imbedded/Panel
Need to have very high PnP UPH: chip shooter vs die bonder

Faster interconnection: FC vs WB

12” wafer ~ 113sqin

18” x 24” panel ~ 432sqin

High density process
Sensor Market

Source: Morphoident wdb page
Contents

• Why TSV?
• 3D/2.5D TSV applications and market
• Challenges in TSV Packaging
  1. Cost
  2. Yield
  3. Performance
• Challenges in MEOL
  1. Technology adoption
  2. Process integration
  3. Cost
Episode 1 : Power of Internet

**ENCYCLOPAEDIA BRITANNICA** : 244 year history
2012 Revenue Breakdown : 85% from Online Sale of Educational Contents
15% from Online Information Sale
0 % from offline Book selling

1990s emerging PC + Internet
  1990 : sold out 120K sets
  1996 : 40K
  2010 : 8K
  2012 : announced no hard copy publication
Why TSV?

<table>
<thead>
<tr>
<th>Year</th>
<th>2001</th>
<th>2002</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2010</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnect length</td>
<td>4km</td>
<td>5km</td>
<td>6km</td>
<td>7km</td>
<td>9km</td>
<td>10km</td>
<td>13km</td>
<td>20km</td>
</tr>
</tbody>
</table>

- Circuit Wire Length in a Chip

- Memory
  Gate delay time at 22 nm : < 0.5 ps
  Circuit wire delay time : ~ 2000 ps

Source: Jerray A., “From 3D technology to 3D-IC demonstrators and associated design flow”, GSA EDA Interest Group, 2011 Feb. 25th
3D/2.5D TSV APPLICATIONS & MARKET
**Market Drivers**

- **Lower Cost**: 2016(?)
- **High speed signal process**
- **Low power consumption**: 2014
- **Small form factor**
- **High thermal performance**: 2012
- **High speed signal process**
- **Low power consumption**: 2015~6

**Market Time Line**

- 2012
- 2014
- 2015
- 2016 (?)
Package Migration to 2.5D & 3D TSV

2.5D MCM - CPU, GPU, Networking
- 100X Improvement in Inter-Die Bandwidth / Watt
- 50% Power Savings
- 5X Latency Reduction
- 20X denser Wire Pitch

3D - Smartphones, Tablets, Memory
- 8X Performance in Bandwidth
- 50% Power Savings
- Profile Improvement
Requests on high performance package technology

- Market requires more memory bandwidth and lower power consumption
- 2.5D & 3D TSV realize interconnection with higher bandwidth & low power consumption (adopting wide IO memory)

Wide IO has 2x power efficiency of LPDDR3

Source: JEDEC, 2012. Mar
3D TSV Development Strategy/Trend

- Mobile AP + Memory 3D TSV

![Diagram showing the development strategy and trend of 3D TSV for mobile AP and memory, with price and performance axes. The timeline ranges from 2011 to 2016, showing the evolution of LPDDR2 (3.2GB), LPDDR3 (12.8GB), LPDDR4 (25.6GB), Wide I/O (12.8GB), and Wide I/O2 (34GB).]
2.5D and 3D Limitations

- The JEDEC WIO memory interface consumes over 2.8 mm\(^2\) of real estate or almost 10% of a 6 x 6 mm die. At 20nm, the cost is very high.
- WIO is already too slow and can be matched by LPDDR3 W/O TSVs.
- WIO-2 will double the number of TSVs, using more area of the die.
- Surely, this cannot continue very long.

- WIO = 12GB/s
- WIO-2 = 35GB/s
Si Photonics

Source: Intel website “50Gbps Si Photonics Link: Tech Overview”
Assembly Process

Foundry

CMOS wafer

Photonics wafer

Probe

Bumping

dicing

P Probe

E Probe

Bumping

Assembly

Final Test

Dicing

Amkor

Optical Module Assembly: LD/Fiber Attach and module test
Challenges on 2.5D/3D to faster Market entry

- **Cost** contributors: TSV fab, MEOL (Middle End of Line), BEOL (Back End of Line or Chip Stacking) and Test
- **Yield**: Pre-matured Technology Process/ Material/ Equipment
  - Yield Gap - Matured Process: TSV = > 99.9% : ~ 95% or so
- **Si Interposer**: Size, Chip attach method, Warpage control, Surface finish
- **Particles**: Affect yields on Micro Bumping, MEOL and BEOL
- **Performance**: Thermal performance for 3D
CHALLENGES IN TSV PACKAGING
Cost Competitiveness _ Organic Interposer

- **Potential Applications (Opportunities)**
  - Cost sensitive products

- **Cost Challenges (Key Enabler)**
  - Easier through hole formation over Si (Laser drilling)
  - Much larger working panel size
  - Cost expectation

---

Si Interposer

- Expectation: Around 50% cost reduction!

- Cost: 2.7 ~ 4 $/cm²

Organic Interposer
Cost Competitiveness _ Organic Interposer
(Design Challenges)

- **Design Capability (Key Enabler)**
  - Bump pitch : 50um
  - L/S : 6 / 6 um
  - Via/via pad : 15 / 32 um
  - 2 ~ 3 layer stack-via capable

  \[
  \text{Sample design rule in 2013}
  \]

- **Design Conversion Example (Si \(\rightarrow\) Organic, Same X-Y size conversion)**

  \[
  \begin{align*}
  \text{Layer count} & : \text{M1, M2, Al layer} \\
  \text{Al L/S/via} & \approx 3 / 2 / 4 \text{ um} \\
  \text{Cu L/S/via} & \approx 1 / 1 / 0.6 \text{ um} \\
  \text{TSV pitch} & : 180 \text{ um} \\
  \text{Size} & : 26 \times 32 \text{mm}^2
  \end{align*}
  \]

  \[
  \begin{align*}
  \text{Layer count} & : 8 \text{ layer} \\
  \text{Line/space} & : 5 / 5 \text{ um} \\
  \text{External layer via pitch} & : 40 \text{ um} \\
  \text{Core layer via pitch} & : 250 \sim 300 \text{ um} \\
  \text{Size} & : 26 \times 32 \text{mm}^2
  \end{align*}
  \]
Cost Competitiveness _ Organic Interposer
(Assembly Challenges)

- **Interposer HT warpage**

  ![](image)

  - Si interposer (Asymmetric)
  - Organic interposer (Symmetric)

  Less HT warpage due to symmetric structure or customized design?

- **Assembly Interconnection Methodology**

  - TCNCP
  - Mass Reflow + UF
  - TC bonding + UF

  - Small die (AP...)
  - Big die (GPU...)

  Difficulties in assembly interconnection due to organic interposer’s expansion at bonding temp.?
Cost Competitiveness - Glass Interposer

Thinner Glass Has Been Increasingly Employed In Evolving Applications of Display Substrates & Cover Glass

<table>
<thead>
<tr>
<th>Gen Size</th>
<th>Glass Thickness (mm)</th>
<th>Flexible display &amp; electronics e-Paper, continuous roll-to-roll component manufacture</th>
<th>Mobile LCD panels, cover glass, touch sensor plates for notebooks, net-books &amp; mobile internet devices</th>
<th>Slates, notebooks, monitors &amp; TVs, small &amp; medium size touch sensors &amp; cover glass</th>
<th>TV &amp; desktop monitors. Large size cover glass &amp; touch sensor plates</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3m</td>
<td>≤ 0.1</td>
<td></td>
<td>Mobile LCD panels, cover glass, touch sensor plates for notebooks, net-books &amp; mobile internet devices</td>
<td>Slates, notebooks, monitors &amp; TVs, small &amp; medium size touch sensors &amp; cover glass</td>
<td>TV &amp; desktop monitors. Large size cover glass &amp; touch sensor plates</td>
</tr>
<tr>
<td>0.5m</td>
<td>0.2</td>
<td></td>
<td>Mobile LCD panels, cover glass, touch sensor plates for notebooks, net-books &amp; mobile internet devices</td>
<td>Slates, notebooks, monitors &amp; TVs, small &amp; medium size touch sensors &amp; cover glass</td>
<td>TV &amp; desktop monitors. Large size cover glass &amp; touch sensor plates</td>
</tr>
<tr>
<td>1.0m</td>
<td>0.3</td>
<td>Commercial availability</td>
<td>Scheduled Development Proposed</td>
<td>Proposed</td>
<td>Proposed</td>
</tr>
<tr>
<td>1.5m</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.0m</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.5m</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3m</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Signal Path Delays in 3D-IC

Source: GIT Dr. Tummala

Glass employed for flat panel displays and cover glass

Glass as a Carrier

Glass an Interposer or PCB

1089 Vias Drilled Simultaneously

Source: Advanced Packaging Oct. 24, 2012
Addition of TSV wafer finishing (MEOL) can be a key challenge to yield.
Technical Challenges - BEOL yield (Chip Attach & Stacking)

3D TSV integration: AP+Memory & memory stack
- Top die > Bottom TSV die
- Same die stacking
- Top die < Bottom TSV die

Thermo compression bonding

2.5D TSV integration: GPU/CPU + memory

Mass reflow & Thermo compression bonding
Mass reflow + CUF
TC + NCP/NCF/CUF
## Technical Challenges _ BEOL yield (Chip Attach & Stacking method)

<table>
<thead>
<tr>
<th>Die stacking</th>
<th>Chip on Substrate (POR)</th>
<th>Chip on Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interposer</td>
<td>Use of finished interposer</td>
<td>Use of full thickness interposer (before MEOL)</td>
</tr>
<tr>
<td>Top die attach method</td>
<td>Mass reflow (preferred) and TC bonding</td>
<td>Mass reflow</td>
</tr>
</tbody>
</table>

### Positivies
- Leverages std. flip chip process
- Intermediate test and flexibility in stacking
- Possible cost reduction when high yield & throughput is possible

### Negatives
- Warpage management required
- Slow interconnection if TC attach is required
- Expensive BOM & high investment
- Requires warpage control for molded wafer
- Top die must be smaller than bottom die
Technical Challenges _ BEOL yield (Chip Attach & Stacking)

- CoS will utilize current flip chip infrastructure with high flexibility
- CoW can be considered as a low cost option: Requires very high MEOL yield
Technical Challenges _ BEOL yield (Chip Attach & Stacking)

• Interposer warpage control
  – Finished interposer from foundry (with high warpage)

– Full thickness interposer from foundry + Interposer MEOL at Amkor
Technical Challenges _ Thermal performance

- Where should heat go?
- Logic die generates hot spots and memory is sensitive to heat

**Baseline case - $\theta_{JA}$ model, still air, ambient = 50°C**
(13 mm lid size, 0.2 mm lid thickness, TIM = 3 W/m-K, Burst ON, P = 6.91W)

Source: Amkor simulation
Technical Challenges _ EM performance

Source: "Challenges for 3D Ics and Systems", Workshop, November 28-29, Toulouse, France
Technical Challenges _ Reliability performance

- IMC crack
- IMD crack
- Interfaces delamination
- Solder consumption
- 3D TSV package
- Failure in Through Silicon Via
- Liner/barrier damage
- Interface delamination
- Void
- Thin die crack
Technical challenges _ MEOL integration

**Yield Management**
2.5D: 65 dice/wafer -> 1.5% yield loss / die  
3D: 420 dice/wafer -> 0.24% yield loss / die  
Cumulative yield  
FS bump (99%) x MEOL (99%) x BS bump (99%) x assy (99%) = 96% (?)

**Cumulative TTV Management**
Process design optimization  
No exposure of silicon at CMP

**Backside Passivation Control**
Film thickness, film property (Mechanical, Electrical), RI  
Film stress: Balance for die warpage

**Cleaning Enhancement**
Huge amount of TSV: Keep high cleanliness of revealed TSV tips  
Reconsidering controlled particle size

**Backside Redistribution and Repassivation**
Passivation integrity: inorganic layer vs. organic layer
Technology Challenges _ Test

- Testing required prior to committing memory to package stack
  - Largest BOM content = Memory in this construction