Packaging
One Key for System Integration

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Intel Mobile Communications
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• System Integration
  • Chip/Package Co-Design
  • Side by Side SiP
  • Stacking
    o Package on Package Stacking
    o 2.5D Interposer Stacking
    o 3D Stacking
• Modules
• Summary
Intel Mobile Communications GmbH (IMC) is a subsidiary of Intel Corporation

IMC develops and markets innovative semiconductor products and solutions for mobile communications

Intel Mobile Communications provides mobile platform solutions for all market segments: from cost-efficient 2G/3G single-chip platforms for ultra-low-cost mobile phones and entry-level smart phones, through to leading-edge 3G and 4G slim modem and RF solutions for smart phones and tablets
### Mobile Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Brick Phone</th>
<th>Candy Bar</th>
<th>Feature Phone</th>
<th>Smart Phone</th>
<th>Touch Phone</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1980</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1990</td>
<td></td>
<td></td>
<td></td>
<td>GPRS, HSPDA, Wi-Fi, Emails driver, Gadget</td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Brick Phone**
- GSM, CDMA, TDMA, iDEN
- Small size
- SMS service

**Candy Bar**
- GSM, CDMA, TDMA, iDEN
- Small size
- SMS service

**Feature Phone**
- GPRS, HSCSD
- Data capable
- Camera & MMS
- Mass adoption

**Smart Phone**
- GPRS, HSPDA, Wi-Fi
- Emails driver
- Gadget

**Touch Phone**
- GPRS, HSPDA, EVDO, Wi-Fi, LTE
- Sensors, MEMS
- Media Platform
- All about web...
Worldwide Device Shipments

PCs shipped
- 2002: 1 bn
- 2007: 2 bn
- Today: ~3.5 bn

PCs installed
- 1.5 billion installed PCs today (2 bn in 2015)

Mobile Phones
- ~6 bn mobile phone subscriptions worldwide at the end of 2011

IDC predictions

PC = desktop, notebook & server
Smart vs. Regular

Mobile device sales [mio]
(end users Western Europe)

<table>
<thead>
<tr>
<th>Year</th>
<th>Total Sales</th>
<th>Regular Handset</th>
<th>Smartphone</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008</td>
<td>196 mio</td>
<td>157 mio (80%)</td>
<td>38 mio (20%)</td>
</tr>
<tr>
<td>2009</td>
<td>204 mio</td>
<td>132 mio (65%)</td>
<td>72 mio (35%)</td>
</tr>
<tr>
<td>2010</td>
<td>215 mio</td>
<td>98 mio (45%)</td>
<td>118 mio (55%)</td>
</tr>
<tr>
<td>2011</td>
<td>223 mio</td>
<td>69 mio (31%)</td>
<td>154 mio (69%)</td>
</tr>
</tbody>
</table>

Source: Gartner, Roland Berger analysis
Smartphones

Smartphone Functionality

Context / Location
- Navigation, guiding
- Internet

Browsing / Apps
- Internet

Gaming
- YouTube

Social Networking
- AIM
- Facebook

Functionality
- Small dimensions
- Increasing no. of sensors, MEMS
- Multiple Bands, connection types
- High computing performance (multi-core)
- Low power consumption/long battery life

High density packaging
- Higher performance
- Less power,
- Smaller size
- Lower cost.

“More Than Moore”
Moore’s Law Scaling can not maintain the pace of progress

In the past: scaling geometries enabled improved performance, less power, smaller size, and lower cost.

Today: scaling alone does not ensure improvement of performance, power, size and cost.

The primary mechanism to deliver “More than Moore” will come from integration of multiple circuit types through SoC and SiP.

SiP will allow the efficient use of three dimensions through innovation in packaging technology.
Optimum trade-offs need to be found

More Moore

- By shrinking of CMOS
  - Performance
  - Miniaturization
  - Power supply
  - Scaling rules
  - Integration density

was improved

This has changed…

More than Moore & High value system

- Packaging has become the limiting element in system cost and performance
- The assembly and packaging role is expanding to include system level integration functions.
- As traditional Moore’s law scaling become more difficult innovation in assembly and packaging can take up the slack.
Driving Factors of Package Development

Cost
- Packaging cost
- Test cost

Dimensions
- Package height \( \downarrow \)
- Lateral dimensions \( \downarrow \)

I/O Density
- Pitches \( \downarrow \)
- No standards
- Small chips/high no. of I/Os

Advanced Packaging
- Batch processing
- High parallelism
- Improved test concepts
- Smallest package heights
- Minimum-lateral area
- Min line length
- Multilayer RDL
- Reduced no. of interconnects
- Improved chip to board coupling

Electrical Performance
- Interconnect line length \( \downarrow \)
- Operating frequencies \( \uparrow \)
- Package Speed \( \uparrow \)
- Parasitics

Functionality (System Integration)
- 3D
- System in Package
- Integrated Passives (incl. system benefit)

Thermal Performance
- Power consumption \( \uparrow \)
- Package Density \( \uparrow \)
Mobile Application Package

Trends

- Package down-sizing
- Higher substrate utilization
- Better electrical performance

Flip Chip BGA
- Down-sizing potential
- Better thermal and electrical performance
- Cost reduction potential
- Minimum SiP cost adder

Wire Bond BGA

Wafer Level BGA
- Performance (f2f)
- Stacking
- Passives embedding

Embedded Die
1) **Reconstitution** of dies to "artificial" wafer
   - Single die or several (different) dies, actives and passives
   - Usage of FE-tested-good-dies (yield)
   - Materials well-known in BE technology
   - Reconstituted wafer is starting point for thin film technology

2) **Redistribution**
   - Using thin-film-technologies
   - Using standard thin-film equipment
   - Using commercially available materials

3) **Ball Apply and Singulation**
   - Standard backend assembly flow (and equipment)

4) **Test, Mark, Scan, Pack**
   - Standard or wafer level based test flow
   - Standard assembly
eWLB (embedded Wafer Level Package)

⇒ More than 600Mio components sold
System Integration

“System integration brings together the component subsystems into one system and is ensuring that the sub-systems function together as a system”

Important:

⇒ Co-Design ... for the design optimization of the system

Integration by:

⇒ Side-by-side SiP
⇒ Stacking
  ⇒ Embedded Package Technologies ... inherent stacking possibility
  ⇒ Package on Package (PoP) stacking ... test and burn-in capability and external supply
  ⇒ 2.5D Interposer Stacking ... half way to stacking
  ⇒ Die stacking (actives, passives) ... the hype
⇒ Modules ... high integration
Chip-Package Co-Design

Design Challenges – we talk about…

- Many technologies (& libraries) within one project:
  different silicon tech’s – substrate / RDL – PCB – other components
- Multiple scaling domains
  cm ⇒ PCB, mm ⇒ Substrate, μm ⇒ chip, sub-μm ⇒ chip devices
- Strong interdependencies between dies, package, testing & application board
- Global design optimization required (chips – package – board/system) mainly in terms of cost, performance & time
Collaboration will lead... to cost effective solutions

Local optimization

Cooperative Co-Design

Advantages of Co-design

- Package/Board influence on system level
- Optimized performance
- Optimized matching
- Optimized system cost
  - Reduced layers
  - Less over-engineering
  - ...
- Better quality
- Shorter time to market
## System Integration

### Package Technology

<table>
<thead>
<tr>
<th>Structure</th>
<th>Example</th>
<th>eWLB based example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Side-by-Side Structure</td>
<td><img src="image1" alt="Wire bonded" />  <img src="image2" alt="Flip Chip" /></td>
<td><img src="image3" alt="Side-by-Side Structure" /></td>
</tr>
<tr>
<td>Stacked Structure</td>
<td><img src="image4" alt="Wire bonded &amp; Flip Chip" /></td>
<td><img src="image5" alt="Stacked Structure" /></td>
</tr>
<tr>
<td>With Interposer</td>
<td><img src="image6" alt="PoP, Flip Chip type" /></td>
<td></td>
</tr>
<tr>
<td>Without Interposer</td>
<td><img src="image7" alt="Through silicon via" /></td>
<td></td>
</tr>
</tbody>
</table>

The standard SiP tool box requires a complex infrastructure. The eWLB SiP tool box allows use of one single infrastructure for all SiP packages.
Side-by-Side SiP

- Typically wire bonding or flip-chip bonding technology has been used
- Enable higher data transfer rate between dies on module
- Short interconnect line length targeted
- The die-stacked structure is mostly cheaper than the side-by-side placement in terms of packaging cost

- Bringing dies close together is the key
- Package size is the trade-off
- In thin-film technology based SiPs the number of interconnects/interfaces is reduced
Embedded Die

- Stacking is an option to side-by-side SiPs
- Example of embedded die: DC/DC converter
- Interesting option for miniaturization and integration
- Basic PCB technology includes an inherent possibility of 3D stacking
- Die embedding into PCB (Printed Circuit Board) laminated substrates has been developed by a wide range of companies for several years

- DC/DC converter:
  - DC/DC converter embedded in substrate
  - Passive SMD components mounted onto substrate
  - Size benefit due to face-down mounting of converter
  - Performance benefit also possible (f2f)
## Package Technologies

Comparison – selected properties without full technology coverage

<table>
<thead>
<tr>
<th></th>
<th>Flip Chip (mass reflow)</th>
<th>Fan-Out</th>
<th>Embedded</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Chip</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimal Chip Pad Pitch (HVM)</td>
<td>120µm</td>
<td>80µm</td>
<td>175-200µm</td>
</tr>
<tr>
<td>Pad Metallization</td>
<td>No requirement</td>
<td>No requirement</td>
<td>Copper needed</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Package</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Warpage</td>
<td>Challenging</td>
<td>Low/ constant over temperature</td>
<td>Symmetrical structure needed</td>
</tr>
<tr>
<td>Via Generation</td>
<td></td>
<td>Difficult/ special flow</td>
<td>Easy/ standard process step</td>
</tr>
<tr>
<td>Line/ Space</td>
<td>20/ 20</td>
<td>20/ 20</td>
<td>20/ 20</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>General</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reliability on Board</td>
<td>Good</td>
<td>Challenging</td>
<td>Good</td>
</tr>
<tr>
<td>Supply Chain</td>
<td>Easy</td>
<td>Easy</td>
<td>Difficult</td>
</tr>
<tr>
<td>...</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

⇒ Package technology to be selected according product requirements
⇒ No “universal” package
Package on Package (PoP)

- Many flavors available in order to fulfill changing requirements for thickness, costs, reliability, warpage, pin count, power efficiency, thermal management, …
- It is the most important platform for each ACPU or AP/BB integrated solution
- Embedded chip in laminate, Fan-Out WLB PoP and TSV PoP are upcoming

**Standard PoP Package**
- 12x12mm², 1.2mm max. height

**Flip Chip (Evolution)**
- Small outline (e.g. 10.5x10.5mm²)
- Peripheral array on backside
- Strip format

**ePoP**
- Low profile, small outline
- Area array on backside
- Panel format

**eWLB-TMV**
- Low profile (1mm), small outline
- Still peripheral array on backside
- Wafer format
Sub Millimeter PoP Solution

⇒ eWLB standard flow with TMV connections
⇒ Lowest package profile with peripheral interconnects
PoP - Mounting Issues
Package Warpage over Soldering Profile

- No significant warpage over reflow profile for eWLB based PoP package
- Basis for high assembly yield
- Classical packages show issues with warpage during reflow/assembly of top package

PoP Stacking - ePoP

- Highest step for package on package:
  - Very thin package profile
  - Area array capability on package backside
  - Low package warpage for high assembly yield

- Multiple possibilities for connection in z-direction: TSV, TMV, pre-fabricated via bars (PCB, Si)

- Large package sizes remain a challenge for board level reliability (without underfill)
2.5D-Interposer

Overall Wafer-Level-Packaging demand
(In Units of 300mm wafer eq.)

<table>
<thead>
<tr>
<th>Year</th>
<th>Traditional MCM on PCB</th>
<th>2.5D Interposer</th>
<th>3D Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td><img src="image1" alt="Flip Chip &amp; Wire Bond" /></td>
<td><img src="image2" alt="2.5D side-by-side integration" /></td>
<td><img src="image3" alt="Vertical Stacking" /></td>
</tr>
<tr>
<td>2011</td>
<td><img src="image1" alt="Flip Chip &amp; Wire Bond" /></td>
<td><img src="image2" alt="2.5D side-by-side integration" /></td>
<td><img src="image3" alt="Vertical Stacking" /></td>
</tr>
<tr>
<td>2012</td>
<td><img src="image1" alt="Flip Chip &amp; Wire Bond" /></td>
<td><img src="image2" alt="2.5D side-by-side integration" /></td>
<td><img src="image3" alt="Vertical Stacking" /></td>
</tr>
<tr>
<td>2013</td>
<td><img src="image1" alt="Flip Chip &amp; Wire Bond" /></td>
<td><img src="image2" alt="2.5D side-by-side integration" /></td>
<td><img src="image3" alt="Vertical Stacking" /></td>
</tr>
<tr>
<td>2014</td>
<td><img src="image1" alt="Flip Chip &amp; Wire Bond" /></td>
<td><img src="image2" alt="2.5D side-by-side integration" /></td>
<td><img src="image3" alt="Vertical Stacking" /></td>
</tr>
<tr>
<td>2015</td>
<td><img src="image1" alt="Flip Chip &amp; Wire Bond" /></td>
<td><img src="image2" alt="2.5D side-by-side integration" /></td>
<td><img src="image3" alt="Vertical Stacking" /></td>
</tr>
<tr>
<td>2016</td>
<td><img src="image1" alt="Flip Chip &amp; Wire Bond" /></td>
<td><img src="image2" alt="2.5D side-by-side integration" /></td>
<td><img src="image3" alt="Vertical Stacking" /></td>
</tr>
</tbody>
</table>

Source: Yole Développement
2.5D-Interposer

⇒ Passive silicon interposer on BGA laminate is called 2.5D Silicon Interposer
⇒ Die(s) are placed on the silicon interposer, which is placed on a substrate interposer
⇒ Advantages:
  • Fine pitch capability of silicon interposer technology allows use of very fine pitch dies and integration of thin-film passives
  • Expansion-matching between interposer and die causing low mechanical stress for (e. g. porous) low-k-silicon technology
⇒ Trade-Off
  • Cost of Si-interposer with TSVs and multiple redistribution lines
  • Size of multi-chip-package
2.5D-Interposer Replacement

**Approach FC-eWLB:**
2.5D-interposer replacement by eWLB (for redistributing the extreme fine pitch to std. Flip-Chip-pitch) and a standard Flip Chip assembly

**Leading to a ...**

**Std. Flip Chip** approach with

- High reliability (FC comparable)
- Lower package height
- Lower cost
- Higher yield
- Existing packaging infrastructure (OSATs)

Avoid extreme fine 1st level interconnect
si interposer w/ 2-sided RDL, TSVs
2.5D-Interposer Replacement

**Approach eWLB:**
2.5D-interposer and BGA laminate replacement by eWLB

**eWLB** approach with
- Lowest package height
- Lowest cost (no bumping, substrate, Si-interposer)
- Highest yield
- Existing packaging infrastructure (OSATs)

2nd level reliability due to large package size is challenging
3D Stacking

Why 3D Stacking?

- **Higher electrical Performance**
  Shorter and less interconnects, lower parasitics, higher bandwidth

- **Smaller Form Factor**
  Small lateral dimensions, low package height, higher density

- **Heterogeneous integration**
  Integration of different functional layers (RF, memory, logic, MEMS, ...) based on different optimized process nodes

- **Shorter Time-to-Market**
  Capability to partitioning, reusable (die-level) building blocks

- **Lower Development, Tooling and Unit Costs**
  In high volume production

- **Die-Level Modularity Reduces Risk**
  Modularity reduces the risk of failure.
## 3D TSV Applications
### Status, Drivers, and Barriers

<table>
<thead>
<tr>
<th>Application</th>
<th>Driver</th>
<th>Status</th>
<th>Barrier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image Sensors</td>
<td>Performance, form factor</td>
<td>Production</td>
<td>None</td>
</tr>
<tr>
<td>CPUs &amp; memory</td>
<td>Performance</td>
<td>16nm silicon and beyond</td>
<td>Cost, process, yield, infrastructure</td>
</tr>
<tr>
<td>CPUs &amp; memory</td>
<td>Performance</td>
<td>2014</td>
<td>Cost, process, yield, infrastructure</td>
</tr>
<tr>
<td>FPGAs</td>
<td>Performance</td>
<td>2014</td>
<td>Cost, process, yield, infrastructure</td>
</tr>
<tr>
<td>Wide I/O memory with Logic</td>
<td>Performance (bandwidth, lower power consumption)</td>
<td>2012-2013</td>
<td>Cost, process, yield, KGD, infrastructure</td>
</tr>
<tr>
<td>Memory (stacked)</td>
<td>Performance, form factor (z)</td>
<td>2012</td>
<td>Cost, process, yield, assembly</td>
</tr>
</tbody>
</table>

⇒ TSV Applications in production with backside vias for Image sensors, MEMS, LED
⇒ 3D IC Research and prototypes in memory, wireless applications (Wide I/O), high-speed logic (processors, FPGAs)

Source: TechSearch International, Inc.
eWLB Module

Realization of a Total Solution…

⇒ **Multi chip**: 2 chips side by side
⇒ **Dual side**: through mold compound vias
⇒ **Module**: passives, filters, packages on backside

Source: Yole Development
Summary

• Performance and power efficiency are main requirements of a growing mobile market
• System Integration will help to achieve these requirements
• Packaging is one key to solve the challenges of System Level Integration
• There is no „universal“ package technology
• Fan-Out Wafer Level Packaging is offering a broad range of possibilities for System Integration and will therefore be one packaging technology of the future
Thank you for your attention!

Mobile and Communications Group