Semiconductor Equipment Assessment

An enabler for production ready 450 mm equipment
Outline

- Introduction
- History of SEA - Semiconductor Equipment Assessment
- Semiconductor Equipment Assessment
- Assessment Activities - Examples
- 450 mm Equipment Assessment
- Summary & Outlook
Introduction

SEA programs proven principle:

• Take novel, innovative and promising equipment, that has left the R&D phase, into a joint assessment activity

• Collaboration of equipment supplier, end-user and research institute to perform assessment experiments for one specific equipment and finally develop the equipment according to the end-user’s specifications

• Bridge the well-known gap between the phase of having an engineered tool available and finding the “first user” for it
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SEAL
06/2010 - 09/2013

SEA-NET
01/2006 - 06/2009

SEA4KET
11/2013 - 10/2016
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Objectives

- Strengthening the European equipment industry
- Bring together critical mass of research and development power to form synergies
- Make use of the excellent European research infrastructure at Fraunhofer IISB, LETI and IMEC
- Increase the chances for SME’s to get access to IC makers
- Developing a common strategy for key enabling technologies in the EU
- Stimulate an approach to initiate sustaining partner-ships amongst equipment industry, IC industry and research institutions
- Sustainable research and development as horizontal activities
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Semiconductor Equipment Assessment for NanoElectronic Technologies - SEA-NET

Partners: 30

Equipment manufactures:

End-user:
- Infineon (Munich, Villach), Qimonda, NXP Semiconductor (Crolles, Netherlands, Belgium), STMicroelectronics Crolles II, MCRT Micro CleanRoom Technology, SOITEC Silicon On Insulator, Siltronic, MEMC Electronic Materials

R&D institutes:
- Fraunhofer IISB, Interuniversitair Micro-Elektronica Centrum, COMMISSARIAT À L'ENERGIE ATOMIQUE, University of Applied Science Wiener-Neustadt

Duration: January 2006 – June 2009
Area Layer processes / Materials

SP2: PULSION

Pulsion 32 nm – Pulsed Plasma Immersion Ion Implanter for USJ Fabrication of sub 32 nm Next Generations of Transistors

Fabrication of an industrial version of “PULSION®” (Pulsed Plasma Immersion Ion Implanter) for extension of 32 nm node S/D fabrication and surface engineering of gate stack optimization

Benefits of Pulsion

Small footprint, 200 - 300 mm compatible, cost effective plasma implanter for

- Ultra Shallow Junction
- Trench doping, 3D doping
- Thin dielectric modification
- Nanoprecipitate synthesis
- Hydrogen implantation

Partners: IBS, CEA-LETI, STMicroelectronics Crolles II
Area Layer processes / Materials

SP3: RACING

RACING – Ruthenium Atomic Vapor Deposition Competitiveness in Nanoelectronic Device Generations

Newly developed deposition equipment for the manufacturing of highly innovative metal electrode systems required for the fabrication of future nanoelectronic devices in nearly all IC applications.

Benefits of Ruthenium
- Base resistivity
- Thermal stability
- Favorable work function for PMOS transistors
- Simple structuring with subtractive processes (masking and etching)

Benefits of Ru(II)Oxid
- Good diffusion barrier

Partners: AIXTRON, Fraunhofer IISB, Infineon Munich

AIXTRON Tricent® AVD® Reaction Chamber
Area Layer processes / Materials

SP5: LDD

LDD - Linear Dynamic Deposition PVD for Production of Metal Gate Electrodes in Combination with High-k Gate Dielectrics

Linear PVD magnetron deposition and linear movement of wafer for investigation of metal gate production using the LDD PVD

Benefits of LDD

- Short target-substrate distance
- Good coating efficiency
- Thickness adjusted by wafer speed
- Tight control & repeatability
- Multi-directional coating
- Smooth films and interfaces

Partners: Singulus, Qimonda, Fraunhofer IISB
Area Layer processes / Materials

SP6: EXCALIBER

EXCALIBER - Extreme Scaling of Low-k dielectric for sub 45 nm BEOL Roadmaps

ASM Eagle 12 cluster with Aurora ELK HM (extreme low-k, high modulus) PECVD chamber and UV cure chamber

Benefits of EXCALIBER

• Production worthiness of CVD low-k deposition tool for $k = 2.5$ and $E > 8$ GPa for 45 nm
  ($k$: Permittivity; $E$: Young's modulus)
• High potential of CVD low-k with $k = 2.3$ and $E > 4$ GPa for 32 nm node

Partners: NXP Belgium NV, IMEC, sub-contractor ASM-I
Area Layer processes / Materials

SP7: Pro-Nano

Pro-nano –
A Process Tool for Nanotubes and Nanowires in IC Technology
Validation of a tool set and processes for depositing of nanotubes and nanowires required for next generations of nonconventional silicon-based devices

Benefits of Pro-nano:

- ZnO nanorods growth
- Growth of mono–crystalline, <111> oriented Si nanowires
- In-situ growth of carbon nanotubes (CNTs) without exceeded current CMOS thermal budgets

Partners:
Oxford Instruments Plasma Technology, IMEC
Area Cleaning / Etching / Automated handling

SP8: SIWAC

SIWAC
Front-End-Of-Line Single-Wafer Cleaning
Development and implementation of ammonium-peroxide mixture (APM) based single wafer cleaning with Megasonic agitation

Benefits of SIWAC
• High cleaning efficiency
• Short process times
• Flexible process integration: e.g. SC-1, SC-2, DHF last

Partners: SEZ, IMEC, NXP Netherlands, Qimonda
Area Analysis / Metrology

SP11: LEAD-IT

LEAD-IT
Low Energy and Dose Implant Test

Use of junction photo-voltage to measure sheet resistance; capacitive pick-up electrodes measure the lateral voltage drop in implanted or epi layers

Benefits of LEAD-IT
- Fully automated 300 mm metrology tool for the measurement of sheet resistivity
- Non-contact metrology
- Non-destructive
- High speed
- High resolution

Partners: Semilab, Fraunhofer IISB, ST Microelectronics Crolles II, NXP Crolles R&D

Sheet resistivity pattern of implanted layer
Area Advanced Assembly

SP15: TLS-Dicing

TLS-Dicing – Dicing System based on Thermal Laser Separation

Application of the industrial approved TLS dicing principle (separating electro ceramics and flat panel display glass) to semiconductor manufacturing backend

Benefits of TLS-Dicing

- No chipping ➔ better mechanical properties
- “Zero gap” ➔ higher yield (dicing street 50...100 ➔ 20...30 µm)
- Clean edges ➔ better electrical & optical properties
- No particles ➔ no cleaning required
- Increased speed ➔ higher throughput and reduced CoO

Partners: Jenoptik Automatisierungstechnik, Infineon Villach, Fraunhofer IISB
Semiconductor Equipment Assessment Leveraging Innovation - SEAL

**Partners:** 35

**Equipment manufactures:**
- Hamatech
- Adixen Vacuum Products
- Jenoptik Automatisierungstechnik
- SUSS MicroOptics
- Reinhardt Microtech
- SUSS Microtech Lithography
- MAPPER
- Toppan Photomasks
- HQ-Dielectrics
- Ion Beam Services
- Nanda Tech
- Semilab Semiconductor Physics Laboratory
- Fries R&T
- Applied Materials
- Integrated Circuit Testing
- Oxford Instruments
- Metryx
- PVA TePla Analytical Systems
- KLA-Tencor
- Protec Carrier Systems

**End-Users:**
- Global Foundries
- Infineon
- Intel
- LFoundry
- MEMC Electronic Materials
- Numonyx
- Siltronic
- STMicroelectronics
- Crolles

**R&D institutes:**
- COMMISSARIAT À L'ÉNERGIE ATOMIQUE
- Fraunhofer IISB
- INTERUNIVERSITAIR MICRO- ELECTRONIC CENTRUM
- University at Albany
- Catalan Institute of Nanotechnology
- University of Applied Science Wiener-Neustadt

**Duration:** June 2010 – September 2013
SEAL SP2 - EUVMTP
HamaTech EUV Mask Track Pro

Short description:
- Implementation of cleaning technique for backside contamination on EUV masks
- Assessment of software and hardware for high volume EUV production

Advances proposed in EUVMTP
- MaskTrack Pro for Next Generation Lithography installed at imec to address the **stringent requirements for EUV masks** including; back-side cleaning, preservation of vulnerable layers, avoidance of carbon growth and an EUV-specific load port for Alpha Demo Tool reticles

Main focus
- Intrinsic cleanliness of the MaskTrackPro tool platform
- EUV reticle back-side particle removal process as back-side particles are a specific concern for EUVL to meet the overlay targets;
- Hardware and software reliability verification meeting high volume EUV manufacturing

**Partners:** HamaTech, imec, Intel
**Coordinator:** Peter Dreß / HamaTech
**Duration:** 12 Months
SEAL SP5 - MAPA
MAssively PArallel electron beam lithography

Short description:
- Assessment by simulations and experiments
- Parallel e-beam lithography for 32nm (22nm logic) node Integration into mask maker
- Assessment of infrastructure (process, data flow and proximity effect correction)

Advances proposed in MAPA
- Multi Beams tools are today under development in the European project MAGIC.
- MAPA will be perfectly aligned with MAGIC allowing the installation and assessment of the Mapper platform in a production like environment.
- Tool performance will be upgraded from the alpha level (45nm hp, small field, 0.1 WPH) to Beta level (32 nm hp, 1 WPH, full field).
- Infrastructure will be evaluated for both semiconductor manufacturing and mask making applications.

Partners: MAPPER Lithography, CEA/LETI, STMicroelectronics Crolles, Toppan Photomasks
Coordinator: Bert Jan Kampherbeek / MAPPER
Duration: 24 Months

MAPPER tool @ CEA-Leti
SEAL SP10 - IMDI

Innovative Meso Defect Inspection

Short description:
- Implementation of new very high throughput and high sensitivity approach for wafer inspection
- Assessment for 3D-Integration (TSV), patterned and un-patterned wafer inspection

Advances proposed in IMDI
- Combines bright field illumination, dark field illumination with **full wafer illumination without movement of the wafer**
- Bright or dark field images of the full 300mm wafer are captured in one shot at high sensitivity of 1-10µm
- Use of full-wafer imaging permits for a first time to **rapidly inspect** every processed wafer at 100% of the surface
- SW algorithms to extract the defects of interests reliably and to automatically identify defect signatures are being optimized during the project

**Partners:** Nanda Technologies, STMicroelectronics Crolles, imec, Fraunhofer IISB

**Coordinator:** Johannes von Borries / Nanda

**Duration:** 22 Months
SEAL SP12 - WISDoMP
White-light interferometer system for the development of 300 mm wafer mechanical processes on the nanometre scale

Short description:
- Application of white-light interferometry to assess the full surface topography of Silicon wafers
- Development and assessment of nanotopography concepts

Advances proposed in WisDoM
- An interferometric sensor with 90 mm size of field of view.
- Stitching topography maps will provide full surface information of 300 mm silicon wafers.
- High-pass filtering of the surface information will enable nano-topography assessment
- Reliable characterization of large areas of polished, lapped and ground surfaces.
- Application will not be limited to silicon wafers only.

Partner: Fries Research & Technology, Siltronic, Fraunhofer IISB
Coordinator: Thomas Fries / FRT
Duration: 16 Months
SEAL SP13 - MCEB (Multi Column E-Beam)
High Resolution Multi Column E-Beam Wafer Inspection – Prototype Assessment at Wafer Fab Production Floor

Short description:
- Assessment of E-Beam inspection technology meeting resolution and throughput requirements of 22nm node
- Tool improvements based on fab feedback

Advances proposed in MCEB
- A high resolution E-Beam defect inspection tool for the 22nm node and below
- Production worthy throughput will be reached with a Multi Column E-Beam inspection tool.
- High resolution is targeted having the required sensitivity for high capture rate defect detection and will be evaluated for defect monitoring in critical layers

Coordinator: Yoram Uziel / AMIL
Duration: 36 Months

The Elite Multi Column e-Beam inspection tool (right) and the Multi Column module (left)
Semiconductor Equipment Assessment for Key Enabling Technologies – SEA4KET

**Partners:** 27

**Users:**
- Intel Electronics, E+H Metrology, Freiberg Instruments, Peter Wolters, INFINEON TECHNOLOGIES, STMICROELECTRONICS CROLLES 2, GLOBALFOUNDRIES, ASM BELGIUM

**Equipment Suppliers:**
- LAM RESEARCH, ASM INTERNATIONAL, ZIMMERMANN & SCHILP HANDHABUNGSTECHNIK, MECHATRONIC SYSTEMTECH-NIK, HAP Handhabungs-, Automatisierungs- und Praezisionstechnik, ADIXEN VACUUM PRODUCTS, KLA-TENCOR, APPLIED MATERIALS ISRAEL, Fraunhofer IISB, RESEARCH CENTRE FOR NATURAL SCIENCES, HUNGARIAN ACADEMY OF SCIENCES, CMD, EV GROUP E. THALLNER, BRUKER, HQ-Dielectrics, Jenoptik Automatisierungstechnik

**Research Institutes:**
- Fraunhofer IISB, Interuniversitair Micro-Elektronica Centrum, COMMISSARIAT À L’ÉNERGIE ATOMIQUE, NEDERLANDSE ORGANISATIE VOOR TOEGEPAST, University of Applied Science Wiener-Neustadt

**Duration:** November 2013 – October 2016
Semiconductor Equipment Assessment for Key Enabling Technologies – 450 mm
Cross-cut R&D
Sustainable Support and Research and Development

• Development of procedures and an infrastructure to exchange wafers between project partners allowing multi-site processing or characterization

• Research on manufacturing science, including the development of APC, VM and PdM modules at equipment level, equipment design and equipment efficiency

• Evaluation of resizing technologies especially for, but not limited to, 450 mm wafers in order to fit in subsequent process or metrology equipment

• Application of “Best Practice” learning techniques
SP3 - SWCC450
Single Wafer Critical Cleaning 450 mm

• Evaluation of a wafer spin wet processing tool for 450 mm

• Target applications:
  – Pre furnace clean
  – Pre ALD clean
  – Pre epi clean
  – Dielectric etch
SP4 - ABP

Advanced Batch Processing

• Assessment of a 450mm batch oxidation system

• Optimization of:
  – Process results
  – Repeatability
  – Cleanliness
  – Reliability aspects

• Investigation of thermal processing behavior of 450mm wafers (stress, deformation)
Critical Wafer Handling

- Definition of requirements for clean wafer handling and specifications of test environments for the wafer spec regime (450mm standard thickness, <=300mm (ultra-) thin) = target wafer spec regime
- Adaption of current end-effector technologies for clean handling to target wafer spec regime
- Integration in assessment environment (cluster-platform and handling demonstrator/load ports)
- Joint Assessment of different end-effector technologies in terms of performance in different test environments
- Identifying suitable clean handling technologies as a function of production processes
SP6 - AMLL450

Vacuum transportation interface for 450mm architecture

• Assessment of a new interface system for vacuum transportation and storage of 450 mm wafers by
  – Integrating and experimentally assessing an adixen vacuum carrier and interface system on a handling platform for 450mm wafers at FhG IISB
  – Generally assessing the system in 450 mm fab environment (including investigation of impact on fab and equipment architecture)
SP7 - MULTI

Combined film metrology and diffraction-based CD/Shape Metrology for 10nm CMOS technologies on 450mm wafers

• Evaluation of novel KLA-Tencor Film/CD 450mm optical metrology platform with respect to
  – 14nm/10nm technology node
  – III-V gate channel materials introduction
  – FinFET technology

Materials for 10nm node and FinFET architecture
SP8 – 450DM
450mm Defects Metrology for Process and Materials Characterization and Qualification

- Defectivity protocol and baseline creation with a 450mm defect review (450DR) tool’s material analysis module (EDX) (part of the 450mm Pilot Line at imec)
SP9 - MetroCom

Metrology Components

• Construction of an open platform that serves as evaluation stand for different metrology components
• Feasibility evaluation of three novel, complementary metrology components in an automated, industry compliant environment by use of that open platform:
  – MDPmap OEM measurement head for scientific and production-related electrical characterization of 450 mm wafers including carrier lifetime metrology
  – Line-based ellipsometry setup for spectroscopic polarization optical line image and mapping of 450 mm wafers
  – Sensor for topography inspection of 450 mm wafers

Open evaluation platform for metrology components: Existing cluster platform shown in black; to be constructed versatile module shown in red.
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Markus Pfeffer
Fraunhofer Institute of Integrated Systems and Device Technology
Erlangen, Germany
markus.pfeffer@iisb.fraunhofer.de

• www.seal-project.eu
• www.sea4ket.eu

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Thank you!