Agenda

>Introduction
   Ibiden Products Over View and Technology Trend.
   Embedding technology and Expectation.

>Embedded Device Technology
  #1. Embedded MLCC in FCCSP Substrate.
  #2. Embedded Active Device.
  #3. Embedded Thin Film Capacitor in FCPKG Substrate
  #4. Embedded Active Device as 2.5D solution.

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Summary
Ibiden Business Area and Technology Trend

FCPKG

2.5D

High BW / Low PW

Embedded (MLCC/Thin Film Cap)

FCCSP

2.5D

High BW / Low PW

Embedded (MLCC)

3D

Coreless / e-TFC

PWB

High Thermal Conductivity

High density is required for all area.
Higher data processing, Higher Bandwidth, Signaling

Higher TDP

Thinner POP, Si Integration

DCA, TSV, 3D, Module

e-Active/passive in PWB

Thinner / well-control’d warpage PWB w/ High density routing and thermal conductivity is needed.
Expectation for Embedded Technology

**High Performance Computing**
- Embedded Active Device as 2.5D
- Embedded Thin Film Capacitor for High BW / Low PW

**Mobile Performance Computing**
- Embedded M LCC for Higher PW efficiency
- Embedded Active Device for High dense Module
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High Performance Computing

Embedded Active Device as 2.5D

Embedded Thin Film Capacitor for High BW / Low PW

Mobile Performance Computing

Embedded MLCC for Higher PW efficiency
**Embedded M LCC for Higher PW efficiency**

Power = k \times C \times f (Clock freq.) \times (Vdd)^2

*Higher clock frequency*

*Power Integrity Improvement*

*Decoupling cap underneath Die \( \hat{E} \)  Lower Vdd noise \( \check{E} \)  Lower Vdd \( \check{E} \)  Lower Power/High speed*
Reliability Test Results of FCCSP w/ embedded M LCC

MLCC embedded substrate passed the general reliability requirement.

Pre-conditioning : 125 deg.C/24hr (Bake) + 60 deg.C/60%RH/40hr(MSL3a)

<table>
<thead>
<tr>
<th>Test item</th>
<th>Standard</th>
<th>Test Condition</th>
<th>N</th>
<th>Success criteria</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moisture Reflow Sensitivity</td>
<td>J-STD-020</td>
<td>Lead free Reflow (Peak 260degC) / 5times</td>
<td>10units</td>
<td>No delamination (T-SAM)</td>
<td>No Mechanical and Electrical failure.</td>
</tr>
<tr>
<td>Temp. Cycle</td>
<td>JESD22-A104</td>
<td>-55 to 125deg.C / 500cycle</td>
<td>10units</td>
<td>R-shift &lt; 10%</td>
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# Experience of Embedded Active Device

![Cross section of manufactured sample](image)

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Substrate</strong></td>
<td></td>
</tr>
<tr>
<td>Unit size / Thickness</td>
<td>4.0x3.5mm / 0.38mm</td>
</tr>
<tr>
<td>Layer count / Thickness</td>
<td>4Layers (1-2-1)</td>
</tr>
<tr>
<td>Array size</td>
<td></td>
</tr>
<tr>
<td></td>
<td>62mm</td>
</tr>
<tr>
<td></td>
<td>230mm</td>
</tr>
<tr>
<td></td>
<td>230x62mm (728 Units/Array)</td>
</tr>
<tr>
<td><strong>Active Device</strong></td>
<td></td>
</tr>
<tr>
<td>Size / Thickness</td>
<td>3.0x2.5mm / 0.2mm</td>
</tr>
</tbody>
</table>
Reliability Test Results and Control Warpage

No issue at general reliability test.

<table>
<thead>
<tr>
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</tr>
</tbody>
</table>

Warpage measurement result of substrate Array.

<table>
<thead>
<tr>
<th>Tech.</th>
<th>Current</th>
<th>Improved</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contour image</td>
<td><img src="image" alt="Contour Image" /></td>
<td><img src="image" alt="Contour Image" /></td>
</tr>
<tr>
<td>Diagonal image</td>
<td><img src="image" alt="Diagonal Image" /></td>
<td><img src="image" alt="Diagonal Image" /></td>
</tr>
</tbody>
</table>

CTE mismatch b/w organic substrate and Silicon device causes the warp. Warpage reduce technology improved the Array warpage.
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**Mobile Performance Computing**

Embedded M LCC for Higher PW efficiency

Embedded Active Device for High dense Module
Embedded Thin Film Capacitor in the Substrate

3. Development Item
Embedded Thin Film Capacitor (TFC) PKG

Embedded thin film capacitor formed with metal foils, to establish > 3uF capacitance in build-up layers.
## Embedded Thin Film Capacitor in the Substrate

### 4. Emb. Cap Material in the market

<table>
<thead>
<tr>
<th>Process / Form</th>
<th>Thick Film</th>
<th>Thin Film</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Film</td>
<td>Paste</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>45</td>
<td>20</td>
</tr>
<tr>
<td>Dielectric Thickness (µm)</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Capacitance (µF/cm²)</td>
<td>0.002</td>
<td>0.009</td>
</tr>
<tr>
<td>Tolerance</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Loss Tangent</td>
<td>0.02</td>
<td>-</td>
</tr>
<tr>
<td>Breakdown Voltage (V)</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Embedded Thin Film Capacitor in the Substrate

5. Embedded Process Flow

1. Bare TFC Material

2. Bottom electrode patterning

3. TFC Lamination

4. Top electrode patterning for Via

5. Via formation

6. Filled Via Cu plating and patterning

7. Insulation Lamination & Via formation

8. Cu Plating and build up layer pattern

→ Build Up process
Embedded Thin Film Capacitor in the Substrate

8. Die Assembly Results

<table>
<thead>
<tr>
<th># of Assembly</th>
<th>Assembly Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>330/331</td>
<td>99.7%</td>
</tr>
</tbody>
</table>

No issues in Assembly. Yields is very high.
Embedded Thin Film Capacitor in the Substrate

9. Simulation of Electrical Performance

To obtain the same electrical performance as embedded TFC Package, 50 chip caps are needed LSC in current package structures.
Embedded Thin Film Capacitor in the Substrate

10. Actual of Electrical performance

- Calculated impedance from voltage by signal generator
- 70% improved compared to current products
11. Reliability evaluation result - TSC -

Test condition: -65C to 150C  
Success criteria: Resistance shift < 10%

<table>
<thead>
<tr>
<th>Leg</th>
<th>Sample size</th>
<th>Initial</th>
<th>100</th>
<th>200</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>PKG only</td>
<td>20pcs</td>
<td>OK</td>
<td>20/20</td>
<td>20/20</td>
<td>20/20</td>
</tr>
<tr>
<td>Die attached PKG</td>
<td>30pcs</td>
<td>OK</td>
<td>30/30</td>
<td>30/30</td>
<td>30/30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NG</td>
<td>-</td>
<td>0/20</td>
<td>0/20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

There is no issue at TSC 500 cycle.
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## Summary

### Pros and Cons of EA/EP

<table>
<thead>
<tr>
<th>Where to embedde</th>
<th>What to embedded</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mother Board</strong></td>
<td>Passive device</td>
<td>Active device</td>
</tr>
<tr>
<td>(MB)</td>
<td>• Lower component cost than active.</td>
<td>• Higher drop test reliability</td>
</tr>
<tr>
<td></td>
<td>• Easier to guarantee function.</td>
<td>• To replace 2nd Level Interconnection</td>
</tr>
<tr>
<td></td>
<td>• Easier to keep component performance in process</td>
<td>✡ (ex.) 0.2mm via connection pitch to device is valuable</td>
</tr>
<tr>
<td></td>
<td>• MB size need to be shrunk enough to compensated cost adder of process and component for embedding. But normally embedding area is too small of MB to compensated cost adder.</td>
<td>• Need very high process yield not to kill expensive active device.</td>
</tr>
<tr>
<td></td>
<td><strong>Con's.</strong></td>
<td>• Need close relationship btw device / board / application business to guarantee device performance</td>
</tr>
<tr>
<td><strong>Package Substrate</strong></td>
<td><strong>Pro's.</strong></td>
<td><strong>Con's.</strong></td>
</tr>
<tr>
<td>(PKG)</td>
<td>• Embedding in large area of substrate to compensated cost+ for embedding.</td>
<td>• No significant con's.</td>
</tr>
<tr>
<td></td>
<td>• Expected price is higher than MB case.</td>
<td>(In addition to Mother board case,)</td>
</tr>
<tr>
<td></td>
<td>• Easier to find business benefit.</td>
<td>• Need to replace 1st Level Interconnection</td>
</tr>
<tr>
<td></td>
<td>✡</td>
<td>✡ (ex.) 0.2mm via connection pitch to device is not enough</td>
</tr>
<tr>
<td><strong>Con's.</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Challenge

Where we are?

The Valley of Death

by Congressman Vernon J. Ehlers

The Darwinian Sea
The Struggle of Inventions to Become Innovations

“Valley of Death”

“Struggle for Life” in a Sea of Technical and Entrepreneurship Risks

by Prof. Lewis Branscomb
Challenge

Where we are?

Testing?
Component cost?
Yield loss?
Assemble LT?

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Thank you very much.