

CALL FOR PAPERS

ASMC

Advanced Semiconductor Manufacturing Conference—ASMC 2018

SEMI and IEEE invite authors to submit a technical abstract to ASMC 2018. ASMC is the leading international technical conference for exploring solutions to improve the collective microelectronics manufacturing expertise. Solving the challenges presented by semiconductor manufacturing is an ongoing collaborative effort by customers, device makers, equipment and materials suppliers, and academia. The conference provides an unparalleled platform for semiconductor professionals to network and learn the latest information in the practical application of advanced manufacturing strategies and methodologies.

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ASMC is now soliciting abstracts from professionals involved in all areas of semiconductor manufacturing. Authors of selected papers will have an opportunity to present their work at the conference. They will also receive an invitation to publish their paper in a special section of ASMC 2018, which will be featured in IEEE Transactions on Semiconductor Manufacturing.

AWARDS

- **ASMC 2018 ENTEGRIS BEST PAPER AWARD**
All papers presented at ASMC will be considered for the ASMC 2018 Entegris Best Paper Award.
- **ASMC 2018 GLOBALFOUNDRIES BEST STUDENT PAPER**
Papers authored and presented by a student or student/professor will receive special consideration for the 2018 ASMC Outstanding Student Paper competition, sponsored by GLOBALFOUNDRIES. Please indicate in the abstract if the paper will be authored by a student.

LOCATION

Saratoga Springs
New York USA

QUESTIONS

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For templates and further instructions, visit:
www.semi.org/asmc

With technical support from



IMPORTANT DATES (subject to change)

- Abstracts Due (extended):** 18 October, 2017
Author Notification: 6 December, 2017
Manuscripts Due: 5 February, 2018
Final Manuscripts Due: 2 April, 2018
Presentations Due: 27 April, 2018
Conference Dates: 30 April – 3 May, 2018

AUTHOR INSTRUCTIONS

Original, non-commercial, non-published works are being solicited in specific categories. Peer-reviewed papers are selected based on a clear outline of the problem, analysis, solution/results and conclusions. Papers co-authored between customers, device manufacturers, equipment or materials suppliers, and/or academic institutions (including students) that demonstrate innovative, practical solutions for advancing semiconductor manufacturing highly encouraged. Authors should:

- Provide an extended abstract of no more than two pages (max. of 1000 words, MS Word or PDF) with supporting data, charts, figures embedded or on the last page.
- Summarize the topic and theme in as much detail as allowed by the word count limitation. Include title, author(s), company affiliation(s), contact information, topic and five key words describing the work.
- The final paper, using the template provided on the [ASMC Author Kit](#) must show a complete set of data to support initial abstract.

Peer-reviewed papers are selected based on a clear outline of the problem, analysis, solution/results and conclusions. Authors who prefer to present in the poster session must indicate this request on their abstract.

AM: Advanced Metrology

Development of new metrology techniques and methodologies; *in-situ* monitoring methods; metrology for process control; measuring critical dimensions, overlay, films; metrology of next-generation materials, processes and architectures (TSV, FinFETs, EUV, etc.); novel extension of existing metrology tools as well as evaluation of upcoming measurement technologies to meet HVM requirements.

APEM: Advanced Equipment Processes and Materials

Development of new front- and back-end processes; characterization and integration of barrier layers, advanced gates, high-k and low-k, isolators, optical and conducting materials; evaluation of novel substrates; methodologies for driving new materials from R&D to mass production.

AP/DFM: Advanced Patterning / Design for Manufacturability

Immersion, double/multiple patterning, and EUV lithography; advanced resolution enhancement techniques; source/mask optimization; alignment and overlay enhancement solutions; advanced reticles; alternative patterning methods; high versus low volume manufacturing effect on lithography processes; computational lithography; process models and process model files; optical proximity correction and verification; design rules creation and verification; DFM in support of yield learning through product cycle; use of test structures for design rule and process window validation; early manufacturing involvement; integrated product and process development (IPPD).

APC: Advanced Process Control

Advanced control techniques such as run-to-run control; model-based control; non-linear control methods; application of advanced statistical methods to control; advanced SPC techniques; fault detection and classification (FDC); virtual metrology.

CFM: Contamination Free Manufacturing

Backside contamination; EUV lithography cleanliness; ultraclean technologies; materials; control of mini-environments; environmental factors; wafer and reticle carriers/transport; static charge control.

DM: Big Data Management and Mining

Fab and test floor data collection methods and analysis; data format, volume and interface challenges; fast drill-down to problem tools and sources; foundry-to-fabless data transfers and information issues; new visualization methods for improved data understanding; applying data mining techniques to isolate critical information from large data volumes; data ownership.

DI: Defect Inspection and Reduction

New brightfield, darkfield, e-beam and other techniques and technologies for cost-effective yield control; process development using defect detection and management; new methodologies for detection, characterization, classification and disposition of defect counts, types and distributions; diagnostic techniques to correlate in-line inspection results to product yield and defectivity.

DP: Discrete and Power Devices

Solutions manufacturers facing challenges other than smallest feature sizes, including analog/mixed-signal applications for automotive devices, power management and display drivers.

ET/ ID: Enabling Technologies and Innovative Devices

MEMS; magnetic read/write heads; micro displays, motion sensors; DLP; MRAM; organic semiconductors; silicon modulators; photonic devices; 3D gates or novel structures; biosensors; semiconductor photovoltaic challenges; new process technologies; CMP developments; novel and emerging applications of existing process techniques; carbon nanotubes; PCM.

ER: Equipment Reliability and Productivity Enhancements

Efficiency/productivity measurements; optimizing and extending fab productivity within the framework of existing wafer sizes; cycle time reduction; cost reduction; best practices; customer-supplier continuous improvement programs; high mix/high-volume factories with high-equipment productivity; small-lot manufacturing and single-wafer/mini batch tools; fab conversions; integration of factory control systems into the complete supply chain.

FA: Factory Automation

Automation in fab; probe; assembly and test factories; e-diagnostics; e-manufacturing; WIP management; scheduling; planning; logistics; modeling; productivity; supply chain management; manufacturing performance; capacity, metrics, supply/demand management; deployment, cycle time and time-to-market; fully automated factory and remote operation center equipment and equipment interfaces; data collection interfaces; automated material handling systems (AMHS) challenges and carriers; standards and standardization.

FE: The Fabless Experience

Challenges faced by fabless semiconductor companies; integrating material from multiple sources; strategies for managing risk due to supply shortages and out of spec. parts; foundry strategies for effectively supplying many customers; foundry methods for controlling costs for small orders, vis-à-vis move to 450mm wafers; related topics of general interest to fabless semiconductor companies or foundries.

GF: Green Factory

The role of environment; health and safety; emissions and effluents control; energy saving; recycling; safety and health; community involvement; ergonomics; zero emission; global environment protection; waste reduction; sustainability.

IE: Industrial Engineering

Facilities design and layout; equipment design and AMHS interactions; manufacturing systems design; statistics/quality; computer modeling; simulation; systems management; human factors in engineering; financial decision making; cost reduction; supply chain.

LM: Lean Manufacturing

Establishing flow; standards and standard work; value stream mapping; kaizen; kaikaku; cycle times; WIP; 5S; continuous improvement; metrics, training within industry (TWI); waste reduction.

MJ: MOL and Junction Interfaces

Development of middle-of-line processes from formation of transistor junctions through local interconnect processing; methods to limit the number of necessary masks; pre-clean requirements and queue-time limitations; elements affecting contact resistance including types of silicide.; control of voids and other MOL-specific yield loss mechanisms; alternate contact materials like cobalt vs tungsten extend-ability; novel ALD/CVD schemes for line and vertical resistance reduction.

SM: Smart Manufacturing

Smart manufacturing systems, equipment and technologies; supply chain modeling and networks; system integration for manufacturing integration; crowdsourcing design for manufacturing; manufacturing process simulation and optimization; information technology; smart and intelligent manufacturing processes; cloud-enabled manufacturing systems and applications; industrial Internet of Things; next-generation robotics/automation; measurement and systems monitoring; business, health & safety, processes, and cost learnings.

YE: Yield Enhancement/Learning

Yield analysis tools and methods, including identifying root cause of yield loss and reliability fails; failure analysis; defect-to-yield correlation; zonal and spatial pattern analysis; slot signature analysis; use of volume diagnostics for pinpointing net failures; determination of critical particle size and types.

YM: Yield Methodologies

Yield monitoring and modeling accuracy; model types; critical area extraction techniques; yield-targeted data mining; modeling of systematic and parametric yield; process sector analysis; short-flow yield programs.

3D/TSV: Packaging and Through Silicon Via

3D integration in general and associated topics like wire bonding, flip chip bonding (bump metallization), micro-bump bonding, C4 New Process, through wafer vias, silicon carrier; Novel approaches to global/local interconnect issues, power delivery and thermal management.