TEST VISION 2020

11th International Workshop on Test Equipment: Test Vision 2020

Moscone Center, San Francisco

July 11-12, 2018

Held in conjunction with SEMICON West 2018

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Call for Papers

Scope:

Test Vision 2020 is today's premier workshop for semiconductor and system test experts, organized with a vision towards the future of test to discuss coming trends, innovations and requirements. It is a highly-anticipated gathering of providers and users of test IP and equipment, all converging to hear and engage with leaders in the field. The conference typically has 100+ participants and is held in conjunction with Semicon West, assuring access to a wide range of expertise and experience. This year's theme is **"The Next Step to Intelligent Test."**

The growth in autonomous driving and the connected "everything" is driving the demand for semiconductors. This trend is putting more pressure on test costs as a result of higher coverage requirements or lower average selling prices. Test must become even smarter to address the increased quality demands, while at the same time remaining economical. Greater computational power coupled with increased analog and sensor content will force changes in test strategies due to more advanced packaging, heterogeneous integration, higher performance analog, and increasing RF complexity. To address those challenges, all the tools in the arsenal must be brought to bear; increasing test instrumentation integration, smarter test strategies, self-test, adaptive test, system level test, and more sophisticated test hardware.

Fresh Perspectives Wanted: With these topics as the backdrop, we intend to spark lively debate. This means picking apart the overall device production process and examining how test could in fact become its ultimate "enabler". To this end, we're seeking papers that offer thought-provoking and even controversial ideas. We especially encourage contributions from individuals that have spent time in the "test trenches.

"Moore's Law" and "More than Moore" packaging advancements still guide our roadmaps as the race for denser, larger, faster and highly heterogeneous devices continues. Now, add the near-instantaneous time-to-market imperatives and the new challenges of 7nm processes and beyond, and the test complexities intensify. This calls for new innovations in DFT, test methodologies, wafer probing technology and device manufacturing - to build valuable solutions for test IP and equipment developers, as well as tool providers and users.

So, at Test Vision 2020, we'll ask questions like this: What can we do differently to provide testing cost effectively with dppm rates approaching zero? What R & D tools are needed for today's and tomorrow's devices? What will test cell (ATE, fixtures, handlers or probers and probe cards) need to look like in 2018 and beyond? How can test be better integrated in to the manufacturing process? Are today's technologies adequate for the future? If not what can we do to close the gap?

Representative topics include, but are not limited to:

- *New market drivers and future trends*
- *Critical "future-proof" ATE capabilities*
- *Innovative Test methods for future defects*
- *2.5D/3D device testing ideas and techniques*
- *Power testing needs for 'green' technology*
- *System Level Test*
- *High-speed IO Test*
- *Automotive and Test Standards*
- *Impact of IC power management on test*
- *R & D Tools*
- *Calibration and Repair Techniques*
- *MEMs device testing*
- *New ideas in manufacturing flow optimization*
- *RF and SOC testing trends*
- *Adaptive & concurrent testing challenges*
- *Self Testing*
- *Automated test program generation*
- *Impact of new fab processes on test/manufacturing*
- *Wafer probing technologies*
- *Low-cost application focused testers*
- *Software for ATE*
- *Traceability of test information*
- *Security Impacts on Test (cyber security/test....)*

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More information available at:
www.TestVision2020.com

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Author information for papers:

To present at the workshop, authors are invited to submit an abstract at http://www.semiconwest.org/call-papers
Each submission should include: title, full name and affiliation of all authors, abstract (up to 500 words), and keywords. Identify a contact author and include a number phone and e-mail address. Authors looking to submit full papers or draft presentations may do so through the SEMICON West Call for Papers link above.

The submission deadline has been extended! **Submissions must be received no later than May 4, 2018**. Authors will be notified of the disposition of their presentation by **May 25, 2018** and must submit the final presentation by **June 22, 2018** for inclusion in the Workshop Notes, which will be provided to the attendees for download prior to the start of the workshop. Optionally, an extended abstract or full paper can be included in the notes.

Call for Posters

Owing to its continuing success, we will again include a Poster Session on **July 11, 2018**. We encourage participation by seasoned test experts, as well as students, post-docs, and others with interesting observations to share on how your test process has adapted to the ever-changing realities of test.

To participate in the poster session, authors are invited to submit an abstract at http://www.semiconwest.org/call-papers

The submission deadline has been extended! Submissions of abstract for your poster session must be received no later than **May 18, 2018**. Authors will be notified of the disposition of their poster by **May 25, 2018.**

Poster Session

The poster material must fit 1m x 1m area. The presenting author should be underlined in the poster text. Please set up your poster on **July 11, 2018** in the morning and be ready to present the content during the breaks and reception.

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