Monday, May 16, 2016
6:30-7:30 pm Welcome Reception and Registration – sponsored by FEI Company (Hilton Hotel Lobby)

Tuesday, May 17, 2016
7:30-8:30am Registration / Networking Breakfast – sponsored by Nikon Precision (City Center Lobby)
8:30  Welcome to the Conference: 2016 co-chairs - Dr. Janay Camp/KLA-Tencor and Dr. Jeanne Bickford/GLOBALFOUNDRIES; 2016 Best Paper Award Presentations
8:45  Keynote: Advanced Manufacturing... Changing Today's Paradigm
Christine Furstoss, Vice President and Technical Director, Manufacturing & Materials Technologies, GE Global Research

9:45  Networking Break

Session 1 Contamination Free Manufacturing (CFM) (sponsored by Teflon™ Fluoroplastics)
Chairs: Chris Ebert, Linde; Chris Long, IBM Research
Control of contamination on the wafer surface in process is essential to achieving critical rapid yield ramps. This session will feature papers focused on cleaning technologies and wafer handling methods to eliminate contamination and defects from wafer surfaces (top, back, edge) in order to reduce killer defects and drive yield improvement, and minimize/eliminate excursions.

10:05 1.1 Effect of Post CMP In-situ Cleaning and Its Optimization on the Defect Improvement
Hong Jin Kim, Tae Hoon Lee, Sumeet Kashyap, Venugopal Govindarajulu, Jason Mazzotti,
GLOBALFOUNDRIES

10:30 1.2 FOUP purge performance improvement using EFEM flow converter
Seong Chan Kim, Greg Schelske, Entegris, Inc.

10:55 1.3 A Solvent Free Method for Post Pad Etch Wafer Cleaning
Mohamed Boumerzoug, Freescale Semiconductor

11:20 1.4 Contamination Free Manufacturing Quality Control for Ultrafiltration of Ultrapure Water Production for High End Semiconductor Manufacturing
Jochen Ruth, Rolf Berndt, Pall GmbH

11:45 1.5 Molybdenum Contamination in BF2 High Current Ion Implantation Causing PNP Beta Variability
Aaron Smith, Peter Kurkowski, Thanas Budri, Texas Instruments

Session 2 Advanced Metrology I (sponsored by Metryx, A Lam Research Company)
Chairs: Amiad Conley, Applied Materials; Ronny Haupt, KLA-Tencor; Alok Vaid,
GLOBALFOUNDRIES
Novel processes, complex materials, shrinking process margins are putting significant pressure on measurement tool-sets. As time available to develop upcoming process node/architectures decreases, there is a drive for ever more sophisticated in-line metrology control for fast cycles of learning and process control. This session will cover several key advancements in the field of optical, acoustic & x-ray metrology.

10:05 2.1 Manufacturing Excellence using Multi-Platform Ellipsometry Thickness Measurement Fleet on Advanced Nodes
Michael Lenahan, Aloki Vaid, Sridhar Mahendrakar, Steven Seipp, David Jayez, Alice Yueh,
Sheweta Saxena, Eric Solecky, GLOBALFOUNDRIES; Samuel Gizzo, Amir Heller, Tianhao Zhang,
Da Song, Nam Hee Yoon, Janay Camp, Kartik Venkaratraman, KLA-Tencor

10:30 2.2 HRXRD for In-Line Monitoring of Advanced FDSOI Technology: Use Cases

10:55 2.3 Inline Monitoring of SiGe Strain Relaxed Buffers (SRBs) using High-Resolution X-ray Diffraction
B.L. ‘Herron, B. Mendoza, J. Frohleis, A. Reznicek, N. Loubet, J. Gaudiello,
GLOBALFOUNDRIES; Peter Gin, K.M. Matney, M. Worman, Jordan Valley Semiconductor

11:20 2.4 Poly Recess Depth in narrow Trenches measured with Scatterometry
Franz Heider, Infineon Technologies Austria AG; Chi Eng New, Kin Loon Chow, Infineon Technologies (Kulim) Sdn. Bhd.; Jeffrey W. Roberts, n&k Technology

11:45 2.5 Non-Destructive Acoustic Metrology and Void Detection in 3x50µm TSV
M. Liebens, S. Van Huylenbroeck, L. Haensel, A. Miller, E. Beyne, imec; Robin A. Mair, M.
Kotelyanskii, M. Mehdendale, X. Ru, P. Mukundhan, T. Kryman, Rudolph Technologies

12:15  Networking Lunch
**Session 3 – Session 3 – Defect Inspection I**

**Chairs:** Jeffrey Barnum, KLA-Tencor; Oliver Patterson, GLOBALFOUNDRIES

Inline defect inspection continues to enable process optimization and yield improvement. This session will focus on optical defect detection techniques for process systematics, process window discovery and expansion control, EUV reticle print check control, edge defectivity, and diversity sampling to improve defect paretos.

1:30

3.1 Line End Voids defectivity improvement on 64 pitch Cu wire interconnects of 14nm technology
Atul Bawari, Balajee Rajagopalan, Hirokazu Aizawa, Jae Choo, Ian Tolle, Ronald Huang, Shiran Xiao, Hoang Nguyen, Amit Srivastava, GLOBALFOUNDRIES; Michael M. Daino, Graham Jensen, Ankit Jain, Sumanth Kini, KLA-Tencor

1:55

3.2 Process Window Discovery Methodology Development for Advanced Lithography
Dieter Van Den Heuvel, Angelica Lee, imec; Andrew Cross, Kaushik Sah, Paolo Parisi, Oksen Baris, KLA-Tencor

2:20

3.3 Detection of Printable EUV Mask Absorber Defects and Defect Adders by Full Chip Optical Inspection of EUV Exposures Wafers
Luciana Meli, Scott D. Halle, Nelson Felix, IBM Research; Kaushik Vemareddy, KLA-Tencor

2:45

3.4 A Study on the Interaction between Barrier and Plating Causing Edge Stringer Defects in 28nm
Eswar Ramanathan, Antonio Fiacco, Mary Claire Silvestre, Val Parks, Balajee Rajagopalan, Scott Hildreth, John Barker, Jeffrey Riendeau, Jean-Baptiste Laloe, Frank Smith, GLOBALFOUNDRIES

3:10

3.5 Novel Methods for SPC defect monitoring: Renormalizable Diversity Sampling
Ian Tolle, Hoang Nguyen, GLOBALFOUNDRIES; Ankit Jain, Martin Plihal, Sumanth Kini, KLA-Tencor

3:35 Networking Break (sponsored by Edwards)

**Session 4 – Session 4 – Factory Optimization I**

**Chairs:** Dave Gross; Stefan Radloff, Intel Corporation

The challenges of current and future semiconductor process technologies require a higher level of equipment reliability and productivity while improving energy efficiency. Optimizing scenarios and embarking on new approaches for addressing known problems will help improve fab metrics, minimize wafer costs and maximize competitiveness. Presentations in this session will introduce novel ideas for fab and equipment performance improvements and simulation.

1:30

4.1 Empowering Existing Automated Material Handling Systems to Rising Requirements
Christian Hammel, Robert Schmaler, Thorsten Schmidt, Technische Universität Dresden; Jörg Lübke, Matthias Schöps, Ulrich Horn, GLOBALFOUNDRIES; Marcin Mosinski, AMM- Solutions

1:55

4.2 Dispatching rules considering transport related restrictions during failure scenarios - A use case
Robert Schmaler, Christian Hammel, Thorsten Schmidt, Technische Universität Dresden; Matthias Schoeps, GLOBALFOUNDRIES

2:20

4.3 Modelling the Variance of the Durations of Maintenance Activities in Semiconductor Fabs
Itai Regev, Intel - Fab 28; Diamanta Benson-Karhi, The Open University of Israel; Yisrael Parmet, Ben-Gurion University

2:45

4.4 Management of Crisis Situations in a Large Unified AMHS of a Semiconductor Manufacturing Facility
Moulaye Aidara Ndiaye, Stéphane Dauzère-Pérès, Claude Yugma, Ecole des Mines de Saint-Etienne; Lionel Rullière, Gilles Lamiable, STMicroelectronics (STUDENT)

3:10

4.5 AMHS design for mask transport in Photolithography area of an existing wafer fab
Ali Ben Salem, Claude Yugma, Ecole des Mines de Saint-Etienne; Emmanuel Tronchet, Jacques Pinaton, STMicroelectronics (STUDENT)

3:35 Networking Break (sponsored by Edwards)

**Tutorial: Nanoscale III-V CMOS**

Professor Jesús A. del Alamo, Director, Microsystems Technology Laboratories, Massachusetts Institute of Technology

Transistors based on III-V compound semiconductors have emerged as a credible alternative to Si for future nanometer-scale CMOS. This talk will review recent progress as well as challenges confronting III-V electronics in the quest to extend Moore’s Law beyond the reach of Si.
The 27th Annual SEMI Advanced Semiconductor Manufacturing Conference - ASMC 2016

Wednesday, May 18, 2016 (Day Two)

7:30-8:00  Registration (City Center Lobby)
8:00-9:00  Keynote: The Economy of Things: How Cognitive IoT Is Driving New Business Models
          Don O'Toole, Business Development Executive, IBM Watson IoT Alliances & Ecosystem Business Development, IBM Corporation

9:00  Networking Break (sponsored by Edwards)

Session 6 - Defect Inspection II
Chairs: Israel Ne’eman, Applied Materials; Larry Pulvirent, GLOBALFOUNDRIES
Defect inspection is integral to the development and manufacturing of semiconductor devices. This session will feature papers describing new case studies on utilizing e-beam based technology for in-line defect detection and wafer characterization, tool-to-tool matching and end-of-line Defect Detection.

9:20  6.1 In-line Characterization of EDRAM for a FINFET technology using VC inspection
     Oliver D. Patterson, Richard Hafer, Surbhi Mittal, GLOBALFOUNDRIES; Xiaohu Tang, Brian Lei, Shuen-Chen Chris Lei, Hermes Microvision, Inc.

9:45  6.2 A Case Study on Inline Defect Diagnosis by Applying E-beam Inspection System
     Hao-Yu Chien, Chan-Hao Hsu, Yue-Ying Yen, Tzung-Hua Ying, Powerchip Technology Co.

10:10  6.3 E-beam Tool-to-Tool Matching Methodology
       Xing J. Zhou, Samsung Austin Semiconductor; Ho Young (Derek) Kim, Hermes Microvion, Inc.

10:35  6.4 Detection of Gate to S/D Shorts by Charge Dynamics Effect
       Ming Lei, Kevin Wu, GLOBALFOUNDRIES; Qing Tian, Yan Zhao, Hermes Microvision, Inc.

11:00  6.5 Optical Beam Induced Current for Monitoring of Defective SRAM Junctions
       Greg M. Johnson, Christopher D’Aleo, GLOBALFOUNDRIES

11:30  Boxed Lunch

Session 7 - Advanced Equipment and Materials Processes (sponsored by Air Liquide)
Chairs: Russell Dover, KLA-Tencor; Brett Williams, ON Semiconductor
Advanced memory, analog, and logic manufacturers face daunting challenges as the next generation device nodes come on line. These challenges are being met by the development and applications of innovation in equipment, materials, and processes. This session will focus on and will highlight some of the latest innovations that are being implemented in leading edge high volume manufacturing

9:20  7.1 Improved 20nm Device Yield and Gate Dielectric Integrity with Optimized Aluminum Metal Fill Process
     David James Williams, Clint Bordelon, Sergei Drizlikh, Paul D. Kirsch, Kin-Sang Lam, Paul Copala, Ian Guerassio, Nikhil Bharat Hira, Steven Trigno, Paul Nester, Ryan Paulsen, Anuj Patel, Samsung Austin Semiconductor; Jun-Han Kim, Jungmin Park, Taegyun Kim, Hee Sung Kang, Jinho Seo, Chulwan An, Sungjong Wang, Samsung Electronics

9:45  7.2 Investigation on critical thickness dependence of ALD TiN diffusion barrier in MOL Archana Subramaniyan, Domingo Ferre Luppi, Neal Makela, Lawrence Bauer, Jr., Anita Madan, Richard Murphy, Frieder Baumann, Kriti, Kohli, GLOBALFOUNDRIES

10:10  7.3 Metal Wiring Critical Dimension Shrink Using ALD Spacer in BEOL Sub-50nm Pitch Ketan Shah, Prakash Periasamy, Ashwini Chandrasekhar, Anbu Selvam KM Mahalingam, Shyam Pal, Christopher Ordonio, Peter Welti, Chun Hui Low, Craig Child, GLOBALFOUNDRIES

10:35  7.4 Interface Preservation During Ge-Rich Source/Drain Contact Formation
       Chengyu Niu, M. Raymond, V. Kamineni, J. Fronheiser, S. Siddiqui, H. Niimi, A. Labonte, GLOBALFOUNDRIES; P. Adusumilli, A.V. Carr, J. Shearer, J. M. Dechene, IBM Research

11:00  7.5 Moore's Law Continues into the 1x-nm Era
       Dick James, Chipworks Inc.

2016 Corporate Sponsors:
Session 8 – Yield Enhancement/Yield Learning
Chairs: Ishtiaq Ahsan, GLOBALFOUNDRIES; Gary Green, AVOTech; Sagar Kekare, KLA-Tencor
Characterization techniques for driving yield are critical for successful semiconductor manufacturing. This session covers reductions in “dark gate” in metal CMOS processes, preventing gate oxide plasma damage using surface photovoltaic measurements, a novel Al deposition process to minimize power short failures caused by Al whiskers, yield improvements in the nitride stress liner, and an investigation into the transient leakage of point-defects in gate oxides due to phosphorus contaminants.

12:25
8.1 Reduction of “Dark-Gate” defects in Replacement-Metal-Gate process and Middle-of-line contacts for advanced CMOS technology
Wen Pin Peng, Min-Hwa Chi, GLOBALFOUNDRIES, Inc.

12:50
8.2 (3641) Detecting and Preventing Gate Oxide Plasma Damage During PECVD Carbon Deposition Through Surface Photovoltage Measurements
Alan K. Fritz, Leonard J. Olmer, Micron Technology

1:15
8.3 Optimized circuit design and novel Al deposition process cure power short failure caused by Al whisker
Yuwei Ma, Chien Hsin Lai, Zhi Min Zhang, Wei Liang Huang, Chao Yong Li, Cong Shu Zhou, Chee Kong Leong, GLOBALFOUNDRIES Singapore Pte Ltd

1:40
8.4 Yield Improvement by Improving Bottom Profile Footing at Nitride Stress Liner
Niti Garg, Philippe Helal, Pranesh Muralidhar, Vincent Sih, Stephanie Waite, Silas Scott, GLOBALFOUNDRIES

2:05
8.5 On the Transient Leakage of Point-Defects in Gate Oxide due to Spatially Transported Constant-Source of Phosphorus Contaminants
Liyi Sheng, Brett Williams, T. Haskett, E. Glines, ON Semiconductor

2:30 Networking Break (sponsored by Edwards)

Session 9 - Advanced Equipment / CFM
Chairs: Anand Subramani, KLA-Tencor; David Tucker, Texas Instruments
Advanced memory, analog and logic manufacturers face daunting challenges as the next generation device nodes come on line. These challenges are being met by the development and applications of innovations in equipment, materials, and processes. In this session, we focus on advanced manufacturing concepts ranging from TaN barrier defect reduction to interesting pattern dependent charging effects. We also cover critical aspects and improvements in both front end and back end cleans.

12:25
9.1 Extra-pattern Killer Defectivity Improvement and Enhancement of within-feature Barrier coverage by Optimization of TaN Barrier PVD process in 90p Cu wire interconnects for 28nm Technology
Balajee Rajagopalan, Jean-Baptiste Laloe, San Leong Liew, Mary Clarie Silvestre, Esvar Ramanathan, Sohanan Khanal, Anbu Selvam Mahalingam, Robert Teagle, GLOBALFOUNDRIES; Alain Laval, Qian Ge, Nobuyuki Takahashi, Applied Materials

12:50
9.2 Pattern Dependent Plasma Charging Effect in High Aspect Ratio 3D NAND Architecture
Zusing Yang, Yao-An Chung, Sheng Yuan Chang, Hong-Ji Lee, Nan-Tzu Lian, Tahone Yang, Kuang-Chao Chen, Chih Yuan Li, Macronix International Co., Ltd.

1:15
9.3 Precleans challenges on middle-of-the-line contacts for 14nm technologies and beyond
Domingo Ferrer, Annie Lévesque, Asli Sirman Junedong Lee, Archana Subramaniyan, Lou Lanzerotti, David F. Hilscher, GLOBALFOUNDRIES; Emre Alpetkin, IBM SRDC

1:40
9.4 Optimization of Wet Clean and its Impact on sub-50 nm Pitch BEOL Yield AKM
AKM Sajjadul Islam, Prakash Periasamy, Ashwini Chandrasekhar, Anbu Selvam KM Mahalingam, Christian Witt, Craig Child, GLOBALFOUNDRIES

2:05
9.5 Optimizing Wet Clean Operations in an Established Manufacturing Environment
Raymond Van Roijen, David Hilscher, Colleen Meagher, Ryan Rettman, Derek McKindles, GLOBALFOUNDRIES

2:30 Networking Break (sponsored by Edwards)
Session 10 – Advanced Patterning (Sponsored by ASML)

Chairs: Erin Lavigne, GLOBALFOUNDRIES; Jacek Tyminski, Nikon Research

Advanced patterning is a key element of leading-edge semiconductor fabrication. This session contains presentations exploring a range of imaging and design for manufacturing (DFM) techniques employed in IC production. The session highlights virtual metrology, imaging optimization, and the status of 450 mm lithography.

2:50
10.1 Novel Hybrid 3D NAND Flash Memory Containing Vertical-Gate and Gate-All-Around Structures
Yao-An Chung, Zusing Yang, Yuan-Chieh Chiu, Shih-Ping Hong, Hon-Ji Lee, Tan Tzu Lian, Tahone Yang, Kuang-Chao Chen, Chih-Yuan Lu, Macronix International Co., Ltd.

3:15
10.2 Logic Characterization Vehicle Design for Yield Learning
Benjamin Taylor Niewenhuis, Zeye (Dexter) Liu, Soumya Mittal, R.D. (Shawn) Blanton, Carnegie Mellon University

3:40
10.3 Process Window Doubling by Optimized SRAF Placement Rules
Luozhou Li, Lianghong Yin, Shaowen Gao, Changan Wang, William Willkonson, Jason Cantone, GLOBALFOUNDRIES

4:05
10.4 Immersion Lithography Scanner Readiness for Volume Manufacturing on 450mm Substrates
Jasper Paul Munson, Nikon Precision; Christopher R. Carr, Global 450mm Consortium

4:45-6:00  Panel Discussion
"Moore’s Law Wall vs. Moore’s Wallet, and Where Do We Grow From Here?"
Moderator: Paul Werbaneth, Intevac
Panelists: David Bloss, VP, Intel Corporation; Mike Campbell, VP of Engineering, Qualcomm; Patrick Martin, Head of Field Technology, Applied Materials; Gary Patton, Chief Technology Officer, GLOBALFOUNDRIES (invited); Samsung (invited)

6:30-7:45  Saratoga Reception – Canfield Casino (sponsored by Applied Materials, Saratoga EDC, Saratoga Convention & Tourism Bureau)

Session 11 – Advanced Process Control (APC)

Chairs: Chairs: Agnes Roussy, EMSE; Raymond van Roijen, GLOBALFOUNDRIES

APC Definition: Advanced Process Control applies virtual metrology, run-to-run control, and big data applications to improve yield and tool availability.

2.50
11.1 Maintenance of Virtual Metrology Models
Jimmy Iskandar, James Moyne, Applied Materials

3:15
11.2 A Multi-step Wafer-level Run-to-Run Controller with Sampled Measurements for Furnace Deposition and CMP Process Flows
Yulei Sun, Joerg Reichelt, Rudolph Technologies; Tilo Bormann, Andreas Gondorf, Vishay Intertechnology

3:40
11.3 Optical Emission Spectrum Processing Using Discrete-Wavelet Transform Compression
Taikang Ning, Trinity College; CH Huang, J. Jensen, V. Wong, H. Chan, Lam Research

4:05
11.4 Virtual metrology based on relevant features extraction and Just-In-Time Learning approach
Mohamed Ali Jebri, Guillaume Graton, El Mostafa El Adel, Mustapha Ouladsine, LSIS-UMR; Jacques Pinaton, STMicroelectronics (STUDENT)
8:00 Session 12 – Advanced Metrology I (sponsored by ASML)
Chair: Delphine Le Cunff, STMicroelectronics; Franz Heider, Infineon Technologies
Novel processes, complex materials, shrinking process margins are putting significant pressure on measurement tool-sets. As time available to develop upcoming process node/architectures decreases, there is a drive for ever more sophisticated in-line metrology control for fast cycles of learning and process control. This session will cover several key advancements in the field of patterning metrology and characterization.

8:30 12.1 An integrated approach to Holistic Metrology Qualification for Multi-Patterning Process layers
Emil Schmitt-Weaver, Lotte Willems, Peter Wardnier, Omer Adam, Grzegorz Grzela, Joost van Heijst, Henry Megens, Kaustave Bhattacharyya, ASML Netherlands B.V.

8:55 12.2 Etch process monitoring possibilities and root cause analysis

9:20 12.3 Reducing Metrology Mean-Time-To-Detect by Utilizing Product Data
Douglas Crauder, Eric Solecky, GLOBALFOUNDRIES

9:45 Networking Break

Session 13 – Factory Optimization
Chair: Thomas Beeg, GLOBALFOUNDRIES; Eric Eisenbraun, SUNY Polytechnic Institute
The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity while improving energy efficiency. Optimizing scenarios and embarking on new approaches for addressing known problems will help improve fab metrics, minimize wafer costs and maximize competitiveness. Presentations in this session will introduce novel strategies to increase the understanding and exploitation of the role played by the process chamber in factory optimization.

8:30 13.1 A Novel Technique for Epitaxy Tool-to-Tool and Chamber Matching anSamsud Optimization
Richard G. Cosway, Steven R. Burch, Andrew D. Rosser, Phillip T. Lazok, ASM America

8:55 13.2 Throughput Evaluation Model for the Linear Platform in Semiconductor manufacturing
Kai-Ting Yang, Elvis Hauang, Leo Ke, Tina Shen, Taiwan Semiconductor Manufacturing Company (tsmc)

9:20 13.3 Wait-Time-Waste improvement opportunities and ‘smart manufacturing’ in legacy 200mm fabs
Jan Driessen, Rene Sjardijn, Frank van Heukelom, Corstian van Roest, Martijn Mom, NXP Semiconductors

9:45 Networking Break

Session 14 – Yield Enhancement
Chair: Pratik Joshi, Samsung Austin; Dieter Rathei, DR Yield; Brett Schroeder, Applied Materials
Characterization techniques for driving yield are critical for successful semiconductor manufacturing. This session proposes a novel first-metal trench post-lithography rework process for improved yield, an exploration of the correlation between inline electrical yield versus optical inspection at the 14nm node, and methodology for more accurate 3-D capacitance modeling and process variation characterization to enable Moore’s Law below 10nm.

10:05 14.1 Trench First Metal Hardmask Post-Lithography Novel Rework Process for Defectivity and Yield Improvement
Mary Claire Silvestre, Mukesh Gogna, Selvam, KM Mahalingam, Eswar Ramanathan, Christopher Ordonio, GLOBALFOUNDRIES; John Schaller, Applied Materials

10:30 14.2 Inline Electrical Yield versus Optical Inspection: Correlations, Connections and Disconnections
Fan Zheng, Dave Salvador, Cathy Gow, Lori Kermal, Bryan Rhoads, Kan Zhang, Xiao Pan, Ben Stahl, William Davies, Amanda Tessier, Edward Crawford, Rebekah Sheraw, Ishthiaq Ahsan, Brett Engel, GLOBALFOUNDRIES; Brad Austin, Yongchun Xin, Jan Sim, IBM Corporation

10:05 14.1 Process Development and Optimization for High-Aspect Ratio Through-Silicon Via (TSV) Etch

10:30 14.2 Non-Conductive Film Underfill for 3D Integration of 30 μm-Thick LSI Wafers with Fine Cu-TSVs
Murugesan Mariappan, J.C. Bea, K.W. Lee, M. Koyanagi, Y. Ito, T. Fukushima, T. Tanaka, Tohoku University

10:55 14.3 Advanced Detection Method for Polymer Residue on Semiconductor Substrates
Helene Richter, Markus Pfeffer, Anton Bauer, Fraunhofer Institute for Integrated Systems and Device Technology; J. Siegert, T. Bodner, M. Schrems, ams AG
Polymer Surface Treatment to Reduce RDL Leakage and Solve Delamination Issue
W.L. Huang, J.J. Wong, Danial Huang, K.P. Chang, Harry Ki, H.S. Su, TSMC

(Snack Packs sponsored by Avantor Electronic Materials)

11:25 Keynote: Is China Driving the Urge to Merge?
Robert Maire, President, Semiconductor Advisors

12:15 Closing Remarks