The 26th Annual SEMI Advanced Semiconductor Manufacturing Conference – ASMC 2015 May 3-6, 2015 – Saratoga Hilton/City Center (Saratoga Springs, NY) 1-May-15 (***subject to change***)

Sunday, May 3, 2015

6:30-7:30 pm Welcome Reception and Registration (***sponsored by FEI***) **(Hilton Hotel Lobby)**

Monday, May 4, 2015

7:30-8:30am Registration / Networking Breakfast (***sponsored by Nikon Precision***) **(City Center Lobby)**

8:30 Welcome to the Conference (Dr. Matthew Wagner/Pall Corporation and Brett Williams/ON Semiconductor) and 2014 Best Paper Awards (**Room M1)**

8:45 Keynote: **Balancing Eco-System Value Creation and Value Capture** - Thomas Caulfield, Ph.D., Sr. Vice President and General Manager, GLOBALFOUNDRIES (Fab 8)

Session 1 Defect Inspection I **(Room M2B)**

Chairs: Jeff Barnum, KLA-Tencor; Byoung-Ho Lee, Ultratech Stepper; Larry Pulvirent, GLOBALFOUNDRIES

Defect inspection in our industry is critically important to process optimization and yield improvement. This session will focus on defect reduction in the BEOL Cu CMP processes for both physical and non-visual defects, a unique method to quantify Ge and SiGe growth, defect source isolation in 20nm gate module, and defect challenges associated with triple patterning in the 14nm node.

9:50

1.1 Nanoparticle Reduction in Cu CMP for <20nm Nodes

Damien Jeanjean, O. Robin, R. Sramek, S. Mermoz, S. Gaillard, STMicroelectronics; Y. Chen, F. Pitard, L. Nicoud, B. Brown, Applied Materials

10:15

1.2 Correlation of Non-Visual Defects at Post Copper CMP to Yield Critical Physical Defects at Next Metallization Layer

Marc Specht, H. Franke, O. Luxonhofer, K. Mai, Infineon Technologies Dresden GmbH, W. Usry, R. Newcomb, Qcept Technologies

10:40 Networking Break (***sponsored by Edwards***)

11:00

1.3 Using the low frequency component of the background signal for SiGe and Ge growth monitoring

Sandip Halder, Andreas Schulze, Philippe Leray, Matty Caymax, imec; Gerhard Bast, Gavin Simpson, Neli Ulea, Marco Polli, KLA-Tencor

11:25

1.4 Defect Reduction for 20nm High-k Metal Gate Technology

Vincent Charbois, Julie Lebreton, Mylène Savoye, Eric Labonne, Antoine Labourier, Benjamin Dumont, STMicroelectronics; Chet Lennox, Mike von Den Hoff, KLA-Tencor

11:50

1.5 Inspection Challenges for Triple Patterning at Sub-14 nm nodes with Broadband Plasma Inspection Platforms

Sandip Halder, Vincent Truffert, Dieter van den Heuvel, Philippe Leray, Shaunee Cheng, Greg McIntrye, imec; Kaushik Sah, Jim Brown, Paolo Parisi, Marco Polli, KLA-Tencor

12:15 Networking Lunch (City Center M1)

Session 2 Factory Optimization I **(Room M2A)**

Chairs: Alan Brightman, Edwards; Holly Magoon, Nikon; Jan Rothe, GLOBALFOUNDIRES

Semiconductor equipment and manufacturing is increasingly complex and driven by strict economic constraints, making it essential for IC makers to maximize fab productivity and efficiency. This session discusses management of several semiconductor manufacturing constraints and as well as optimization of fab parameters and scenarios towards lean manufacturing.

9:50

2.1 Managing the Economic Constraints of Foundries and Fabless Enterprises

Charles M. Weber, Jiting Yang Portland State University **(STUDENT)**

10:15

2.2 Inspection Control in semiconductor Manufacturing with Time Constraints

Rezvan Sadeghi, Stéphane Dauzère-Pérès, Claude Yugma, EMSE-CMP; Guillaume Lepellietier, STMicroelectronics **(STUDENT**)

10:40 Networking Break (***sponsored by Edwards***)

11:00

2.3 Shortening of cycle time in semiconductor manufacturing via meaningful lot sizes by identifying Detailed Time Based Leverages and Machine Characteristics

Sophia Keil, Rainer Lasch, Frederik Peipp, Dresden University of Technology; Dietrich Eberts, Infineon Technologies Dresden GmbH

11:25

2.4 Use of Simulation Studies to Overcome Challenges for Fab Automation of a 300 mm Power Semiconductor Pilot Line Including Thin-Wafer Processing

Germar Schneider, Infineon Dresden Technologies GmbH; Thomas Wagner, Technische Universität Dresden; Martin Kraft, CTR Carinthian Tech Research AG

11:50

2.5 Bridging the Gap – Integrating APC Constraints and WIP Flow Optimization to Enhance Automated Decision Making in Semiconductor Manufacturing

Marcel Stehli, Daniel Zschäbitz, and Thomas Jähnig, GLOBALFOUNDRIES

12:15 Networking Lunch

Session 3 – Yield Enhancement/Methodology I **(Room M2B)**
Chairs: Jeanne Bickford, IBM; Sagar Kekare, KLA-Tencor; Raymond Van Roijen, IBM
Nanometer nodes technologies are bringing about significant new yield loss mechanisms, both in random and systematic categories. This session will review leading edge efforts to capture, manage, and reduce these yield loss avenues through process or device optimization.

1:45
3.1 Collapse-Free Patterning of High Aspect Ratio Silicon Structures for 20 nm NAND Flash Technology
Vikram V. Iyengar, Suresh Chandrasekaran, Darryl Weddington, Monte M. Nettles, Oliver H. Eagle, Shih Hwee Tey and Thad B. Parry, IM Flash Technologies

2:10
3.2 Standby Leakage Current Reduction in a 180nm EEPROM Process Technology
Santosh Menon, Moshe Agam, ON Semiconductor

2:35
3.3 A Case Study On Severe Yield Loss Caused by Wafer Arcing in BEOL Manufacturing
Hong-Ji Lee, Hsu-Sheng Yu, Shih-Chin Lee, Chih-Kai Yang, Shao-En Chang , Kuo-Feng Lo, Xin-Guan Lin, Nan-Tzu Lian, Tahone Yang and Kuang-Chao Chen, Macronix International Co., Ltd

3:00
3.4 Effect Of Top Corner Rounding in BEOL To Yield In Advanced Technologies
Eswar Ramanathan, Mary Claire Silvestre, KM Mahalingam, Anbu Selvam, Niti Garg, Siddhartha Siddhartha, Christopher Ordonio, John Schaller, GLOBALFOUNDRIES

3:25 Networking Break (***sponsored by Edwards***)

Session 4 – Advanced Metrology I (***sponsored by FEI***) **(Room M2A)**
Chairs: Amiad Conley, Applied Materials; Franz Heider, Infineon; Erin Lavigne, IBM
Novel processes and complex materials are putting significant pressure on measurement tool-sets. As the time to develop upcoming process nodes and new semiconductor architectures decreases there is a drive for ever more in-line Critical Dimension and films metrology control for fast cycles of learning and process control. This session will cover several key advancements in integrated metrology module control and advances TSV films metrology and control.

1:45
4.1 Integrated Metrology's Role in Gas Cluster Ion Beam Etch
Taher Kagalwala, Ravi Dasaka, Michael Aquilino, Laertis Economikos, IBM Microelectronics; Aron Cepler, Charles Kang, Naren Yellai, Nova Measuring Instruments Inc.

2:10
4.2 Methodology to Estimate TSV Film Thicknesses Using a Novel Inline "Adaptive Pattern Registration" Method
Shravanthi L Manikonda, Dingyou Zhang, Rudy R. Giridharan, Abner Bello, GLOBALFOUNDRIES Inc.; Jun Song, RUDOLPH Technologies

2:35
4.3 Optical step height and trench depth measurement
Franz Heider, Georg Janisch, Michael Kern, Kurt Weinzierl, Infineon Technologies; Matthias Meyer, Bastian Tröger, FRT Fries Research & Technology GmbH

3:00
4.4 Through Silicon Via Process Characterization by Integrated Inspection/Metrology Solutions in Visible and Infrared Domain
Nicolas Devanciard, Stephane Rey, Thomas Magis, Stephane Minoret, Carlos Beitia, CEA, LETI; Dario Alliata, David Marx, Prasad Bachiraju, Darcy Hart, John Thornell, Russ Dudley, Rudolph Technologies, Inc.

3:25 Networking Break (***sponsored by Edwards***)

3:50-5:00 Tutorial: **The Science, Technology and Art of Graphene** **(Room M2B)**
Prof. Paul L. McEuen, John A. Newman Professor of Physical Science, Director, LAASP, Kavli Institute of Cornell for Nanoscale Science, Department of Physics, Cornell University

Monday, May 4, 2015 - 5:00-6:30 Session 5 - Poster Session **(sponsored by KLA-Tencor; Marcy NanoCenter/NY Loves NanoTech)** (**Room M1)**

Chairs: Jennifer Braggin, Interplex Industries; Thanas Budri, Texas Instruments; Philippe Campion, STMicroelectronics; Eric Eisenbraun, SUNY CNSE; Mutaz Haddadin, Intel; Larry Hennessy, CH2M Hill; Weimin Li, Entegris; Sophia Keil, Dresden University of Technology; Hamid Khorram, Nikon; George Kong, Peregrine Semiconductor; Delphine Le Cunff, STMicroelectronics; Daniel Maynard, IBM; Kazunori Nemoto, Hitachi High-Tech; Rob Pearson, Rochester Institute of Technology; Anand Subramani, KLA-Tencor; Patrick Varekamp, IBM; Naomi Yoshida, Applied Materials

450mm SEMI Physical Interface Standards: Architecture and Efficiency
Mutaz Haddadin, Stefan Radloff, Intel Corporation

Advanced Contamination Control Methods for Yield Enhancement
Helene Richter, A. Liebold, R. Altmann, B. Doffek, J. Koebl, M. Pfeffer, A. Bauer, Fraunhofer Institite IISB; G. Schneider, Infineon Dresden GmbH; D. Cheung, Entegris ECP

Application of a 3-Step Kaizen Strategy for Improvement of WIP Flow in a Semiconductor Fab
Samantha Comulada, Justin Mendola, IBM Semiconductor R&D Center

Automatic Metrology Algorithm Identification Using Pattern Matching
Daniel S. Fischer, Khaled Akid, Erin C. Lavigne, IBM R&D Center; Islam S. Abed, Dina Abdelhaliem, Juli Optiz, Nick Dragiewicz, Chris McGinty, Joe Britton, Mentor Graphics

Big Data Emergence in Semiconductor Manufacturing Advanced Process Control
James Moyne, Jamini Samantaray, Mike Armacost, Applied Materials

Blowback Filtration for CVD Vacuum Pump Protection
Jochen Ruth, Matthew L. Wagner, Gerd Heser, Pall Microelectronics

Challenges in Integrating Embedded Non Volatile with Floating Poly and ONO in Base Line Process
Moshe Agam, Santosh Menon, Peter Cosmin, Thierry Yao, Peter McGrath, Bladimiro Ruiz, Brian Baylis, Eric Ameele, Kirk Rolofson, Roger Young, ON Semiconductor

Device Specific Characterization of Yield Limiting Pattern Geometries by Combining Layout Profiling with High Sensitivity Wafer Inspection
Jean-Christophe Le Denmat, Laurent Tetar, Pierre Fanton, Emek Yesilada, Pierre-Jérôme Goirand, ST Microelectronics; Narayani Narasimhan, Paolo Parisi, Vijay Ramachandran, Sagar A. Kekare, KLA-Tencor

Effect of Defectivity Reduction in Spacer and Junction Modules on RMG Defectivity
Akshey Sehgal, Sridhar Kuchibhatla, Bharat Krishnan, Dhiman Bhattacharyya, Jing Wan, Hsiao-Chi Peng, Shi You, GLOBALFOUNDRIES, Inc.

Effective wet clean method to eliminate unwanted growth SiGe defect in FinFET
Jian Li, Jagdish Prasad, Zhiguo Sun, Byoung-Gi Min, GLOBALFOUNDRIES

Emerging Atomic Layer Deposition (ALD) Processes for Low Thermal Budget Flexible Electronics
Dillon Gregory, Paul Hansen, George Marshall, Eric Eisenbraun, SUNY Polytechnic CNSE (**STUDENT**)

Energy Conservation Mode Signaling Standardization
Mike Czerniak, Edwards Ltd.; Gino Cripieri, consultant

High Aspect Ratio Etch Yield Improvement by A Novel Polymer Dump Thickness Metrology
Jeff J. Ye, Ganga R. Ega, Shaun P. Thompson, Micron Technology Inc.

Impact of Molybdenum Contamination on Stacking Faults in Epitaxial Silicon
Michael J. McCormick, Paul Porath, ON Semiconductor

Improved Ion Implant Exhaust Management for Reduced Energy and Capital Costs
Joseph Sweeney, Karl Olendar, Entegris, Inc.; Steve Ballance, Texas Instruments

Inspection step modelling for defect source tool identification using in-line defectivity control
Mohamad Chakaroun, Rabah Messouci, Mohand Djeziri, Mustapha Ouladsine, LSIS Laboratory; Jacques Pinaton, STMicroelectronics (**STUDENT**)

Local Wafer Temperature Non-Uniformity Correction with Laser Irradiation
Preetham Rao, Applied Materials, Inc.

Managing Fab UHP N_2 By Measuring Trace Moisture
Douglas Barth, Matthew L. Wagner, Pall Microelectronics; Marion Bolkenius, Jean-Luc Cloarec, Air Liquide

Modeling and Dispatching Refinement for Implantation to Reduce the Probability of Tuning Beam
Kai-Ting Yang, Leo Ke, Tina Sheen, Taiwan Semiconductor Manufacturing Company

Optical properties determination of Fully Depleted Silicon On Insulator (FDSOI) substrates by ellipsometry
Loïc Schneider, F. Abbate, D. Le Cunff, STMicroelectronics; A. Michallet, E. Nolot, CEA LETI **(STUDENT)**

Post TSV Etch Cleaning Process Development using SAPS Megasonic Technology
Fuping Chen, Xiaoyan Zhang, Xi Wang, Xuecheng Tao, Shu Yang, David H. Wangline, ACM Research, Inc.; Victor Vartanian, Brian Sapp, SEMATECH

Productivity Challenges in PVD Processing in 300mm Pilot Lines for Power Semiconductors
Amit Rastogi, N. Morin, C. Jones, S. Burgess, R. Trowell, C. Widdicks, I. Moncrieff , SPTS Technologies; M. Ehmann, S. Schmidbauer, Infineon Technologies

Quick Process Troubleshooting by Using Advanced SEM ADC system
Cheng Yi Hsieh, C.C. Yang, S.C. Gao, Taiwan Semiconductor Manufacturing Company; Travis Chang, Wallas Chen, Henry Chen, Alex Cheng, KLA Tencor

Rapid Non-Destructive Detection of Sub-Surface Cu in Silicon-On-Insulator Wafers by Optical Second Harmonic Generation M.L. Alles, D.M. Fleetwood, R.D. Schrimpf, N.H. Told, Vanderbilt University; Victor Koldyaev, M Kyrger, J. Changala, Femtometrix

Real-Time Information Base as key enabler for Manufacturing Intelligence - "Industrie 4.0" Building the bridge between "real" Real-time Exploitation and Big Data via mathematically grounded Information Fundamentals
Gerhard Luhn, Johannes Postel, Travis Stevens, Martin Zinner, Systema Gmbh; Dirk Habich, Technical University Dresden; Katrin Bartl, X-FAB

Spatial risk assessment on circular domains Application to wafer profile monitoring
Esperan Padonou, Hugues Duverneuil, STMicroelectronics; Olivier Roustant, Jakey Blue, Mines Saint-Etienne; (**STUDENT)**

Trace Analysis of Hydrogen Peroxide Contamination
Megan E. Lydon, Joseph K. Comeau, Jason P. Ritter, IBM Systems and Technology

Track Process Monitoring Via Laser Scattering Imaging
Luciana Meli, Ranee Kwong, Cody J. Murray, Karen E. Petrillo, Alex R. Hubbard, Parul Dhagat, IBM; Shawn MacNish, Chandar Palamadai, KLA-Tencor

Using a visible BI to construct Lean Manufacturing within big data
S.H. Chiu, Hung Kai Lin, Jung Pin Hsu, Che Yu Chiu, Taiwan Semiconductor Manufacturing Corporation

Yield Improvement in dense EEPROM by Bit Mapping and Experimental Design
Moshe Agam, Santosh Menon, Peter Cosmin, ON Semiconductor

The 26th Annual SEMI Advanced Semiconductor Manufacturing Conference - ASMC 2015

Tuesday, May 5, 2015 (Day Two)

7:30-8:00 Registration **(City Center Lobby)**

8:00-9:00 Keynote: A Dynamic View of Nanostructure Growth - Frances M. Ross, Ph.D., Research Staff Member, Nanoscale Materials Analysis Dept., IBM T.J. Watson Research Center **(Room M1)**

Session 6 - Defect Inspection II **(Room M2B)**

Chairs: Pinyen Lin, G450C/TSMC; Israel Ne'eman, Applied Materials

Defect inspection is integral to the development and manufacturing of semiconductor devices. This session will feature papers describing new ways to utilize e-beam technology for defect detection and process monitoring.

9:05

6.1 The Merits of High Landing Energy for E-beam Inspection

Oliver D. Patterson, Richard Hafer, IBM Semiconductor R&D Center; Xiaohu Tang, Shuen-Cheng Chris Lei, Hermes MicroVision

9:30

6.2 Application of Backscattered Electron Imaging for Process Development in Advanced Technology Nodes

Ming Lei, Kevin Wu, Hoang Nguyen and Mingchu King, GLOBALFOUNDRIES; Hong Xiao, Dmitry Spivak, Jim Brown, Olivier Moreau, Paul MacDonald, KLA-Tencor Corp.

9:55 Networking Break (***sponsored by Edwards***)

10:15

6.3 Novel Method for Detecting Bitline Contact Misalignment Using Quantitative Analysis of High-Aspect Ratio SEM Images

Hong Kia Ang, Kok Hui Lim, Qin Deng, Kian Boon Tan, Wi Hoong Lim, Jessica Zhang, Micron; Ronnie Porat, Kia Kearn Chng, Seng Kee Wee, Khor Wui Cheng, Guy Gichon, Roy Mizrahi, Applied Materials, Inc.

10:40

6.4 E-beam Inspection Throughput Acceleration Via Targeted Critical Area Inspection

Oliver D. Patterson, Rasit O Topaloglu, Richard F Hafer; Shuen-Cheng Chris Lei, Xiaohu Tang, Hermes MicroVision

11:05

6.5 Enabling Future Generation High-Speed Inspection Through a Massively Parallel E-beam Approach

Matt Malloy, Ben Bunday, Stefan Wurm, SEMATECH; Brad Thiel, CNSE at SUNY Polytechnic Institute

11:30 Boxed Lunch (Hilton Hotel – Gallery)

Session 7 - Factory Optimization II **(Room M2A)**

Chairs: Thomas Beeg, GLOBALFOUNDRIES; Stefan Radloff, Intel Corporation; Charles Weber, Portland State University

The challenges of current and future semiconductor process technologies require a higher level of equipment reliability, quality, repeatability and productivity while improving energy efficiency. Optimizing scenarios and embarking on new approaches for addressing known problems will help improve fab metrics, minimize wafer costs and maximize competitiveness. Presentations in this session will introduce novel ideas for fab and equipment performance improvements and simulation

9:05

7.1 Using fractal dimension as performance indicators for manufacturing systems

Gero Grau, Detlef Pabst, Marcel Stehli, GLOBALFOUNDRIES

9:30

7.2 An Empirical Approach to Accurate Single Wafer Wet Etch Simulation

Manish Kumar Singh, Ping-Jung Huang, Pi-Chun Yu, Jack Shih, Taiwan Semiconductor Company

9:55 Networking Break (***sponsored by Edwards***)

10:15

7.3 Segmentation of Expected Duration of Maintenance Activities in Semiconductor Fabs

Itai Regev, Intel Fab 28; Diamanta Benson-Karhi , The Open University of Israel

10:40

7.4 Semiconductor Green Fabrication Innovative and Design of Intelligent system Energy-Savings

J. S. Shyu, L. K. Zhu, Y. J. Wann, H. W. Fung, C. N. Chang, TSMC

11:05

7.5 Conceptual Product Planning

Rose Bannister, Jeanne Paulette Bickford, Haylley Johnson, IBM Systems and Technology Group

Corporate Sponsors:

Session 8 – Advanced Equipment and Materials I **(Room M2B)**

Chairs: Anand Subramani, KLA-Tencor; Raymond Van Roijen, IBM

Advanced memory, analog and logic manufacturers face daunting challenges as the next generation device nodes come on line. These challenges are being met by the development and applications of innovations in equipment, materials, and processes. This session will focus on and will highlight some of the latest innovations that are being implemented in leading edge high volume manufacturing.

12:00

8.1 Semiconductor Equipment Assessment – An Enabler for Production Ready Equipment

M. Pfeffer, L. Pfitzner, A. Bauer, Fraunhofer Institute for Integrated Systems and Device Technology (IISB)

12:25

8.2 Validation of High Efficiency ICP Source Performance for Advanced Resist Ashing

Vladimir Nagorny, Vijay Vaniapura, Vijay Surla, Mattson Technology

12:50

8.3 Selective Isotropic Wet Etching of TiN and TaN for High k Metal Gate Structure

Dhiman Bhattacharyya, Sridhar Kuchibhatla, Akshey Sehgal, Yan Ping Shen, Haiting Wang, Jagdish Prasad, GLOBALFOUNDRIES

1:15

8.4 Wafer Topology Effect on the Etching Saturation Behaviors in NF_3/NH_3 Remote Plasmas

Kuo-Feng Lo, Fang-Hao Hsu, Xin-Guan Lin, Hong-Ji Lee, Nan-Tzu Lian, Tahone Yang, Kuang-Chao Chen, Macronix International Co., Ltd.

1:40 Networking Break (***sponsored by Edwards***)

Session 9 - Advanced Metrology II (**sponsored by FEI**) **(Room M2A)**

Chairs: Janay Camp, KLA-Tencor; Alok Vaid, GLOBALFOUNDRIES

Novel processes and complex materials are putting significant pressure on measurement tool-sets. As the time to develop upcoming process nodes and new semiconductor architectures decreases there is a drive for ever more in-line Critical Dimension and films metrology control for fast cycles of learning and process control. This session will cover several key advancements in integrated metrology module control and advances TSV films metrology and control.

12:00

9.1 Predictive Data Analytics and Machine Learning Enabling Metrology and Process Control for Advanced Node IC fabrication

Narender Rana, Yunlin Zhang, Ronald Wall, Bachir Dirahoui, IBM Semiconductor R&D Center

12:25

9.2 On-product performance improvement via advanced litho-cluster control using integrated metrology and multi-layer overlay target

Kaustuve Bhattacharyya, Martijn Maassen, Emil Schmitt-Weaver, Robin Tijssen, Jackie Chen, Gin Hung, ASML; Kai-Hsiung Chen, Jimmy Hu, Chih-Ming Ke, JH Chen, CP Yeh, CJ Huang, BJ Cheng, TSMC Ltd.

12:50

9.3 High Volume Manufacturing Capabilities of Run-to-Run CPE Overlay Control

Lokesh Subramany, Woong Jae Chung, Karsten Gutjahr, GLOBALFOUNDRIES; Miguel Garcia-Medina, Christian Sparka, Lipkong Yap, Onur Demirer, Ramkumar Karur-Shanmugam, Brent Riggs, Vidya Ramanathan, John C. Robinson, KLA-Tencor

1:15

9.4 CD Metrology for EUV Lithography and Etch

Hayley Johanesen, Anne Kenslea, Mark Williamson, Matt Knowles, Laurens Kwakman, FEI; Jan van Puymbroeck, Dan Felder, Imec; Shimon Levi, Noam Nishry, Ofer Adan, Ilan Englard, Applied Materials; Shahar Gov, Oded Cohen, Igor Turovets, NOVA

1:40 Networking Break ((***sponsored by Edwards***)

Session 10 – Advanced Patterning **(Room M2B)**
Chairs: Oliver Patterson, IBM; Jacek Tyminski, Nikon Research
Advanced patterning is a key element of leading edge semiconductor fabrication. This session contains papers on the use of inspection and metrology tools to characterize and improve on patterning weaknesses. The final paper discusses lithography tool improvements to enable complex MEMS part manufacture.

1:55
10.1 In-line Inspection of DRC generated Hotspots
Amit Srivastava, Thomas Hermann, Remo Kirsch, Hoang Nguyen, GLOBALFOUNDRIES; Rajeev Kini, KLA-Tencor Inc.

2:20
10.2 Monitoring process-induced focus errors using high-resolution flatness metrology
Bradley J. Morgenfeld, Timothy A. Brunner, Karen Nummy, Derek Stoll, Nan Jing, Hong Lin, IBM Semiconductor R&D Center; Pradeep Vukkadala, Roshita Ramkhalawon Pedro Herrera, Jaydeep Sinha, KLA-Tencor

2:45
10.3 Process Induced Wafer Geometry Impact on center and edge lithography performance for sub 2X nm nodes
Stephen Tran, Erica Ng, Michael Johnson, Dave Kewley, Venky Subramony, Micron Technology; Sathish Veeraraghavan, Michael Chang, Jaydeep K. Sinha, KLA-Tencor

3:10
10.4 Printability Study of Reticle Defects on Wafer Using Reticle Defect Review on Ebeam Review Tools
ChanSeob Cho, Ron Taylor, Ashish Mungmode, GLOBALFOUNDRIES; Dongsheng Fan, Dmitry Spivak, Janay Camp, Hong Xiao, KLA-Tencor Corp.

3:35
10.5 MEMS Manufacturing Solutions: How to optimize lithography tool capability with various alignment methods.
Jumpei Fukui , Makoto Osanai, Sigeo Mizoroke, , Nikon Engineering, Co. Ltd; Hamid R. Khorram, Nikon Precision, Inc.

4:00 Networking Break (***sponsored by Edwards***)

Session 11 – Contamination Free Manufacturing (CFM) **(Room M2A)**
Chairs: Dave Gross, GLOBALFOUNDRIES; Christopher Long, IBM Research
Control of contamination on the wafer surface in process is essential to achieving critical rapid yield ramps. This session will feature papers focused on cleaning technologies and wafer handling methods to eliminate contamination and defects from wafer surfaces (top, back, edge) in order to reduce killer defects and drive yield improvement, and minimize/eliminate excursions.

1:55
11.1 Backside and Edge Clean of III-V on Si Wafers for Contamination Free Manufacturing
Alexey Vert, Tommaso Orzali, Tom Dyer, Richard J. W. Hill, PapaRao Satyavolu, Edward Barth, SEMATECH; Richard Gaylord, Shan Hu, Tokyo Electron Technology Center America; Saikumar Vivekanand, Josh Herman, Uzma Rana, Vidya Kaushik, College of Nanoscale Science and Engineering

2:20
11.2 Particle Free Handling of Substrates
Hassan Samadi, Markus Pfeffer, Roswitha Altmann, Thomas Gumprecht, Anton Bauer, Fraunhofer for Integrated Systems and Device Technology (IISB)

2:45
11.3 Optimized Salicide Clean to Reduce Post Fill Defectivity
SherJang Singh, Pranesh Muralidhar, Sabarinath Jayaseelan, Yue Hu, Silas Scott, GLOBALFOUNDRIES Inc.

3:10
11.4 Eliminating As Containing Residue that Create Killer Defects in 20nm HVM
Akshey Sehgal, Sridhar Kuchibhatla, Bharat Krishnan, Jing Wan, Hsiao-Chi Peng, Hui Zhan, Jinping Liu, GLOBALFOUNDRIES Inc.

3:35
11.5 Yield Improvement in 2x Node Technology by Introducing Backside Cleaning
Niti Garg, Balajee Rajagopalan, Silas Scott, Raita Hoech, GLOBALFOUNDRIES Inc.

4:00 Networking Break (***sponsored by Edwards***)

4:15-5:45 Panel Discussion **(Room M1)**
Semiconductor Manufacturing: Keeping the Silicon Magic Alive!
"*Any sufficiently advanced technology is indistinguishable from magic*." Arthur C. Clarke
How can industry, in concert with academia and government, keep silicon magic alive? Speakers from industry, academia and government will discuss how semiconductors have and will continue to have a critical role in the future of innovation.
Moderator: Paul Werbaneth, contributing editor, 3D InCites
Kerry Bernstein, Program Manager, DARPA; Danielle Merfeld, Ph.D., Global Technology Director, Electrical Technologies & Systems, GE Global Research; Jeffrey Marks, Ph.D., Vice President of Advanced Technology, Lam Research Corp.; Lynn Fuller, Ph.D., Professor Electrical and Microelectronic Engineering, Rochester Institute of Technology; Robert Maire, President, Semiconductor Advisors LLC

6:15-7:30 Saratoga Reception – Canfield Casino **sponsored by**

The 26th Annual SEMI Advanced Semiconductor Manufacturing Conference - ASMC 2015

Wednesday, May 6, 2015 (Day Three)

7:30-8:00 Registration **(City Center Lobby – Floor #2)**

8:00-9:00 Tutorial: Emerging Memories Technology Landscape **(Room M2B)**

Gurtej S. Sandhu, Ph.D., Senior Fellow, IEEE Fellow, Advanced Technology Development, Process R&D, Micron

Session 12 - Advanced Process Control **(Room M2A)**

Chairs: Agnés Roussy, EMSE-CMP; Patrick Varekamp, IBM

Advanced Process Control applies feedback and predictive techniques, including predictive maintenance, to improve yield and tool availability.

9:05

12.1 Predictive Maintenance in Semiconductor Manufacturing: Moving to Fab-Wide Solutions

Jimmy Iskandar, James Moyne, Kommisetti Subrahmanyam, Parris Hawkins, Mike Armacost, Applied Materials

9:30

12.2 Advanced Process Control (APC) and Real Time Dispatch (RTD) System Integration for Etch Depth Control Process in 300mm Fab

Gaurav K. Agrawal, Soon Yoong Loh, GLOBALFOUNDRIES; Abemelek B. Shebi, Final Phase Systems

9:55

12.3 A Study of Feed-forward Strategies for Overlay Control in Lithography Processes Using CGS Technology

Byoung-Ho Lee, David M. Owen, Doug Anberg, Shrinivas Shetty, Eric Bouche, Ultratech, Inc.

10:20

12.4 Critical sensitivity of Flash gate dimension spread on electriccal performances for advanced embedded memory

El Amine Agharben, A.Roussy, EMSE-CMP; M.Bocquet, IM2NP;, M.Bileci, S.Bégouin, A.Marchadier, STMicroelectronics **(STUDENT)**

10:45 Networking Break (***sponsored by Edwards***)

Session 13 – Yield and Reliability Enhancement/Methodology II **(Room M2B)**

Chairs: Ishtiaq Ahsan, IBM; Gary Green, AOVtech; Dieter Rathei, D R YIELD

Characterization techniques for driving yield are critical for successful semiconductor manufacturing. This session explores the projected yield impact of new product designs based on manufacturing history, capacitive TDDB improvements at 28nm, detecting BEOL process marginalities on vias with hammer testing and improving reliability using nitrogen purge of FOUPs.

9:05

13.1 Improving Reliability through Nitrogen Purge of Carriers

Raymond van Roijen, Aurelia Amanda, Javier Ayala, Laura Morgenfeld, Giuseppe La Rosa, IBM Microelectronics

9:30

13.2 Hammer Test to Detect BEOL Process Marginalities on Via Chains in Advanced Nodes

Anbu Selvam KM Mahalingam, Mary Claire Silvestre, Eswar Ramanathan, Christopher Ordonio, John Schaller, GLOBALFOUNDRIES,

9:55

13.3 Vertical Natural Capacitor Time Dependent Dielectric Breakdown (TDDB) Improvement in 28nm

Mary Claire Silvestre, Zhang Galor Wenyi, Anbu Selvam KM Mahalingam, Eswar Ramanathan, Christopher Ordonio, John Schaller, Lee Jong Hyup, Cristiano Capasso, Patrick Justison, GLOBALFOUNDRIES

10:20

13.4 Composite Attribute Method and Software to Interlock Semiconductor Product Design and Manufacturing Yield

Jeanne P. Bickford, Lori Rolfing, Candance Sullivan, Carlos They, Edward M. Wolf, and Joseph W. Yoder, IBM Systems and Technology Group; Paul Niekrewicz, Encore Semi

10:45 Networking Break (***sponsored by Edwards***)

Session 14 – 3D/TSV **(Room M2A)**
Chairs: James Lu, RPI; Thuy Tran-Quinn, IBM; Sathish Veeraraghavan, KLA -Tencor
This session will cover key innovations in the field of 3D/Through-silicon via technology (TSV) including TSV design, processing, and wafer bonding.

11:00
14.1 Deep Trench Capacitor in Three Dimensional Through Silicon Via Keepout Area for Electrostatic Discharge Protection
Nazmul Habib, Mujahid Muhammad, Jeanne Bickford, John Safran, Ahmed Y Ginawi, Fred J Towler, IBM Systems and Technology Group

11:25
14.2 Enhanced Etch Process for TSV and Deep Silicon Etch
Qing Xu, Alex Paterson, Jon McChesney Russell Dover, Yoko Yamaguchi, Aaron Eppler, Lam Research Corporation

11:50
14.3 Precision Wafer Bonding Process for Future Cost-Effective 3DICs
Isao Sugaya, Hajime Mitsuishi, Hidehiro Maeda, Masashi Okada, Takashi Tsuto, Hosei Nakahira, Nikon Corporation; Kazuya Okamoto, Nikon Corporation/Osaka University

12:15
14.4 Yield enhancement and mitigating the Si-chipping and cracking in ultra-thin 20µm-thick 8 and 12 inch LSI wafer
M. Murugesan, T. Fukushima, J.C. Bea, K.W. Lee, and M. Koyanagi, Tohoku University

Session 15 - Advanced Equipment and Materials II **(Room M2B)**
Chairs: Russell Dover, Lam Research; Leonard Olmer, Micron Technology
Advanced memory, analog and logic manufacturers face daunting challenges as the next generation device nodes come on line. These challenges are being met by the development and applications of innovations in equipment, materials, and processes. This session will focus on and will highlight some of the latest innovations that are being implemented in leading edge high volume manufacturing.

11:00
15.1 Remote Plasma Processing for Reduction of CuOx before Damascene Electroplating
Tighe A. Spurlin, Jonathan Reid, Lam Research Corporation

11:25
15.2 Modelling of the electrochemical etch stop with high reverse bias across pn-junctions
Robert Szwarc, Lothar Frey, University of Erlangen Nuremberg; Hans Weber, Iris Moder, Infineon Technologies Austria AG; Tobias Erlbacher, Mathias Rommel, Anton J. Bauer
Fraunhofer IISB **(STUDENT)**

11:50
15.3 300mm Wafer Level Sulfur Monolayer Doping for III-V Materials
W.-Y. Loh, R. T.P. Lee, R. Tieckelmann, T. Orzali, B. Sapp, C. Hobbs, S.S. Papa Rao
SEMATECH; K. Fuse, M. Sato, N. Fujiwara, L. Chang, H. Uchida, SCREEN Semiconductor Solutions Co.

12:15
15.4 Multiple Epitaxial Si Film Deposition by APCVD for Power Semiconductors
Matthias Künle, Johannes Baumgartl, Katrin Koren, Olaf Fiedler, Infineon Technologies

12:40 Keynote: The Semiconductor Industry at an Economic Crossroads - Robert Maire, President, Semiconductor Advisors **(Room M2B)**
1:20 Closing Remarks