Equipment and Process Technologies for 3D Structural Devices

Semicon China2015, Equipment & Material Forum, March 18th, 2015

Takashi Hayakawa
Senior Manager / SPE Marketing Department
Tokyo Electron Limited
Outline

• TEL China Introduction

• Further Scaling Scenario
  – Technology Trend
  – Tool Supplier’s Challenges & Opportunities

• Equipment & Process Technology
  – Wet Technology  (Prevent Pattern Collapse)
  – Dry Etch Technology  (SAC & Defect Reduction)

• Summary & Message
## TEL China Mainland History

<table>
<thead>
<tr>
<th>Date</th>
<th>Event Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1998Jun</td>
<td>TEL Shanghai office established</td>
</tr>
<tr>
<td>2002Apr</td>
<td>Tokyo Electron (Shanghai) Logistic Center Limited (TSL) established</td>
</tr>
<tr>
<td>2003Apr</td>
<td>Tokyo Electron (Shanghai) Limited (TES) established</td>
</tr>
<tr>
<td>2003Dec</td>
<td>TES Beijing Branch office established</td>
</tr>
<tr>
<td>2004Feb</td>
<td>TES moved into TES-owned new building located in Zhangjiang Hi-Tech Park</td>
</tr>
<tr>
<td>2006Apr</td>
<td>TES Wuxi Branch office established</td>
</tr>
<tr>
<td>2006Jul</td>
<td>TEL celebrated the 1,000th new systems installed in mainland China</td>
</tr>
<tr>
<td>2008Jun</td>
<td>TEL celebrated 10-year anniversary of establishment in China</td>
</tr>
<tr>
<td>2011Jan</td>
<td>Ground break of Tokyo Electron (Kunshan) Limited (TKS)</td>
</tr>
<tr>
<td>2011Oct</td>
<td>TEL set research fund for IMECAS and PKU R&amp;D</td>
</tr>
<tr>
<td>2012Mar</td>
<td>Opening ceremony of TKS</td>
</tr>
<tr>
<td>2012Jun</td>
<td>Start NEXX business in China (PVD/ECD)</td>
</tr>
<tr>
<td>2012Nov</td>
<td>50 years anniversary of TEL</td>
</tr>
<tr>
<td>2013Apr</td>
<td>Start FSI business in China (cleaning equipment)</td>
</tr>
<tr>
<td>2013Aug</td>
<td>TES Xi’an Branch office established</td>
</tr>
</tbody>
</table>
TEL China Mainland Operations

(As of Dec31, 2014)

Shanghai
Beijing
Wuxi
Xi’an
Kunshan

Head Office
Branch
Manufacture
Service Site
Parts Center
FinFET Formation

3-D Tri-Gate Transistor Benefits

• Dramatic performance gain at low operating voltage, better than Bulk, PDSOI or FDSOI
  - 37% performance increase at low voltage
  - >50% power reduction at constant performance
• Improved switching characteristics
  (On current vs. Off current)
• Higher drive current for a given transistor footprint
  • Only 2-3% cost adder (vs. ~10% for FDSOI)

3-D Tri-Gate transistors are an important innovation needed to continue Moore’s Law

Source: Intel

download.intel.com/newsroom/kits/22nm/pdfs/22nm-Announcement_Presentation.pdf

Does FinFET require more process steps???
FinFET Process Flow Comparison

2D Planar

- STI Ox CMP
- STI Ox Recess
- SiN Removal

FinFET

- STI Ox CMP
- STI Ox Recess & Gate Height Control
- SiN Removal
- Fin Corner Rounding
- Sac-Ox Removal

Few more process are needed for FinFET formation

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<td>Double Patterning</td>
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Scaling Cost Challenges

The Fabless community openly discuss concerns about cost...
Expanding Requirements: Scaling, Structure/Material

CMOS Scaling

Patterning

More Moore

More than Moore

Advanced Packaging

Memory

FEOL

BEOL

Si Photonics

EUV

DP/MP

Source: TEL based on ITRS

Takashi Hayakawa / Tokyo Electron Limited / March 18th, 2015
# Inflection Point in Patterning (2D → 1D)

## 90nm (Planar Poly Gate)

<table>
<thead>
<tr>
<th>Layout</th>
<th>STI</th>
<th>Gate</th>
<th>Contact 1</th>
<th>Contact 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="SiGe PMOS" /></td>
<td><img src="image2.png" alt="STI" /></td>
<td><img src="image3.png" alt="Gate" /></td>
<td><img src="image4.png" alt="Contact 1" /></td>
<td>NA</td>
</tr>
<tr>
<td>T. Ghani, et al., IEDM 2003</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## 45nm (Planar RMG)

<table>
<thead>
<tr>
<th>Layout</th>
<th>STI</th>
<th>Gate</th>
<th>Contact 1</th>
<th>Contact 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image5.png" alt="PMOS" /></td>
<td><img src="image6.png" alt="STI" /></td>
<td><img src="image7.png" alt="Gate" /></td>
<td><img src="image8.png" alt="Contact 1" /></td>
<td>2-Level Local Interconnect</td>
</tr>
<tr>
<td>K. Mistry, et al., IEDM 2003</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## 22nm (FinFET RMG)

<table>
<thead>
<tr>
<th>Layout</th>
<th>STI</th>
<th>Gate</th>
<th>Contact 1</th>
<th>Contact 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image9.png" alt="C. Auth et al., VLSI tech. 2012" /></td>
<td><img src="image10.png" alt="STI" /></td>
<td><img src="image11.png" alt="Gate" /></td>
<td><img src="image12.png" alt="Contact 1" /></td>
<td>LELE</td>
</tr>
<tr>
<td>C-H Jan, et al., IEDM 2012</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

There is design simplification together with processing complexity
## Self-Aligned Multiple Patterning

<table>
<thead>
<tr>
<th></th>
<th>32nm</th>
<th>10nm</th>
<th>7nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active</td>
<td>193i</td>
<td>SADP + Cut</td>
<td>1+1 SAQP + LE2 Cut</td>
</tr>
<tr>
<td>Gate</td>
<td>193i + Cut</td>
<td>SADP + Cut</td>
<td>1+1 SADP + Cut</td>
</tr>
<tr>
<td>Contact</td>
<td>193i + 193i</td>
<td>LE2+LE2</td>
<td>4 LE2 + LE3</td>
</tr>
<tr>
<td>Via 0</td>
<td>193i</td>
<td>LE2</td>
<td>2 LE3</td>
</tr>
<tr>
<td>Metal 1</td>
<td>193i + Cut</td>
<td>LE3</td>
<td>3 SADP + LE3 Block</td>
</tr>
<tr>
<td>Via 1</td>
<td>193i</td>
<td>LE2</td>
<td>2 LE4</td>
</tr>
<tr>
<td>Metal 2</td>
<td>193i + Cut</td>
<td>SADP + Block</td>
<td>1+1 SAQP + LE3 Block</td>
</tr>
<tr>
<td><strong>Mask Count</strong></td>
<td><strong>12</strong></td>
<td><strong>17</strong></td>
<td><strong>25</strong></td>
</tr>
</tbody>
</table>

Source: Julien R, IMEC

SaMP also increase process complexity
Extendability of SADP

Because of EUV introduction delay, SaDP can be extended to 4x and 8x pitch multiplication

SAOP : Self-Aligned Octuple Patterning
Edge Placement Error in SA Multi Patterning

PAST:
Single pattern variation defined by CDU, overlay and LWR

FUTURE:
Multiple pattern variation defined by Edge Placement Error (EPE)

\[ EPE_{\text{Grid} + \text{cut}} = f(CDU_{\text{Grid}}, LER_{\text{Grid}}, LCDU_{\text{Grid}}, OL_{\text{Cut}}, CDU_{\text{Cut}}, CER_{\text{Cut}}, LCDU_{\text{Cut}}) \]

Multiple patterning increases variability (2x, 3x...more)
## Process Assumptions for N7 (EUV Intro.)

<table>
<thead>
<tr>
<th></th>
<th>Pitch [nm]</th>
<th>193i SAMP</th>
<th>EUV hybrid</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fin / STI</td>
<td>21 - 24</td>
<td>SAQP + LE2 Cut</td>
<td>SAQP + <strong>EUV Cut</strong></td>
</tr>
<tr>
<td>Gate</td>
<td>40 - 45</td>
<td>SADP + Cut</td>
<td>SADP + <strong>EUV Cut</strong></td>
</tr>
<tr>
<td>Contact</td>
<td>40 - 45</td>
<td>LE2 + LE3</td>
<td><strong>EUV LE2</strong></td>
</tr>
<tr>
<td>Via 0</td>
<td>40 - 45</td>
<td>LE3</td>
<td><strong>EUV SE</strong></td>
</tr>
<tr>
<td>Metal 1</td>
<td>40 - 45</td>
<td>SADP + LE3 Block</td>
<td><strong>EUV SE</strong></td>
</tr>
<tr>
<td>Via 1</td>
<td>45 - 51</td>
<td>LE4</td>
<td><strong>EUV SE</strong></td>
</tr>
<tr>
<td>Metal 2</td>
<td>28 - 36</td>
<td>SAQP + LE3 Block</td>
<td>SAQP + <strong>EUV Block</strong></td>
</tr>
<tr>
<td><strong>Mask Count</strong></td>
<td></td>
<td><strong>25 (193i)</strong></td>
<td><strong>11 (193i 3 + 8 EUV)</strong></td>
</tr>
</tbody>
</table>

Source: Julien R, IMEC

EUV hybrid approach can reduce patterning process complexity
EUV Benefit in N7 Mask Decomposition

Target Design

193i

EUV

4 Masks

1 Mask

Fewer masks reduce overlay contribution to EPE

\[
EPE_{\text{via-to-metal}} = f(CDU_{\text{via}}, LCDU_{\text{via}}, OL_1, OL_2, OL_3, OL_4, CDU_{\text{grid}}, LER_{\text{grid}})
\]

\[
EPE_{\text{via-to-metal}} = f(CDU_{\text{via}}, LCDU_{\text{via}}, OL_1, CDU_{\text{grid}}, LER_{\text{grid}})
\]
Challenges & Opportunities

Thin Film / Diffusion
- Thin Film Quality
- Expand Surface Area
- Film Stack (Warpage, Productivity)
- Doping on Topological Pattern
- Fin Rounding (Sac-Ox, Removal)
- Atomic Layer Deposition
- Variability (Dopant, CD...etc)

Dry Etch
- Twisting / Distortion, Profile
- Multi Film Etch (HAR, Stair)
- Charge up Damage
- High Selectivity, Over Etch
- Loading Effect
- Sidewall Etchback (Extension)

Wet / Clean / Etch
- Pattern Collapse / Leaning
- Chemical Delivery to Small Patterns
- Chemical Exchange
- Depth Axis, Profile Control
- Loading Effect

Advanced Packaging
- TSV Etch: Deep Si Etch
- Metallization (PVD, ECD)
- RDL Formation
- Wafer Thinning
- Wafer Bonder / De-bonder
- Probe & Test

Equipment & process development is ongoing for the various challenges. Except for “Thin Film”, “Diffusion” & 3DI, the remaining indicates conventional scaling technologies, not specific to 3D devices.
Short Summary of Further Scaling Scenario

• Almost all CMOS devices have adapted to 3D structure, Capacitor, 3D NAND, FinFET…

• In parallel, scaling centric tool & process development with economical cost is important
Mechanism of Pattern Collapse

Ref.: ECS2013, Advanced wafer drying technology for 1x node and beyond using Surface Modification Method

Fluid on Wafer → Evaporation of Fluid → Pattern Collapse

*Laplace Pressure*

\[ \Delta P = P_2 - P_1 \]

\[ \Delta P = \frac{\gamma}{R} = \frac{2\gamma \cos \theta}{S} \]

\( \gamma \): Surface tension,
\( R \): Radius of curvature

*Pattern Collapse Force*

\[ F = \left( \frac{2\gamma \cos \theta}{S} \right) \times H \times D \]

Collapse force can be controlled by surface condition & hydrophobicity
# Chemical Drying Method Comparison

Ref. : ECS2013, Advanced wafer drying technology for 1x node and beyond using Surface Modification Method

<table>
<thead>
<tr>
<th></th>
<th>Liquid IPA</th>
<th>F-Solvent</th>
<th>SMM**</th>
</tr>
</thead>
<tbody>
<tr>
<td>Final Drying Liquid</td>
<td>IPA</td>
<td>HFE</td>
<td>Water</td>
</tr>
<tr>
<td>*Surface Tension(mN/m)</td>
<td>22</td>
<td>14</td>
<td>73</td>
</tr>
<tr>
<td>Contact Angle(°)@SiO2</td>
<td>10 (0.98)</td>
<td>10 (0.98)</td>
<td>92 (-0.035)</td>
</tr>
</tbody>
</table>

* Value 20° C, **SMM : Surface Modification Method  \( (\ ) = \cos \theta \)

## Pattern Feature
- Vertical line and space pattern with 18nm width
- (1: 1 pitch, 2 dimensions)
- Patterning substrate : Si (Young’s modulus : 112[GPa])

## Surface Modification Method
Successfully prevents failure due to collapse
Surface Modification Agent Reaction

Ref. : ECS2013, Advanced wafer drying technology for 1x node and beyond using Surface Modification Method

Control contact angle, $\cos \theta = \sim 1.0$, minimize collapse force
Experimental Results

Ref.: ECS2013, Advanced wafer drying technology for 1x node and beyond using Surface Modification Method

Surface Modification Method:
Process time 120sec

Surface modification method is effective in minimizing the failure.
Etch Challenges : SAC (Self-Aligned Contact)

2D Planar
- STI Ox CMP
- STI Ox Recess
- SiN Removal

FinFET
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22nm & beyond technologies require SAC process
Model of SiO₂ Selective Etch Over Si₃N₄

Ref. : AVS2014 Dielectric Etch Challenges and Evolutions

<table>
<thead>
<tr>
<th>Low Wafer Temperature</th>
<th>High Wafer Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>O₂ = -2sccm</td>
</tr>
</tbody>
</table>

| Post Ash              |                         |                         |
|                       | Just Etch               | Under Etch              |
|                       |                         |                         |

| Post HF dip           |                         |                         |
| 150nm                 | 50nm                    |                         |
| 10.2nm                | 7.2nm                   | 6.8nm                   |
| 10-15nm               |                         | 4.6nm                   |

SEM Images : Wafer Temp. Split (Condition = CxFy/Ar/O₂ Chemistry)

Higher wafer temperature condition is one of the effective solution to suppress SiN shoulder loss during SAC etching
Investigation of Selectivity Difference

Ref. : AVS2014 Dielectric Etch Challenges and Evolutions

At higher wafer temp., fluorocarbon (FC) deposition thickness on SiO decreases, while FC deposition thickness on SiN is almost kept. In addition, C/F ratio become higher, as wafer temp. become higher.
To Realize Furthermore Highly Selective Etch

Ref. : AVS2014 Dielectric Etch Challenges and Evolutions

ALE, Atomic Layer Etch, is one of the powerful candidate to realize ultra highly selective SiO2 etching in SAC, because ALE has a strong potential to control the thinner CF polymer and lower ion energy precisely in principle.
Reaction of FC depo isn’t self-limited, so not mono layer but several atomic layers adsorb in accordance with time and plasma condition of the adsorption step. So we named this process “Quasi-ALE”.

Separation of radical adsorption and ion bombardment step enables independent control of radical and ion flux. With this scheme, precise control of surface reaction layer by layer becomes possible by controlling process time.
Feasibility Study : Quasi-ALE for SAC

Ref. : AVS2014 Dielectric Etch Challenges and Evolutions

Trade off relationship between SiO2 etch through capability and SiN loss amount is improves by Quasi-ALE process
Quasi-ALE process shows the best SiN loss performance with keeping good etch through capability on slit pattern compared to conventional one. ALE is one of the strong candidate to overcome the issues related selectivity.
Summary & Message

Functional Diversification

CMOS Scaling

More Moore

Expanding Requirements: Scaling, Structure/Material, 450mm

Patterning

BEOL

DKF

Wire-Bonding

DRAM

Flip-Chip

2.5D

Si Photonics

Advanced Packaging

Memory

FinFET

SAC

More than Moore

Source: TEL based on ITRS

Expanding Requirements: Scaling, Structure/Material, 450mm
Summary & Message

• There are many technical challenges ahead for the industry and we at Tokyo Electron will continue to provide solutions to address them

• We support, and will continue to support 3D device technology

• Productivity and cost effective process are important factors for continuous scaling

• Collaboration and/or Eco-system is essential for future technology development, and TEL will welcome collaboration with potential partners